MB86965B

FUJITSU

EtherCoupler™ ETHERNET CONTROLLER WITH 10BASE–T TRANSCEIVER

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The MB86965B EtherCoupler™ Ethernet Controller is a high–performance, highly integrated monolithic device, a superset of the Fujitsu MB86965A, that incorporates a network controller with buffer management, Manchester encoder/decoder, 10BASE–T transceiver with on–chip transmit and receive filters, and bus interface for a PC/XT/AT/ISA bus. New features of the MB86965B not present in its predecessor, the MB86965A, are summarized below. The EtherCoupler allows implementation of adapter solutions with as few as four chips. With its optional generic bus mode, it is suitable for use directly on a microprocessor bus, local bus or expansion bus.

A serial EEPROM can be interfaced to the chip for storage of Ethernet ID and configuration settings. The EtherCoupler is designed to be configured electronically, thus eliminating the jumpers typically used to configure system network adapters. When either the reset pin is activated, or a 'software reset' is issued by writing any value to any on–chip address in the range x18 to x1F(hex), the MB86965B will download three essential configuration parameters from the EEPROM to BMPR19.

New Features of the MB86965B EtherCoupler

- Full–duplex capability
- External loopback mode allows testing of all 10BASE–T interface circuits
- Write support for an external Flash boot PROM
- Software Reset now enables the system to fully reset and re–initialize the controller without the need to activate the system reset line
- 24 mA drive capability for IOCHRDY and IOS16 pins to allow direct connection to the ISA bus

ADDITIONAL FEATURES

- Optional, generic host interface to connect to industry–standard microprocessor busses
- Built–in interface for PC/XT™/AT® or compatible busses
- Interface to serial EEPROM for Node ID and configuration storage allows construction of jumperless, electronically–configurable adapters
- Automatic polarity correction on twisted–pair 10BASE–T receive twisted–pair cable
- Allows automatic selection of non conflicting I/O address for self–installing under software control
- High–performance, packet–buffer architecture pipelines data for highest throughput
- On–chip buffer management controls buffer pointers to reduce software overhead and improve performance
- Hash filter for multicast packet reception
- Manchester encoder/decoder tolerates input jitter up to ±18 ns
- Fully compliant with ISO/ANSI/IEEE 8802–3 specifications
- Two network ports, AUI and 10BASE–T, with automatic port selection
- Integrated pulse shaper, and transmit and receive filters
- Selectable 150 Ω and 100 Ω termination for shielded or unshielded twisted–pair cable, respectively
- Powerdown mode to reduce power dissipation in battery–powered equipment
- Low–power CMOS technology
- Single 5–volt power supply
- 160–pin plastic quad flat package (PQFP)

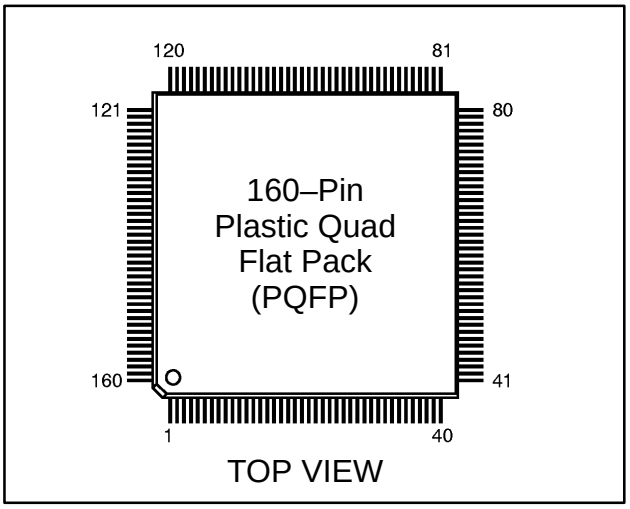

Figure A. Pin Configuration

EtherCoupler's receive and transmit sections fully implement the ISO/ANSI/IEEE 8802–3 CSMA/CD specification for 10 megabit–per–second Ethernet. The transmitter assembles data packets for transmission and the receiver disassembles received data packets. On–chip Ethernet protocol functions include: automatic generation and stripping of the 64–bit preamble; generation and verification of 32–bit cyclic redundancy code (CRC); collision resolution by binary exponential backoff and re–transmission; several modes of address recognition, error detection and reporting; serial/parallel and parallel/serial conversions.

EtherCoupler's transmit buffer is programmable as a single 2–kbyte bank or as two banks of 2, 4, or 8 kbytes each. This buffer chains multiple data packets and transmits them to the network from a single transmit command, thereby offering greater design flexibility and throughput. A ring buffer that can be sized from 4 to 62 kbytes, depending on the amount of available memory, captures the receive packets.

The buffer management architecture of the MB86965B allows packet data to access a buffer memory area simultaneously from the host and from the network media. The network controller updates all receive and transmit pointers automatically to reduce the software overhead needed to control these operations, which results in superior benchmark speed and application performance.

The MB86965B performs pulse shaping and filtering internally, which eliminates the need for external L–C filtering components and reduces overall system cost. EtherCoupler is compatible with shielded and unshielded twisted–pair cables and provides outputs for receive, transmit, collision and link test LEDs. The twisted pair receive threshold can be reduced to allow an extended range between nodes in low–noise environments. Its wide range of features makes EtherCoupler the ideal device for 10BASE–T twisted–pair Ethernet.

Possible configurations for the system bus interface include I/O mapping, memory mapping and DMA access, or a combination of these. With a 20 Mbyte/s bandwidth, the EtherCoupler system bus interface allows use of full throughput capacity of its packet–buffering architecture. EtherCoupler bus modes are selectable, thereby providing big or little endian byte–ordering, permitting efficient data interface with most microprocessors and higher–level protocols. The Fujitsu high–speed, low–power CMOS process is used to manufacture the MB86965B, which is furnished in a 160–pin plastic quad flat package.

Pin Function Changes

The pinout of the MB86965B is identical to that of its predecessor, the MB86965A, except for two new functions added to pins 60 and 108. Refer to the MB86965 data sheet for the following descriptions.

Pin 60 is a dual–function pin in the MB86965B, designated LEDC/$\overline{\text{FDX}}$. It retains its original function as a driver output for a collision indicator LED. In addition, if the pin is grounded by an
external switch, jumper or open–collector gate, the 10BASE–T port will operate in full–duplex mode. It does this by disabling the collision function of the 10BASE–T port, which normally activates if a packet or fragment is received while the chip is transmitting. This mode can be used to increase transmission speed, or to perform loopback testing on the 10BASE–T port through an externally–applied loop.

Pin 108 is also a dual–function pin, designated $\overline{\text{SMEMWR}}$/RDYPOL. In ISA–BUS compatible operating modes 0, 1 and 2 (when one or both of mode pins 91 and 92 are tied low), pin 108 serves as the 'system memory write' input ($\overline{\text{SMEMWR}}$) to support writing to a Flash Boot ROM (For this purpose, it should be connected to the system memory write pin of the PC/XT/AT/ISA bus connector.) In these three modes, the MB86965B will provide chip select pulses to the boot ROM for both read and write operations. In mode 3 (pins 91 and 92 both tied high), this function is disabled as no boot ROM support is available in this mode. In mode 3, pin 108 reverts to its original role in the MB86965A as RDYPOL, an input to select the polarity of the ready pin.

PACKAGE STYLE	PACKAGE CODE	ORDERING CODE
160–Pin Plastic Quad Flat Package	FPT–160P–M03	MB86965BPF–G–BND

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