Features

- **1.65V - 1.95V Read/Write**
- **High Performance**
  - **Random Access Time – 70 ns**
  - **Page Mode Read Time – 20 ns**
  - **Synchronous Burst Frequency – 66 MHz**
  - **Configurable Burst Operation**
- **Sector Erase Architecture**
  - **Sixteen 4K Word Sectors with Individual Write Lockout**
  - **Two Hundred Fifty-four 32K Word Main Sectors with Individual Write Lockout**
- **Typical Sector Erase Time: 32K Word Sectors – 500 ms; 4K Word Sectors – 100 ms**
- **Thirty-two Plane Organization, Permitting Concurrent Read in Any of the Thirty-one Planes not Being Programmed/Erased**
- **Suspend/Resume Feature for Erase and Program**
  - **Supports Reading and Programming Data from Any Sector by Suspending Erase of a Different Sector**
  - **Supports Reading Any Word by Suspending Programming of Any Other Word**
- **Low-power Operation**
  - **30 mA Active**
  - **10 µA Standby**
- **VPP Pin for Write Protection and Accelerated Program/Erase Operations**
- **RESET Input for Device Initialization**
- **CBGA and TSOP Packages**
- **Seventeen 128-bit Protection Registers (2,176 Bits)**
- **Common Flash Interface (CFI)**

Description

The AT49SN/SV12804 is a 1.8-volt 128-megabit Flash memory. The memory is divided into multiple sectors and planes for erase operations. The AT49SN/SV12804 is organized as 8,388,608 x 16 bits. The device can be read or reprogrammed off a single 1.8V power supply, making it ideally suited for In-System programming. The device can be configured to operate in the asynchronous/page read (default mode) or burst read mode (not available for the AT49SV12804). The burst read mode is used to achieve a faster data rate than is possible in the asynchronous/page read mode. If the $\overline{AVD}$ and the CLK signals are both tied to GND and the burst configuration register is configured to perform asynchronous reads, the device will behave like a standard asynchronous Flash memory. In the page mode, the $\overline{AVD}$ signal can be tied to GND or can be pulsed low to latch the page address. In both cases the CLK can be tied to GND.

The AT49SN/SV12804 is divided into thirty-two memory planes. A read operation can occur in any of the thirty-one planes which is not being programmed or erased. This concurrent operation allows improved system performance by not requiring the system to wait for a program or erase operation to complete before a read is performed. To further increase the flexibility of the device, it contains an Erase Suspend and Program Suspend feature. This feature will put the erase or program on hold for any amount of time and let the user read data from or program data to any of the remaining sectors. There is no reason to suspend the erase or program operation if the data to be read is in another memory plane.

The VPP pin provides data protection and faster programming and erase times. When the V_{PP} input is below 0.4V, the program and erase functions are inhibited. When V_{PP} is at 0.9V or above, normal program and erase operations can be performed. With V_{PP} at 12.0V, the program (Dual-word Program command) and erase operations are accelerated.

128-megabit (8M x 16) Burst/Page Mode 1.8-volt Flash Memory

AT49SN12804
AT49SV12804

Preliminary

AT49SN/SV12804: Pin Configurations

| Pin Name	Pin Function
I/O0 - I/O15	Data Inputs/Outputs
A0 - A22	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{AVD}$[1]	Address Latch Enable
CLK[1]	Clock
$\overline{RESET}$	Reset
$\overline{WP}$[1]	Write Protect
VPP	Write Protection and Power Supply for Accelerated Program Operations
WAIT[1]	WAIT
VCCQ	Output Power Supply

Note: 1. These signals are not available for use with the AT49SV12804. The AT49SV12804 can only be used in the asynchronous/page mode.

AT49SN12804: CBGA – Top View
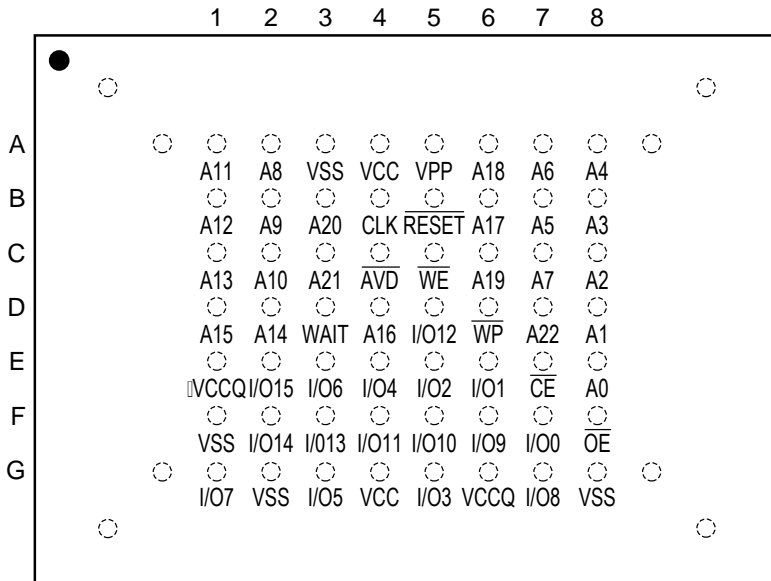
AT49SV12804: TSOP – Top View
Type 1
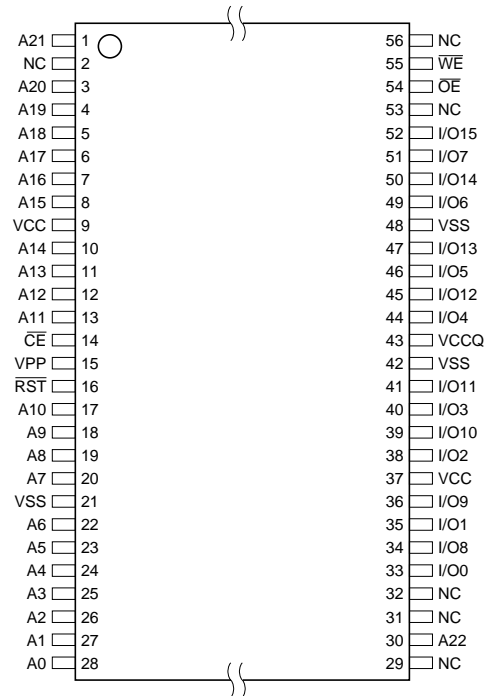
Device Operation

COMMAND SEQUENCES: When the device is first powered on, it will be in the read mode. Command sequences are used to place the device in other operating modes such as program and erase. The command sequences are written by applying a low pulse on the $\overline{WE}$ input with $\overline{CE}$ low and $\overline{OE}$ high or by applying a low-going pulse on the $\overline{CE}$ input with $\overline{WE}$ low and $\overline{OE}$ high. Prior to the low-going pulse on the $\overline{CE}$ or $\overline{WE}$ signal, the address input may be latched by a low-to-high transition on the $\overline{AVD}$ signal. If the $\overline{AVD}$ is not pulsed low, the address will be latched on the first rising edge of the $\overline{WE}$ or $\overline{CE}$. Valid data is latched on the rising edge of the $\overline{WE}$ or the $\overline{CE}$ pulse, whichever occurs first. The addresses used in the command sequences are not affected by entering the command sequences.

BURST CONFIGURATION COMMAND: The Program Burst Configuration Register command is used to program the burst configuration register. The burst configuration register determines several parameters that control the read operation of the device. Bit B15 determines whether synchronous burst reads are enabled or asynchronous reads are enabled. Since the page read operation is an asynchronous operation, bit B15 must be set for asynchronous reads to enable the page read feature. Bit B14 determines whether a four-word page or an eight-word page will be used. The rest of the bits in the burst configuration register are used only for the burst read mode. Bits B13 - B11 of the burst configuration register determine the clock latency for the burst mode. The latency can be set to two, three, four, five or six cycles. The clock latency versus input clock frequency table is shown on page 20. The "Burst Read Waveform" as shown on page 31 illustrates a clock latency of four; the data is output from the device four clock cycles after the first valid clock edge following the high-to-low $\overline{AVD}$ edge. The B10 bit of the configuration register determines the polarity of the WAIT signal. The B9 bit of the burst configuration register determines the number of clocks that data will be held valid (see Figure 4). The Hold Data for 2 Clock Cycles Read Waveform is shown on page 31. The clock latency is not affected by the value of the B9 bit. The B8 bit of the burst configuration register determines when the WAIT signal will be asserted. When synchronous burst reads are enabled, a linear burst sequence is selected by setting bit B7. Bit B6 selects whether the burst starts and the data output will be relative to the falling edge or the rising edge of the clock. Bits B2 - B0 of the burst configuration register determine whether a continuous or fixed-length burst will be used and also determine whether a four-, eight- or sixteen-word length will be used in the fixed-length mode. When a four-, eight- or sixteen-word burst length is selected, Bit B3 can be used to select whether burst accesses wrap within the burst length boundary or whether they cross word length boundaries to perform linear accesses (see Table 5). All other bits in the burst configuration register should be programmed as shown on page 20. The default state (after power-up or reset) of the burst configuration register is also shown on page 20.

ASYNCHRONOUS READ: There are two types of asynchronous reads – $\overline{AVD}$ pulsed and standard asynchronous reads. The $\overline{AVD}$ pulsed read operation of the device is controlled by $\overline{CE}$, $\overline{OE}$, and $\overline{AVD}$ inputs. The outputs are put in the high-impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention. The data at the address location defined by A0 - A22 and captured by the $\overline{AVD}$ signal will be read when $\overline{CE}$ and $\overline{OE}$ are low. The address location passes into the device when $\overline{CE}$ and $\overline{AVD}$ are low; the address is latched on the low-to-high transition of $\overline{AVD}$. Low input levels on the $\overline{OE}$ and $\overline{CE}$ pins allow the data to be driven out of the device. The access time is measured from stable address, falling edge of $\overline{AVD}$ or falling edge of $\overline{CE}$, whichever occurs last. During the $\overline{AVD}$ pulsed read, the CLK signal may be static high or static low. For standard asynchronous reads, the $\overline{AVD}$ and CLK signal should be tied to GND. The asynchronous read diagrams are shown on page 28.

PAGE READ: The page read operation of the device is controlled by $\overline{CE}$, $\overline{OE}$, and $\overline{AVD}$ inputs. The CLK input is ignored during a page read operation and should be tied to GND. The page size can be four words (default value) or eight words depending on what value bit B14 of the burst configuration register is programmed to. During a page read, the $\overline{AVD}$ signal can transition low and then transition high, transition low and remain low, or can be tied to GND. If a high to low transition on the $\overline{AVD}$ signal occurs, as shown in Page Read Cycle Waveform 1, the

page address is latched by the low-to-high transition of the $\overline{\text{AVD}}$ signal. However, if the $\overline{\text{AVD}}$ signal remains low after the high-to-low transition or if the $\overline{\text{AVD}}$ signal is tied to GND, as shown in Page Read Cycle Waveform 2, then the page address (determined by A22 - A3 for an eight word page and A22 - A2 for a four-word page) cannot change during a page read operation. The first word access of the page read is the same as the asynchronous read. The first word is read at an asynchronous speed of 90 ns. Once the first word is read, toggling A0 and A1 (four-word page mode) or toggling A0, A1, and A2 (eight word page mode) will result in subsequent reads within the page being output at a speed of 20 ns. If the $\overline{\text{AVD}}$ and the CLK pins are both tied to GND, the device will behave like a standard asynchronous Flash memory. The page read diagrams are shown on page 22.

SYNCHRONOUS READS: Synchronous reads (not available on the AT49SV12804) are used to achieve a faster data rate that is possible in the asynchronous/page read mode. The device can be configured for continuous or fixed-length burst access. The burst read operation of the device is controlled by $\overline{\text{CE}}$, $\overline{\text{OE}}$, CLK and $\overline{\text{AVD}}$ inputs. The initial read location is determined as for the $\overline{\text{AVD}}$ pulsed asynchronous read operation; it can be any memory location in the device. In the burst access, the address is latched on the rising edge of the first clock pulse when $\overline{\text{AVD}}$ is low or the rising edge of the $\overline{\text{AVD}}$ signal, whichever occurs first. The CLK input signal controls the flow of data from the device for a burst operation. After the clock latency cycles, the data at the next burst address location is read for each following clock cycle.

Figure 1. Word Boundary

16-word Boundary
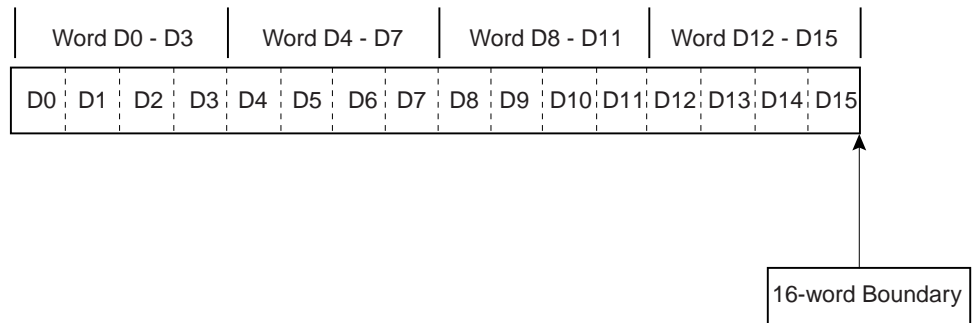
CONTINUOUS BURST READ: During a continuous burst read, any number of addresses can be read from the memory. When operating in the linear burst read mode (B7 = 1) with the burst wrap bit (B3 = 1) set, the device may incur an output delay when the burst sequence crosses the first 16-word boundary in the memory (see Figure 1). If the starting address is D0 - D12, there is no delay. If the starting address is D13 - D15, an output delay equal to the initial clock latency is incurred. The delay takes place only once, and only if the burst sequence crosses a 16-word boundary. To indicate that the device is not ready to continue the burst, the device will drive the WAIT pin low (B10 and B8 = 0) during the clock cycles in which new data is not being presented. Once the WAIT pin is driven high (B10 and B8 = 0), the current data will be valid. The WAIT signal will be tri-stated when the $\overline{\text{CE}}$ or $\overline{\text{OE}}$ signal is high.

In the "Burst Read Waveform" as shown on page 31, the valid address is latched at point A. For the specified clock latency of three, data D13 is valid within 13 ns of clock edge B. The low-to-high transition of the clock at point C results in D14 being read. The transition of the clock at point D results in a burst read of D15. The clock transition at point E does not cause new data to appear on the output lines because the WAIT signal goes low (B10 and B8 = 0) after the clock transition, which signifies that the first boundary in the memory has been crossed and that new data is not available. After a clock latency of three, the clock transition at point F does cause a burst read of data D16 because the WAIT signal goes high (B10 and B8 = 0) after the clock transition indicating that new data is available. Additional clock transitions, like at point G, will continue to result in burst reads.

FIXED-LENGTH BURST READS: During a fixed-length burst mode read, four, eight or sixteen words of data may be burst from the device, depending upon the configuration. The device supports a linear burst mode. The burst sequence is shown on page 21. When operating in the linear burst read mode (B7 = 1) with the burst wrap bit (B3 = 1) set, the device may incur an output delay when the burst sequence crosses the first 16-word boundary in the memory. If the starting is D0 - D12, there is no delay. If the starting address is D13 - D15, an output delay equal to the initial clock latency is incurred. The delay takes place only once, and only if the burst sequence crosses a 16-word boundary. To indicate that the device is not ready to continue the burst, the device will drive the WAIT pin low (B10 and B8 = 0) during the clock cycles in which new data is not being presented. Once the WAIT pin is driven high (B10 and B8 = 0), the current data will be valid. The WAIT signal will be tri-stated when the $\overline{CE}$ or $\overline{OE}$ signal is high.

The "Four-word Burst Read Waveform" on page 32 illustrates a fixed-length burst cycle. The valid address is latched at point A. For the specified clock latency of four, data D0 is valid within 13 ns of clock edge B. The low-to-high transition of the clock at point C results in D1 being read. Similarly, D2 and D3 are output following the next two clock cycles. Returning $\overline{CE}$ high ends the read cycle. There is no output delay in the burst access wrap mode (B3 = 0).

BURST SUSPEND: The Burst Suspend feature allows the system to temporarily suspend a synchronous burst operation if the system needs to use the Flash address and data bus for other purposes. Burst accesses can be suspended during the initial latency (before data is received) or after the device has output data. When a burst access is suspended, internal array sensing continues and any previously latched internal data is retained.

Burst Suspend occurs when $\overline{CE}$ is asserted, the current address has been latched (either rising edge of $\overline{AVD}$ or valid CLK edge), CLK is halted, and $\overline{OE}$ is deasserted. The CLK can be halted when it is at V_{IH} or V_{IL}. To resume the burst access, $\overline{OE}$ is reasserted and the CLK is restarted. Subsequent CLK edges resume the burst sequence where it left off.

Within the device, $\overline{OE}$ gates the WAIT signal. Therefore, during Burst Suspend the WAIT signal reverts to a high-impedance state when $\overline{OE}$ is deasserted. See "Burst Suspend Waveform" on page 32.

RESET: A $\overline{RESET}$ input pin is provided to ease some system applications. When $\overline{RESET}$ is at a logic high level, the device is in its standard operating mode. A low level on the $\overline{RESET}$ pin halts the present device operation and puts the outputs of the device in a high-impedance state. When a high level is reasserted on the $\overline{RESET}$ pin, the device returns to read mode.

ERASE: Before a word can be reprogrammed it must be erased. The erased state of the memory bits is a logical "1". The entire memory can be erased by using the Chip Erase command or individual planes can be erased by using the Plane Erase command or individual sectors can be erased by using the Sector Erase command.

CHIP ERASE: Chip Erase is a two-bus cycle operation. The automatic erase begins on the rising edge of the last $\overline{WE}$ pulse. Chip Erase does not alter the data of the protected sectors. The hardware reset during chip erase will stop the erase, but the data will be of an unknown state.

PLANE ERASE: As an alternative to a full Chip Erase, the device is organized into thirty-two planes that can be individually erased. The Plane Erase command is a two-bus cycle operation. The plane whose address is valid at the second rising edge of $\overline{WE}$ will be erased. The Plane Erase command does not alter the data in the protected sectors.

SECTOR ERASE: The device is organized into multiple sectors that can be individually erased. The Sector Erase command is a two-bus cycle operation. The sector whose address is valid at the second rising edge of $\overline{WE}$ will be erased provided the given sector has not been protected.

WORD PROGRAMMING: The device is programmed on a word-by-word basis. Programming is accomplished via the internal device command register and is a two-bus cycle operation. The programming address and data are latched in the second cycle. The device will automatically generate the required internal programming pulses. Please note that a "0" cannot be programmed back to a "1"; only erase operations can convert "0"s to "1"s.

FLEXIBLE SECTOR PROTECTION: The AT49SN/SV12804 offers two sector protection modes, the Softlock and the Hardlock. The Softlock mode is optimized as sector protection for sectors whose content changes frequently. The Hardlock protection mode is recommended for sectors whose content changes infrequently. Once either of these two modes is enabled, the contents of the selected sector is read-only and cannot be erased or programmed. Each sector can be independently programmed for either the Softlock or Hardlock sector protection mode. At power-up and reset, all sectors have their Softlock protection mode enabled.

SOFTLOCK AND UNLOCK: The Softlock protection mode can be disabled by issuing a two-bus cycle Unlock command to the selected sector. Once a sector is unlocked, its contents can be erased or programmed. To enable the Softlock protection mode, a two-bus cycle Softlock command must be issued to the selected sector.

HARDLOCK AND WRITE PROTECT ($\overline{WP}$): The Hardlock sector protection mode operates in conjunction with the Write Protection ($\overline{WP}$) pin. The Hardlock sector protection mode can be enabled by issuing a two-bus cycle Hardlock software command to the selected sector. The state of the Write Protect pin affects whether the Hardlock protection mode can be overridden.

- When the $\overline{WP}$ pin is low and the Hardlock protection mode is enabled, the sector cannot be unlocked and the contents of the sector is read-only.
- When the $\overline{WP}$ pin is high, the Hardlock protection mode is overridden and the sector can be unlocked via the Unlock command.

To disable the Hardlock sector protection mode, the chip must be either reset or power cycled.

Table 1. Hardlock and Softlock Protection Configurations in Conjunction with $\overline{WP}$

V_{PP}	$\overline{WP}$	Hard-lock	Soft-lock	Erase/ Prog Allowed?	Comments
V_{CC}	0	0	0	Yes	No sector is locked
V_{CC}	0	0	1	No	Sector is Softlocked. The Unlock command can unlock the sector.
V_{CC}	0	1	1	No	Hardlock protection mode is enabled. The sector cannot be unlocked.
V_{CC}	1	0	0	Yes	No sector is locked.
V_{CC}	1	0	1	No	Sector is Softlocked. The Unlock command can unlock the sector.
V_{CC}	1	1	0	Yes	Hardlock protection mode is overridden and the sector is not locked.
V_{CC}	1	1	1	No	Hardlock protection mode is overridden and the sector can be unlocked via the Unlock command.
V_{IL}	x	x	x	No	Erase and Program Operations cannot be performed.

Figure 2. Sector Locking State Diagram
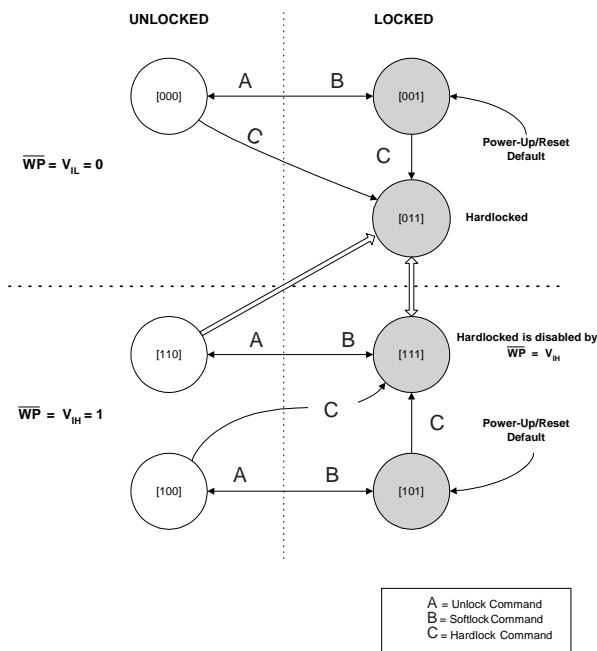
Note: 1. The notation [X, Y, Z] denotes the locking state of a sector. The current locking state of a sector is defined by the state of $\overline{WP}$ and the two bits of the sector-lock status D[1:0].

SECTOR PROTECTION DETECTION: A software method is available to determine if the sector protection Softlock or Hardlock features are enabled. When the device is in the software product identification mode a read from the I/O0 and I/O1 at address location 00002H within a sector will show if the sector is unlocked, softlocked, or hardlocked.

Table 2. Sector Protection Status

I/O1	I/O0	Sector Protection Status
0	0	Sector Not Locked
0	1	Softlock Enabled
1	0	Hardlock Enabled
1	1	Both Hardlock and Softlock Enabled

READ STATUS REGISTER: The status register indicates the status of device operations and the success/failure of that operation. The Read Status Register command causes subsequent reads to output data from the status register until another command is issued. To return to reading from the memory, issue a Read command.

The status register bits are output on I/O7 - I/O0. The upper byte, I/O15 - I/O8, outputs 00H when a Read Status Register command is issued.

The contents of the status register [SR7:SR0] are latched on the falling edge of $\overline{OE}$ or $\overline{CE}$ (whichever occurs last), which prevents possible bus errors that might occur if status register contents change while being read. $\overline{CE}$ or $\overline{OE}$ must be toggled with each subsequent status read, or the status register will not indicate completion of a Program or Erase operation.

When the Write State Machine (WSM) is active, SR7 will indicate the status of the WSM; the remaining bits in the status register indicate whether the WSM was successful in performing the preferred operation (see Table 3).

READ STATUS REGISTER IN THE BURST MODE: The waveform below shows a status register read during a program operation. The two-bus cycle command for a program operation is given followed by a read status register command. Following the read status register command, the $\overline{AVD}$ signal is pulsed low to latch the valid address at point A. With the $\overline{OE}$ signal pulsed low and for the specified clock latency of three, the status register output is valid within 13 ns from clock edge B. The same status register data is output on successive clock edges. To update the status register output, the $\overline{AVD}$ signal needs to be pulsed low and the next data is available after a clock latency of three. The status register output is also available after the chosen clock latency during an erase operation.

Figure 3. Read Status Register in the Burst Mode
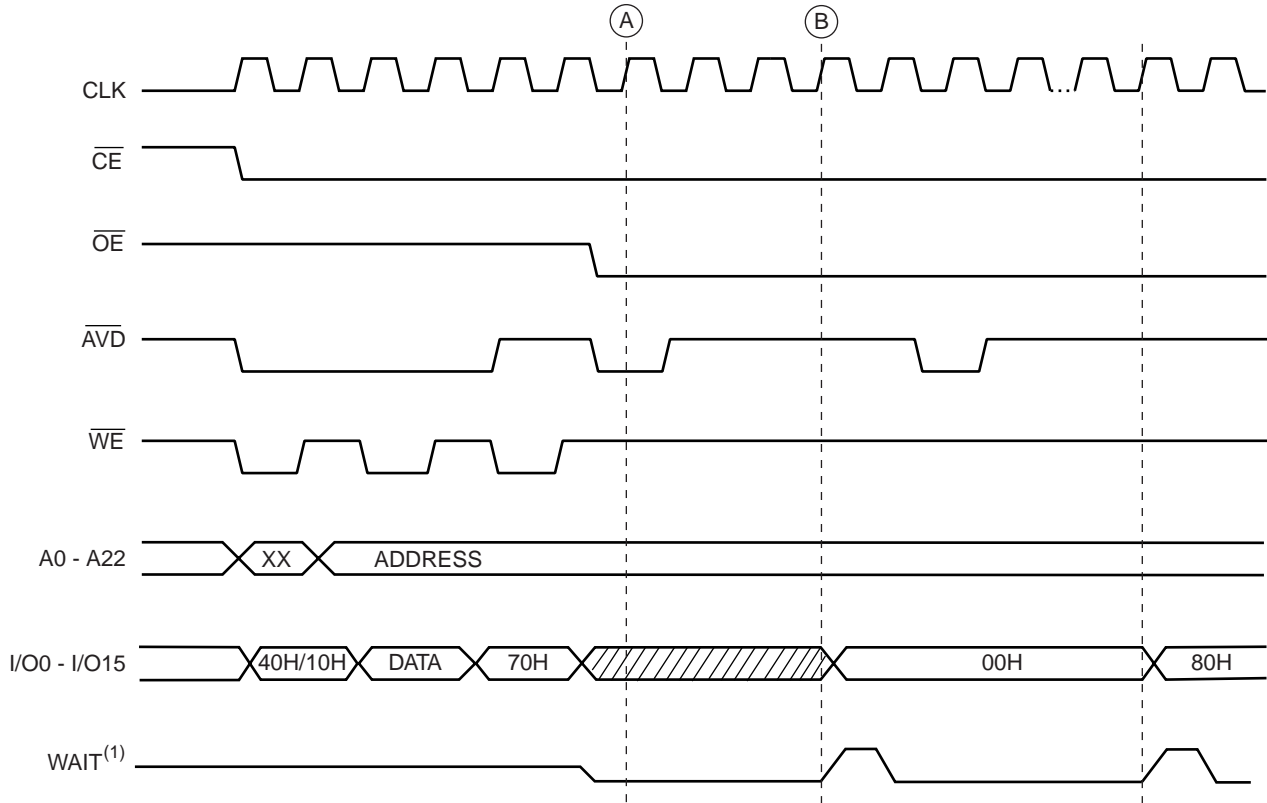
Note: 1. The WAIT signal is for a burst configuration setting of B10 and B8 = 0.

Table 3. Status Register Bit Definition

WSMS	ESS	ES	PRS	VPPS	PSS	SLS	PLS
7	6	5	4	3	2	1	0
				Notes			
SR7 WRITE STATE MACHINE STATUS (WSMS) 1 = Ready 0 = Busy				Check Write State Machine bit first to determine Word Program or Sector Erase completion, before checking program or erase status bits.			
SR6 = ERASE SUSPEND STATUS (ESS) 1 = Erase Suspended 0 = Erase In Progress/Completed				When Erase Suspend is issued, WSM halts execution and sets both WSMS and ESS bits to "1" – ESS bit remains set to "1" until an Erase Resume command is issued.			
SR5 = ERASE STATUS (ES) 1 = Error in Sector Erase 0 = Successful Sector Erase				When this bit is set to "1", WSM has applied the max number of erase pulses to the sector and is still unable to verify successful sector erasure.			
SR4 = PROGRAM STATUS (PRS) 1 = Error in Programming 0 = Successful Programming				When this bit is set to "1", WSM has attempted but failed to program a word			
SR3 = VPP STATUS (VPPS) 1 = VPP Low Detect, Operation Abort 0 = VPP OK				The V_{PP} status bit does not provide continuous indication of VPP level. The WSM interrogates V_{PP} level only after the Program or Erase command sequences have been entered and informs the system if V_{PP} has not been switched on. The V_{PP} is also checked before the operation is verified by the WSM.			
SR2 = PROGRAM SUSPEND STATUS (PSS) 1 = Program Suspended 0 = Program in Progress/Completed				When Program Suspend is issued, WSM halts execution and sets both WSMS and PSS bits to "1". PSS bit remains set to "1" until a Program Resume command is issued.			
SR1 = SECTOR LOCK STATUS 1 = Prog/Erase attempted on a locked sector; Operation aborted. 0 = No operation to locked sectors				If a Program or Erase operation is attempted to one of the locked sectors, this bit is set by the WSM. The operation specified is aborted and the device is returned to read status mode.			
SR0 = Plane Status (PLS)				Indicates program or erase status of the addressed plane.			

Note: 1. A Command Sequence Error is indicated when SR1, SR3, SR4 and SR5 are set.

Table 4. Status Register Device WSMS and Write Status Definition

WSMS (SR7)	PLS (SR0)	Description
0	0	The addressed plane is performing a program/erase operation.
0	1	A plane other than the one currently addressed is performing a program/erase operation.
1	x	No program/erase operation is in progress in any plane. Erase and Program suspend bits (SR6, SR2) indicate whether other planes are suspended.

ERASE SUSPEND/ERASE RESUME: The Erase Suspend command allows the system to interrupt a sector erase or plane erase operation. The erase suspend command does not work with the Chip Erase feature. Using the erase suspend command to suspend a sector erase operation, the system can program or read data from a different sector within the same plane. Since this device is organized into thirty-two planes, there is no need to use the erase suspend feature while erasing a sector when you want to read data from a sector in another plane. After the Erase Suspend command is given, the device requires a maximum time of 15 μs to suspend the erase operation. After the erase operation has been suspended, the plane that contains the suspended sector enters the erase-suspend-read mode. The system can then read data or program data to any other sector within the device. An address is not required during the Erase Suspend command. During a sector erase suspend, another sector cannot be erased. To resume the sector erase operation, the system must write the Erase Resume command. The Erase Resume command is a one-bus cycle command, which does require the plane address. Read, Read Status Register, Product ID Entry, Clear Status Register, Program, Program Suspend, Erase Resume, Sector Softlock/Hardlock, Sector Unlock are valid commands during an erase suspend.

PROGRAM SUSPEND/PROGRAM RESUME: The Program Suspend command allows the system to interrupt a programming operation and then read data from a different word within the memory. After the Program Suspend command is given, the device requires a maximum of 10 μs to suspend the programming operation. After the programming operation has been suspended, the system can then read from any other word within the device. An address is not required during the program suspend operation. To resume the programming operation, the system must write the Program Resume command. The program suspend and resume are one-bus cycle commands. The command sequence for the erase suspend and program suspend are the same, and the command sequence for the erase resume and program resume are the same. Read, Read Status Register, Product ID Entry, Program Resume are valid commands during a Program Suspend.

128-BIT PROTECTION REGISTERS: The AT49SN/SV12804 contains seventeen (PR0 - PR16) 128-bit registers that can be used for security purposes in system design. Please see the Protection Register Addressing Table on page 19 for the address locations within each protection register. The first protection register (PR0) is divided into two 64-bit blocks. The two blocks are designated as block A and block B. The data in block A is non-changeable and is programmed at the factory with a unique number. The data in block B is programmed by the user and can be locked out such that data in the block cannot be reprogrammed. The other 16 registers (PR1 - PR16) have 128 bits (16 words) each that are all user programmable. To program block B in PR0 or to program PR1 - PR16 register, a two-bus cycle command must be used as shown in the Command Definition table on page 18. To lock out block B in PRO or to lock out PR1 - PR16, a two-bus cycle command must also be used as shown in the Command Definition table. To lock out block B in PRO, the address used in the second bus cycle is 080h and data bit D1 must be zero during the second bus cycle. All other data bits during the second bus cycle are don't cares. To lock out PR1 - PR16, the address used in the second bus cycle is 089h and sixteen bits of data are programmed. If any of these bits is programmed to a zero, the appropriate register is locked. After being locked, the protection register cannot be unlocked. To determine whether block B in PRO or PR1 - PR16 is locked out, the Product ID Entry command is given followed by a read operation from address 80H or address 89H, respectively. (This command is shown as status of protection in the Command Definition table). For block B in PRO, if data bit D1 is zero, block B is locked. If data bit D1 is one, block B can be reprogrammed. For PR1 - PR16, sixteen bits of data are read out. Each bit represents the protection status of a particular register. If the bit is a zero, the register is locked. If the bit is a one, the register can be reprogrammed. To read a protection register, the Product ID Entry command is given followed by a normal read operation from an address within the protection register. After determining whether a register is protected or not or reading the protection register, the Read command must be given to return to the read mode.

CFI: Common Flash Interface (CFI) is a published, standardized data structure that may be read from a flash device. CFI allows system software to query the installed device to determine the configurations, various electrical and timing parameters, and functions supported by the device. CFI is used to allow the system to learn how to interface to the flash device most optimally. The two primary benefits of using CFI are ease of upgrading and second source availability. The command to enter the CFI Query mode is a one-bus cycle command which requires writing data 98h to any address. The CFI Query command can be written when the device is ready to read data or can also be written when the part is in the product ID mode. Once in the CFI Query mode, the system can read CFI data at the addresses given in Table on page 31. To return to the read mode, the read command should be issued.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT49SN/SV12804 in the following ways: (a) V_{CC} sense: if V_{CC} is below 1.2V (typical), the device is reset and the program and erase functions are inhibited. (b) V_{CC} power-on delay: once V_{CC} has reached the V_{CC} sense level, the device will automatically time-out 10 ms (typical) before programming. (c) Program inhibit: holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles. (d) Noise filter: pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle. (e) V_{PP} is less than V_{ILPP}.

INPUT LEVELS: While operating with a 1.65V to 1.95V power supply, the address inputs and control inputs ($\overline{OE}$, $\overline{CE}$ and $\overline{WE}$) may be driven from 0 to 2.5V without adversely affecting the operation of the device. The I/O lines can be driven from 0 to V_{CCQ} + 0.6V.

OUTPUT LEVELS: For the AT49SN/SV12804, output high levels are equal to V_{CCQ} - 0.1V (not V_{CC}). V_{CCQ} must be regulated between 1.8V - 2.25V.

Word Program Flowchart
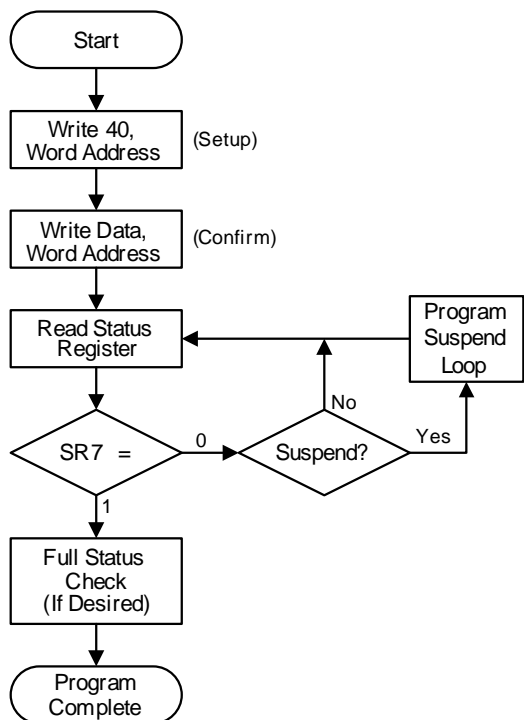
Word Program Procedure

Bus Operation	Command	Comments
Write	Program Setup	Data = 40 Addr = Location to program
Write	Data	Data = Data to program Addr = Location to program
Read	None	Status register data: Toggle $\overline{CE}$ or $\overline{OE}$ to update status register
Idle	None	Check SR7 1 = WSM Ready 0 = WSM Busy

Repeat for subsequent Word Program operations.

Full status register check can be done after each program, or after a sequence of program operations.

Write FF after the last operation to set to the Read state.

Full Status Check Flowchart
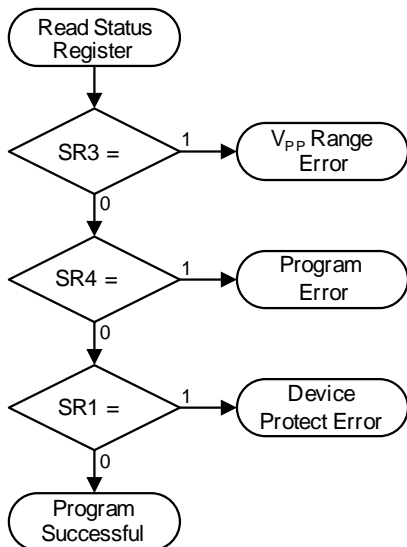
Full Status Check Procedure

Bus Operation	Command	Comments
Idle	None	Check SR3: 1 = V_{PP} Error
Idle	None	Check SR4: 1 = Data Program Error
Idle	None	Check SR1: 1 = Sector locked; operation aborted

SR3 MUST be cleared before the Write State Machine allows further program attempts.

If an error is detected, clear the status register before continuing operations – only the Clear Status Register command clears the status register error bits.

Program Suspend/Resume Flowchart

```
          ┌──────────┐
          │  Start   │
          └──────────┘
                │
                ▼
       ┌─────────────────┐
       │   Write B0      │ (Program Suspend)
       │   Any Address   │
       └─────────────────┘
                │
                ▼
       ┌─────────────────┐
       │   Write 70      │
       │   Any Address   │ (Read Status)
       │     within      │
       │  the Same Plane │
       └─────────────────┘
                │
                ▼
       ┌─────────────────┐◄──────┐
       │  Read Status    │       │
       │    Register     │       │
       └─────────────────┘       │
                │                 │
                ▼                 │
           ╱────────╲    0        │
          ╱  SR7 =   ╲────────────┘
           ╲────────╱
                │ 1
                ▼
           ╱────────╲    0      ┌──────────────┐
          ╱  SR2 =   ╲─────────►│   Program    │
           ╲────────╱           │  Completed   │
                │ 1             └──────────────┘
                ▼                      │
       ┌─────────────────┐             ▼
       │   Write FF      │ (Read    ┌──────────┐  (Read
       │  Suspend Plane  │  Array)  │ Write FF │   Array)
       └─────────────────┘          └──────────┘
                │                         │
                ▼                         ▼
       ┌─────────────────┐◄──┐       ┌──────────┐
       │   Read Data     │   │       │  Read    │
       └─────────────────┘   │       │  Data    │
                │            │       └──────────┘
                ▼            │
           ╱────────╲   No   │
          ╱   Done   ╲───────┘
          ╲ Reading  ╱
           ╲────────╱
                │ Yes
                ▼
       ┌─────────────────┐
       │   Write D0      │ (Program Resume)
       │   Any Address   │
       └─────────────────┘
                │
                ▼
          ┌──────────┐
          │ Program  │
          │ Resumed  │
          └──────────┘
                │
                ▼
       ┌ ─ ─ ─ ─ ─ ─ ─ ─ ┐
       │   Write 70H     │
         Any Address       (Read Status)
       │     within      │
         the Same Plane
       └ ─ ─ ─ ─ ─ ─ ─ ─ ┘
```
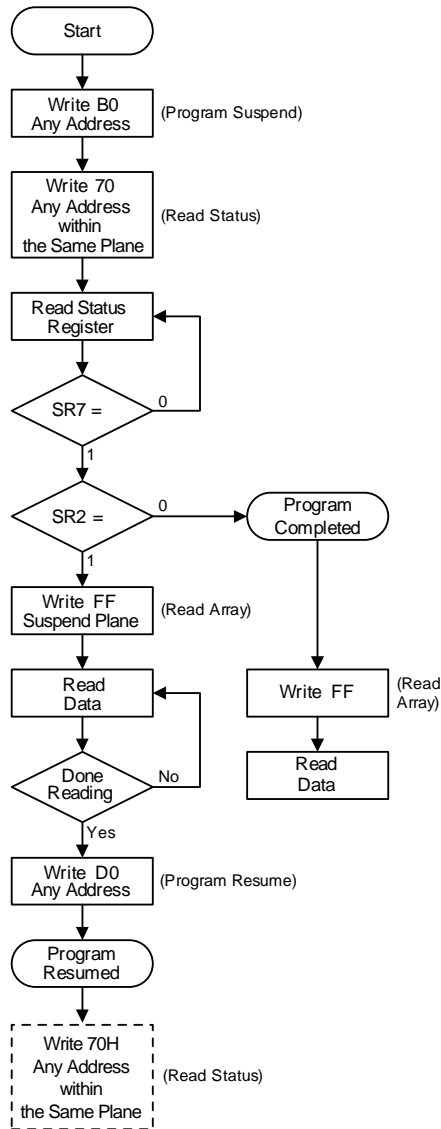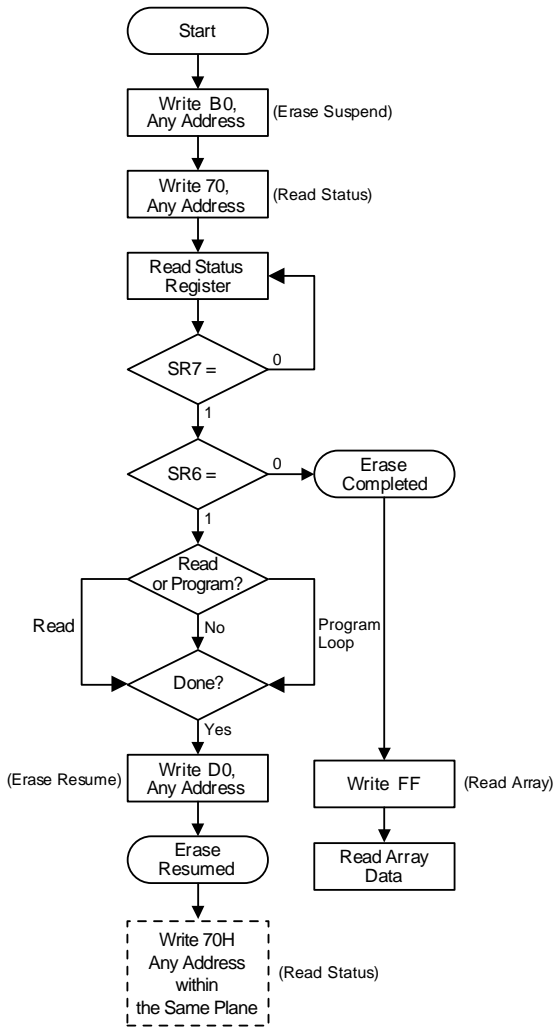
Program Suspend/Resume Procedure

Bus Operation	Command	Comments
Write	Program Suspend	Data = B0 Addr = Sector address to Suspend (SA)
Write	Read Status	Data = 70 Addr = Any address within the Same Plane
Read	None	Status register data: Toggle $\overline{CE}$ or $\overline{OE}$ to update status register Addr = Any address
Idle	None	Check SR7 1 = WSM Ready 0 = WSM Busy
Idle	None	Check SR2 1 = Program suspended 0 = Program completed
Write	Read Array	Data = FF Addr = Any address within the Suspended Plane
Read	None	Read data from any sector in the memory other than the one being programmed
Write	Program Resume	Data = D0 Addr = Any address

If the Suspend Plane was placed in Read mode:

| Write	Read Status	Return Plane to Status mode: Data = 70 Addr = Any address within the Same Plane

Erase Suspend/Resume Flowchart

Erase Suspend/Resume Procedure

Bus Operation	Command	Comments
Write	Erase Suspend	Data = B0 Addr = Any address within the Same Plane
Write	Read Status	Data = 70 Addr = Any address
Read	None	Status register data: Toggle $\overline{CE}$ or $\overline{OE}$ to update status register Addr = Any address within the Same Plane
Idle	None	Check SR7 1 = WSM Ready 0 = WSM Busy
Idle	None	Check SR6 1 = Erase suspended 0 = Erase completed
Write	Read or Program	Data = FF or 40 Addr = Any address
Read or Write	None	Read or program data from/to sector other than the one being erased
Write	Program Resume	Data = D0 Addr = Any address

If the Suspended Plane was placed in Read mode or a Program loop:

| Write	Read Status	Return Plane to Status mode: Data = 70 Addr = Any address within the Same Plane

Sector Erase Flowchart
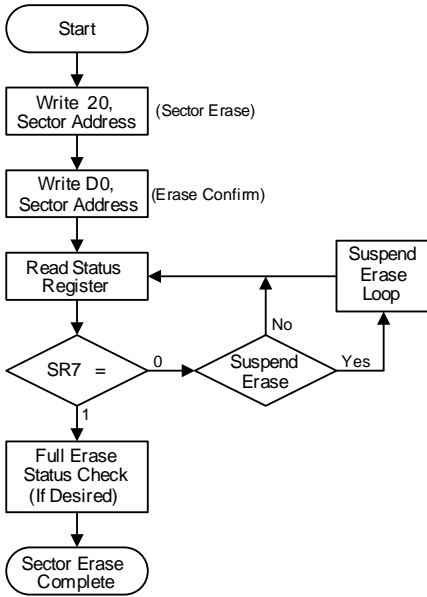
Sector Erase Procedure

Bus Operation	Command	Comments
Write	Sector Erase Setup	Data = 20 Addr = Sector to be erased (SA)
Write	Erase Confirm	Data = D0 Addr = Sector to be erased (SA)
Read	None	Status register data: Toggle $\overline{CE}$ or $\overline{OE}$ to update status register data
Idle	None	Check SR7 1 = WSMS Ready 0 = WSMS Busy
Repeat for subsequent sector erasures. Full status register check can be done after each sector erase, or after a sequence of sector erasures. Write FF after the last operation to enter read mode.		

Full Erase Status Check Flowchart
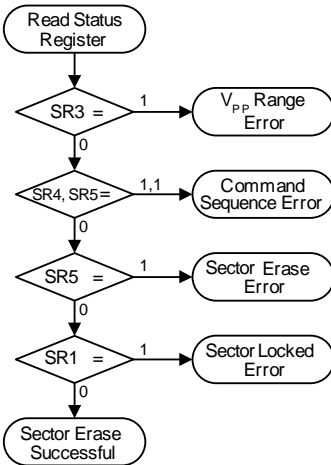
Full Erase Status Check Procedure

Bus Operation	Command	Comments
Idle	None	Check SR3: 1 = V_{PP} Range Error
Idle	None	Check SR4, SR5: Both 1 = Command Sequence Error
Idle	None	Check SR5: 1 = Sector Erase Error
Idle	None	Check SR1: 1 = Attempted erase of locked sector; erase aborted.
SR1, SR3 must be cleared before the Write State Machine allows further erase attempts. Only the Clear Status Register command clears SR1, SR3, SR4, SR5. If an error is detected, clear the status register before attempting an erase retry or other error recovery.		

Protection Register Programming Flowchart

Start

Write C0, PR Address (Program Setup)

Write PR Address & Data (Confirm Data)

Read Status Register

SR7 = → 0

1

Full Status Check (If Desired)

Program Complete
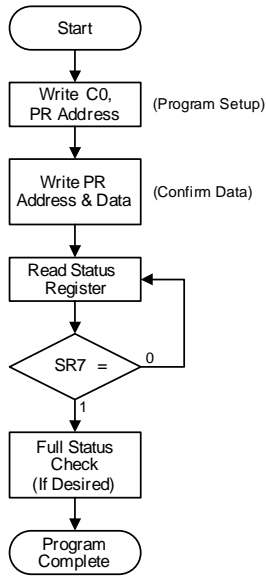
Protection Register Programming Procedure

Bus Operation	Command	Comments
Write	Program PR Setup	Data = C0 Addr = First Location to Program
Write	Protection Program	Data = Data to Program Addr = Location to Program
Read	None	Status register data: Toggle $\overline{CE}$ or $\overline{OE}$ to update status register data
Idle	None	Check SR7 1 = WSMS Ready 0 = WSMS Busy

Program Protection Register operation addresses must be within the protection register address space. Addresses outside this space will return an error.

Repeat for subsequent programming operations.

Full status register check can be done after each program, or after a sequence of program operations.

Write FF after the last operation to return to the Read mode.
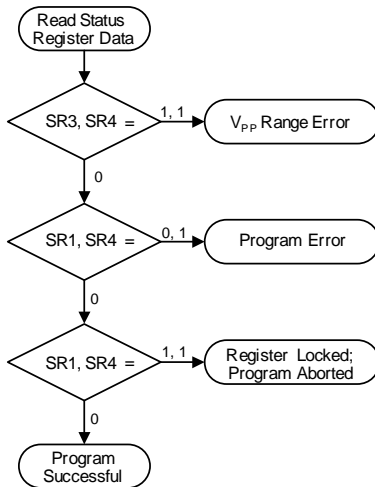
Full Status Check Flowchart

Read Status Register Data

SR3, SR4 = → 1, 1 → V_{PP} Range Error

0

SR1, SR4 = → 0, 1 → Program Error

0

SR1, SR4 = → 1, 1 → Register Locked; Program Aborted

0

Program Successful

Full Status Check Procedure

Bus Operation	Command	Comments
Idle	None	Check SR1, SR3, SR4: 0,1,1 = V_{PP} Range Error
Idle	None	Check SR1, SR3, SR4: 0,0,1 = Programming Error
Idle	None	Check SR1, SR3, SR4: 1, 0,1 = Sector locked; operation aborted

SR3 must be cleared before the Write State Machine allows further program attempts.

Only the Clear Status Register command clears SR1, SR3, SR4.

If an error is detected, clear the status register before attempting a program retry or other error recovery.

Command Definition in Hex[1]

Command Sequence	Bus Cycles	1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle	
		Addr	Data	Addr	Data	Addr	Data
Read	1	PA[2]	FF				
Chip Erase	2	XX	21	Addr	D0		
Plane Erase	2	XX	22	Addr	D0		
Sector Erase	2	SA	20	SA[3]	D0		
Word Program	2	Addr[14]	40/10	Addr[14]	D_{IN}		
Dual Word Program[9]	3	Addr0	E0	Addr0	D_{IN0}	Addr1	D_{IN1}
Erase/Program Suspend	1	XX	B0				
Erase/Program Resume	1	PA	D0				
Product ID Entry[13]	1	PA	90				
Sector Softlock	2	SA	60	SA[3]	01		
Sector Hardlock	2	SA	60	SA[3]	2F		
Sector Unlock	2	SA	60	SA[3]	D0		
Read Status Register	2	PA	70	XX	D_{OUT}[4]		
Clear Status Register	1	XX	50				
Program PR0 (Block B) or PR1-PR16	2	XX[8]	C0	Addr[10]	D_{IN}		
Lock Protection PR0 – Block B	2	80	C0	80	FFFD		
Lock Protection PR1-PR16	2	XX	C0	89	D_{IN}[11]		
Status of Protection PR0 (Block B)	2	PA	90	80	D_{OUT}[5]		
Status of Protection PR1-PR16	2	PA	90	89	D_{OUT}[12]		
Program Burst Configuration Register	2	Addr[6]	60	Addr[6]	03		
Read Burst Configuration Register	2	PA	90	PAX005[7]	D_{OUT}		
CFI Query	1	XX	98				

Notes:
1. The DATA FORMAT shown for each bus cycle is as follows; I/O7 - I/O0 (Hex). I/O15 - I/O8 are don't care. The ADDRESS FORMAT shown for each bus cycle is as follows: A7 - A0 (Hex). Address A22 through A8 are don't care.
2. PA is the plane address (A22 - A18). Any address within a plane can be used.
3. SA = sector address. Any word address within a sector can be used to designate the sector address (see pages 22 - 25 for details).
4. The status register bits are output on I/O7 - I/O0.
5. If data bit D1 is "0", block B is locked. If data bit D1 is "1", block B can be reprogrammed.
6. See "Burst Configuration Register" on page 20. Bits B15 - B0 of the burst configuration register determine A15 - A0. Addresses A16 - A22 can select any plane.
7. The plane address has to be the same as the plane address in the second bus cycle.
8. Any address within the user programmable protection register region.
9. This fast programming option enables the user to program two words in parallel only when V_{PP} = 12V. The addresses, Addr0 and Addr1, of the two words, D_{IN0} and D_{IN1}, must only differ in address A0. This command should be used during manufacturing purposes only.
10. Address locations are shown on next page.
11. D_{IN} represents 16 bits of data. If any bit is programmed to a "0", the appropriate protection register is locked.
12. D_{OUT} represents 16 bits of data. Each bit corresponds to the protection status of a given register. The most significant bit read out corresponds to PR16, and the last significant bit corresponds to PR0. If the data bit is a "0", the register is locked. If the data bits is a "1", the register can be programmed.
13. The manufacturer code is read from address 0000H, and the device code is read from address 0001H.
14. The first bus cycle address should be the same as the word address to be programmed.

Absolute Maximum Ratings*

Temperature under Bias .... -55°C to +125°C

Storage Temperature .... -65°C to +150°C

All Input Voltages Except V_{PP}
(including NC Pins)
with Respect to Ground ....-0.6V to +6.25V

V_{PP} Input Voltage
with Respect to Ground .... 0V to 12.5V

All Output Voltages
with Respect to Ground ....-0.6V to V_{CCQ} + 0.6V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Protection Register Addressing Table

	Address	Use	Block	A8	A7	A6	A5	A4	A3	A2	A1	A0
PRO	81	Factory	A	0	1	0	0	0	0	0	0	1
	82	Factory	A	0	1	0	0	0	0	0	1	0
	83	Factory	A	0	1	0	0	0	0	0	1	1
	84	Factory	A	0	1	0	0	0	0	1	0	0
	85	User	B	0	1	0	0	0	0	1	0	1
	86	User	B	0	1	0	0	0	0	1	1	0
	87	User	B	0	1	0	0	0	0	1	1	1
	88	User	B	0	1	0	0	0	1	0	0	0

	Address	Use	Block	A8	A7	A6	A5	A4	A3	A2	A1	A0
PR1	8A	User		0	1	0	0	0	1	0	1	0
	• • •			• • •								
	91	User		0	1	0	0	1	0	0	0	1

	Address	Use	Block	A8	A7	A6	A5	A4	A3	A2	A1	A0
PR2	92	User		0	1	0	0	1	0	0	1	0
	• • •			• • •								
	A1	User		0	1	0	1	0	0	0	0	1

	Address	Use	Block	A8	A7	A6	A5	A4	A3	A2	A1	A0
PR16	102	User		1	0	0	0	0	0	0	1	0
	• • •			• • •								
	109	User		1	0	0	0	0	1	0	0	1

Note: 1. All address lines not specified in the above table must be 0 when accessing the Protection Register, i.e., A22 - A9 = 0.

Burst Configuration Register

B15	0 1[1]	Synchronous Burst Reads Enabled Asynchronous Reads Enabled
B14	0[1] 1	Four-word Page Eight-word Page
B13 - B11:	010[2] 011 100 101 110[1]	Clock Latency of Two Clock Latency of Three Clock Latency of Four Clock Latency of Five Clock Latency of Six
B10	0 1[1][3]	WAIT Signal is Asserted Low WAIT Signal is Asserted High
B9	0 1[1]	Hold Data for One Clock Hold Data for Two Clocks
B8	0 1[1]	WAIT Asserted during Clock Cycle in which Data is Valid WAIT Asserted One Clock Cycle before Data is Valid
B7	1[1]	Linear Burst Sequence
B6	0 1[1]	Burst Starts and Data Output on Falling Clock Edge Burst Starts and Data Output on Rising Clock Edge
B5 - B4	00[1]	Reserved for Future Use
B3	0 1[1]	Wrap Burst Within Burst length set by B2 - B0 Don't Wrap Accesses Within Burst Length set by B2 - B0
B2 - B0	001 010 011 111[1]	Four-word Burst Eight-word Burst Sixteen-word Burst Continuous Burst

Notes: 1. Default State
2. Burst configuration setting of B13 - B11 = 010 (clock latency of two), B9 = 1 (hold data for two clock cycles) and B8 = 1 (WAIT asserted one clock cycle before data is valid) is not supported.
3. Data is not ready when WAIT is asserted.

Clock Latency versus Input Clock Frequency

Minimum Clock Latency (Minimum Number of Clocks Following Address Latch)	Input Clock Frequency
5, 6	≤ 66 MHz
4	≤ 61 MHz
2, 3	≤ 40 MHz

Figure 4. Output Configuration

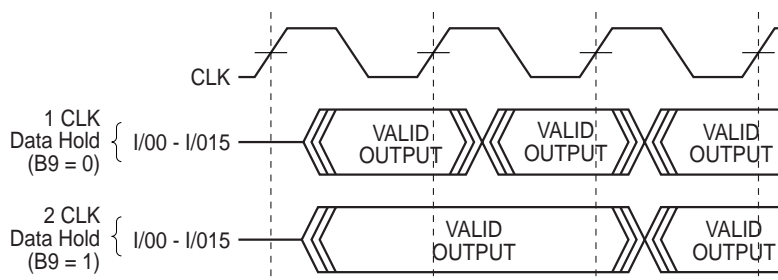**Table 5.** Sequence and Burst Length

Start Addr. (Decimal)	Wrap B3 = 0	Wrap B3 = 1	Burst Addressing Sequence (Decimal)			
			4-word Burst Length B2 – B0 = 001	8-word Burst Length B2 – B0 = 010	16-word Burst Length B2 – B0 = 011	Continuous Burst B2 – B0 = 111
			Linear	Linear	Linear	Linear
0	0		0-1-2-3	0-1-2-3-4-5-6-7	0-1-2...14-15	0-1-2-3-4-5-6...
1	0		1-2-3-0	1-2-3-4-5-6-7-0	1-2-3...14-15-0	1-2-3-4-5-6-7...
2	0		2-3-0-1	2-3-4-5-6-7-0-1	2-3-4...15-0-1	2-3-4-5-6-7-8...
3	0		3-0-1-2	3-4-5-6-7-0-1-2	3-4-5...15-0-1-2	3-4-5-6-7-8-9...
4	0			4-5-6-7-0-1-2-3	4-5-6...15-0-1-2-3	4-5-6-7-8-9-10...
5	0			5-6-7-0-1-2-3-4	5-6-7...15-0-1...4	5-6-7-8-9-10-11...
6	0			6-7-0-1-2-3-4-5	6-7-8...15-0-1...5	6-7-8-9-10-11-12...
7	0			7-0-1-2-3-4-5-6	7-8-9...15-0-1...6	7-8-9-10-11-12-13...
...	...	...	...	...	...	...
14	0				14-15-0-1...13	14-15-16-17-18-19-20
15	0				15-0-1-2-3...14	15-16-17-18-19-20-21
...	...	...	...	...	...	...
0		1	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2...14-15	0-1-2-3-4-5-6...
1		1	1-2-3-4	1-2-3-4-5-6-7-8	1-2-3...15-16	1-2-3-4-5-6-7...
2		1	2-3-4-5	2-3-4-5-6-7-8-9	2-3-4...16-17	2-3-4-5-6-7-8...
3		1	3-4-5-6	3-4-5-6-7-8-9-10	3-4-5...17-18	3-4-5-6-7-8-9...
4		1		4-5-6-7-8-9-10-11	4-5-6...18-19	4-5-6-7-8-9-10...
5		1		5-6-7-8-9-10-11-12	5-6-7...19-20	5-6-7-8-9-10-11...
6		1		6-7-8-9-10-11-12-13	6-7-8...20-21	6-7-8-9-10-11-12...
7		1		7-8-9-10-11-12-13-14	7-8-9...21-22	7-8-9-10-11-12-13...
...	...	...	...	...	...	...
14		1			14-15...28-29	14-15-16-17-18-19-20
15		1			15-16...29-30	15-16-17-18-19-20-21

Memory Organization – AT49SN/SV12804

Plane	Plane Size (Bits)	Sector	Size Words	x16 Address Range (A22 - A0)
1	4M	SA0	4K	00000 - 00FFF
		SA1	4K	01000 - 01FFF
		SA2	4K	02000 - 02FFF
		SA3	4K	03000 - 03FFF
		SA4	4K	04000 - 04FFF
		SA5	4K	05000 - 05FFF
		SA6	4K	06000 - 06FFF
		SA7	4K	07000 - 07FFF
		SA8	32K	08000 - 0FFFF
		SA9	32K	10000 - 17FFF
• • •		• • •	• • •	• • •
1		SA13	32K	30000 - 37FFF
		SA14	32K	38000 -3FFFF
2	4M	SA15	32K	40000 - 47FFF
• • •		• • •	• • •	• • •
2		SA22	32K	78000 - 7FFFF
3	4M	SA23	32K	80000 - 87FFF
• • •		• • •	• • •	• • •
3		SA30	32K	B8000 - BFFFF
4	4M	SA31	32K	C0000 - C7FFF
• • •		• • •	• • •	• • •
4		SA38	32K	F8000 - FFFFF
5	4M	SA39	32K	100000 - 107FFF
• • •		• • •	• • •	• • •
5		SA46	32K	138000 - 13FFFF
6	4M	SA47	32K	140000 - 147FFF
• • •		• • •	• • •	• • •
6		SA54	32K	178000 - 17FFFF
7	4M	SA55	32K	180000 - 187FFF
• • •		• • •	• • •	• • •
7		SA62	32K	1B8000 - 1BFFFF

Memory Organization – AT49SN/SV12804 (Continued)

Plane	Plane Size (Bits)	Sector	Size Words	x16 Address Range (A22 - A0)
8		SA63	32K	1C0000 - 1C7FFF
•	4M	•	•	•
•		•	•	•
•		•	•	•
8		SA70	32K	1F8000 - 1FFFFF
9		SA71	32K	200000-207FFF
•	4M	•	•	•
•		•	•	•
•		•	•	•
9		SA78	32K	238000 - 23FFFF
10		SA79	32K	240000 - 247FFF
•	4M	•	•	•
•		•	•	•
•		•	•	•
10		SA86	32K	278000 - 27FFFF
11		SA87	32K	280000 - 287FFF
•	4M	•	•	•
•		•	•	•
•		•	•	•
11		SA94	32K	2B8000 - 2BFFFF
12		SA95	32K	2C0000 - 2C7FFF
•	4M	•	•	•
•		•	•	•
•		•	•	•
12		SA102	32K	2F8000 - 2FFFFF
13		SA103	32K	300000 - 307FFF
•	4M	•	•	•
•		•	•	•
•		•	•	•
13		SA110	32K	338000 - 33FFFF
14		SA111	32K	340000 - 347FFF
•	4M	•	•	•
•		•	•	•
•		•	•	•
14		SA118	32K	378000 - 37FFFF
15		SA119	32K	380000 - 387FFF
•	4M	•	•	•
•		•	•	•
•		•	•	•
15		SA126	32K	3B8000 - 3BFFFF
16		SA127	32K	3C0000 - 3C7FFF
•	4M	•	•	•
•		•	•	•
•		•	•	•
16		SA134	32K	3F8000 - 3FFFFF

Plane	Plane Size (Bits)	Sector	Size Words	x16 Address Range (A22 - A0)
17		SA135	32K	400000 - 407FFF
•	4M	•	•	•
•		•	•	•
•		•	•	•
17		SA142	32K	438000 - 43FFFF
18		SA143	32K	440000 - 447FFF
•	4M	•	•	•
•		•	•	•
•		•	•	•
18		SA150	32K	478000 - 47FFFF
19		SA151	32K	480000 - 487FFF
•	4M	•	•	•
•		•	•	•
•		•	•	•
19		SA158	32K	4B8000 - 4BFFFF
20		SA159	32K	4C0000 - 4C7FFF
•	4M	•	•	•
•		•	•	•
•		•	•	•
20		SA166	32K	4F8000 - 4FFFFF
21		SA167	32K	500000 - 507FFF
•	4M	•	•	•
•		•	•	•
•		•	•	•
21		SA174	32K	538000 - 53FFFF
22		SA175	32K	540000 - 547FFF
•	4M	•	•	•
•		•	•	•
•		•	•	•
22		SA182	32K	578000 - 57FFFF
23		SA183	32K	580000 - 587FFF
•	4M	•	•	•
•		•	•	•
•		•	•	•
23		SA190	32K	5B8000 - 5BFFFF
24		SA191	32K	5C0000 - 5C7FFF
•	4M	•	•	•
•		•	•	•
•		•	•	•
24		SA198	32K	5F8000 - 5FFFFF
25		SA199	32K	600000 - 607FFF
•	4M	•	•	•
•		•	•	•
•		•	•	•
25		SA206	32K	638000 - 63FFFF

Memory Organization – AT49SN/SV12804 (Continued)

Plane	Plane Size (Bits)	Sector	Size Words	x16 Address Range (A22 - A0)
26		SA207	32K	640000 - 647FFF
•	4M	•	•	•
•		•	•	•
•		•	•	•
26		SA214	32K	678000 - 67FFFF
27		SA215	32K	680000 - 687FFF
•	4M	•	•	•
•		•	•	•
•		•	•	•
27		SA222	32K	6B8000 - 6BFFFF
28		SA223	32K	6C0000 - 6C7FFF
•	4M	•	•	•
•		•	•	•
•		•	•	•
28		SA230	32K	6F8000 - 6FFFFF
29		SA231	32K	700000 - 707FFF
•	4M	•	•	•
•		•	•	•
•		•	•	•
29		SA238	32K	738000 - 73FFFF
30		SA239	32K	740000 - 747FFF
•	4M	•	•	•
•		•	•	•
•		•	•	•
30		SA246	32K	778000 - 77FFFF
31		SA247	32K	780000 - 787FFF
•	4M	•	•	•
•		•	•	•
•		•	•	•
31		SA254	32K	7B8000 - 7BFFFF
32		SA255	32K	7C0000 - 7C7FFF
		SA256	32K	7C8000 - 7CFFFF
•		•	•	•
•		•	•	•
•		•	•	•
	4M	SA261	32K	7F0000 - 7F7FFF
		SA262	4K	7F8000 - 7F8FFF
		SA263	4K	7F9000 - 7F9FFF
		SA264	4K	7FA000 - 7FAFFF
32		SA265	4K	7FB000 - 7FBFFF
		SA266	4K	7FC000 - 7FCFFF
		SA267	4K	7FD000 - 7FDFFF
		SA268	4K	7FE000 - 7FEFFF
		SA269	4K	7FF000 - 7FFFFF

DC and AC Operating Range

		AT49SN/SV12804-70
Operating Temperature (Case)	Industrial	-40°C - 85°C
V_{CC} Power Supply		1.65V - 1.95V

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RESET}$	V_{PP}[4]	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	Ai	D_{OUT}
Burst Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	Ai	D_{OUT}
Program/Erase[3]	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IHPP}[5]	Ai	D_{IN}
Standby/Program Inhibit	V_{IH}	X[1]	X	V_{IH}	X	X	High Z
Program Inhibit	X	X	V_{IH}	V_{IH}	X		
	X	V_{IL}	X	V_{IH}	X		
	X	X	X	X	V_{ILPP}[6]		
Output Disable	X	V_{IH}	X	V_{IH}	X		High Z
Reset	X	X	X	V_{IL}	X	X	High Z
Product Identification							
Software				V_{IH}		A0 = V_{IL}, A1 - A22 = V_{IL}	Manufacturer Code[3]
						A0 = V_{IH}, A1 - A22 = V_{IL}	Device Code[3]

Notes: 1. X can be VIL or VIH.
2. Refer to AC programming waveforms.
3. Manufacturer Code: 001FH; Device Code: 00BBH
4. The VPP pin can be tied to V_{CC}. For faster program/erase operations, V_{PP} can be set to 12.0V ± 0.5V.
5. V_{IHPP} (min) = 0.9V.
6. V_{ILPP} (max) = 0.4V.

DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		1	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		1	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CCQ} - 0.3V to V_{CC}		20	µA
I_{CC}[1]	V_{CC} Active Current	f = 66 MHz; I_{OUT} = 0 mA		30	mA
I_{CCRE}	V_{CC} Read While Erase Current	f = 66 MHz; I_{OUT} = 0 mA		50	mA
I_{CCRW}	V_{CC} Read While Write Current	f = 66 MHz; I_{OUT} = 0 mA		50	mA
V_{IL}	Input Low Voltage			0.4	V
V_{IH}	Input High Voltage		V_{CCQ} - 0.2		V
V_{OL}	Output Low Voltage	I_{OL} = 100 µA I_{OL} = 2.1 mA		0.1 0.25	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA	V_{CCQ} - 0.1		V
		I_{OH} = -400 µA	1.4		

Note: 1. In the erase mode, I_{CC} is 30 mA.

Input Test Waveforms and Measurement Level

t_R, t_F < 5 ns
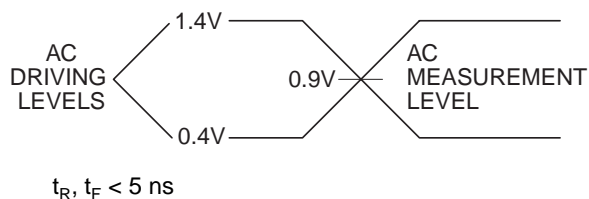
Output Test Load
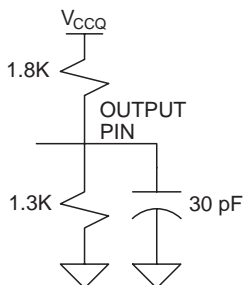
Pin Capacitance

f = 1 MHz, T = 25°C[1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

AC Asynchronous Read Timing Characteristics

Symbol	Parameter	Min	Max	Units
t_{ACC1}	Access, $\overline{AVD}$ To Data Valid		70	ns
t_{ACC2}	Access, Address to Data Valid		70	ns
t_{CE}	Access, $\overline{CE}$ to Data Valid		70	ns
t_{OE}	$\overline{OE}$ to Data Valid		20	ns
t_{AHAV}	Address Hold from $\overline{AVD}$	9		ns
t_{AVLP}	$\overline{AVD}$ Low Pulse Width	10		ns
t_{AVHP}	$\overline{AVD}$ High Pulse Width	10		ns
t_{AAV}	Address Valid to $\overline{AVD}$	7		ns
t_{DF}	$\overline{CE}$, $\overline{OE}$ High to Data Float		25	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, Whichever Occurred First			ns
t_{RO}	$\overline{RESET}$ to Output Delay		150	ns

$\overline{AVD}$ Pulsed Asynchronous Read Cycle Waveform[1][2]
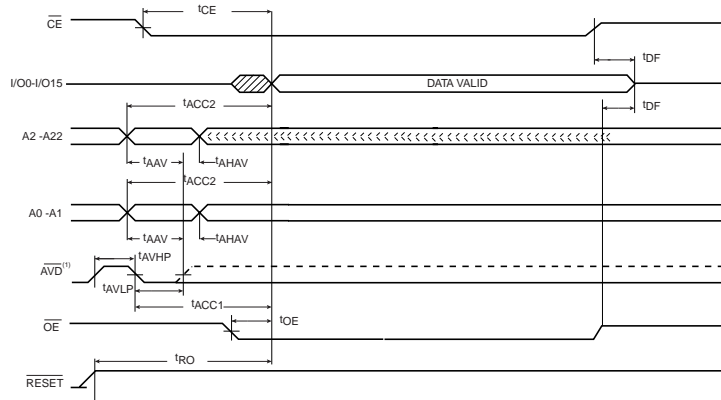
Notes: 1. After the high-to-low transition on $\overline{AVD}$, $\overline{AVD}$ may remain low as long as the address is stable.
2. CLK may be static high or static low.

Asynchronous Read Cycle Waveform[1][2][3][4]
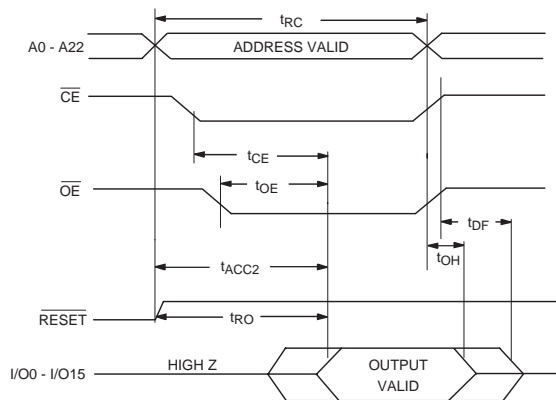
Notes: 1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first (CL = 5 pF).
4. $\overline{AVD}$ and CLK should be tied low.

AC Asynchronous Read Timing Characteristics

Symbol	Parameter	Min	Max	Units
t_{ACC1}	Access, $\overline{AVD}$ To Data Valid		70	ns
t_{ACC2}	Access, Address to Data Valid		70	ns
t_{CE}	Access, $\overline{CE}$ to Data Valid		70	ns
t_{OE}	$\overline{OE}$ to Data Valid		20	ns
t_{AHAV}	Address Hold from $\overline{AVD}$	9		ns
t_{AVLP}	$\overline{AVD}$ Low Pulse Width	10		ns
t_{AVHP}	$\overline{AVD}$ High Pulse Width	10		ns
t_{AAV}	Address Valid to $\overline{AVD}$	7		ns
t_{DF}	$\overline{CE}$, $\overline{OE}$ High to Data Float		25	ns
t_{RO}	$\overline{RESET}$ to Output Delay		150	ns
t_{PAA}	Page Address Access Time		20	ns

Page Read Cycle Waveform 1[1]
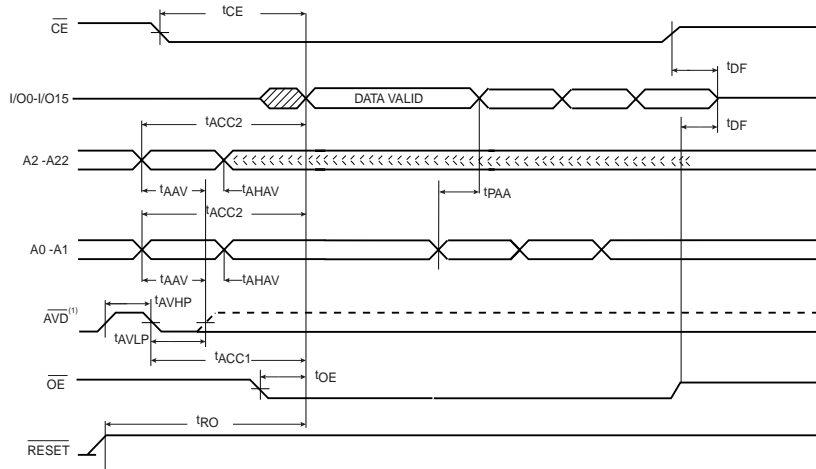
Note: 1. After the high-to-low transition on $\overline{AVD}$, $\overline{AVD}$ may remain low as long as the page address is stable.

Page Read Cycle Waveform 2[1]
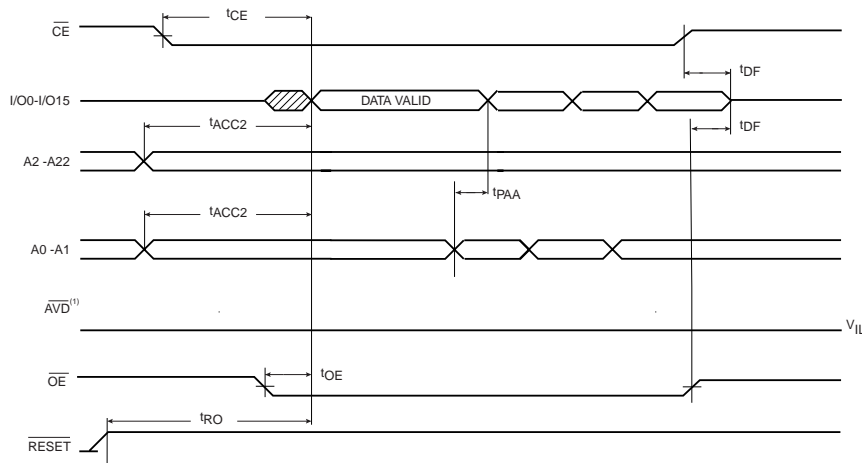
Note: 1. $\overline{AVD}$ may remain low as long as the page address is stable.

AC Burst Read Timing Characteristics

| Symbol	Parameter	Min	Max	Units
t_{CLK}	CLK Period	15		ns
t_{CKH}	CLK High Time	4		ns
t_{CKL}	CLK Low Time	4		ns
t_{CKRT}	CLK Rise Time		3.5	ns
t_{CKFT}	CLK Fall Time		3.5	ns
t_{ACK}	Address Valid to Clock	7		ns
t_{AVCK}	$\overline{AVD}$ Low to Clock	7		ns
t_{CECK}	$\overline{CE}$ Low to Clock	7		ns
t_{CKAV}	Clock to $\overline{AVD}$ High	3		ns
t_{QHCK}	Output Hold from Clock	3		ns
t_{AHCK}	Address Hold from Clock	8		ns
t_{CKRY}	Clock to WAIT Delay		13	ns
t_{CESAV}	$\overline{CE}$ Setup to $\overline{AVD}$	10		ns
t_{AAV}	Address Valid to $\overline{AVD}$	10		ns
t_{AHAV}	Address Hold From $\overline{AVD}$	9		ns
t_{CKQV}	CLK to Data Delay		13	ns
t_{CEQZ}	$\overline{CE}$ High to Output High-Z		10	ns

Burst Read Cycle Waveform
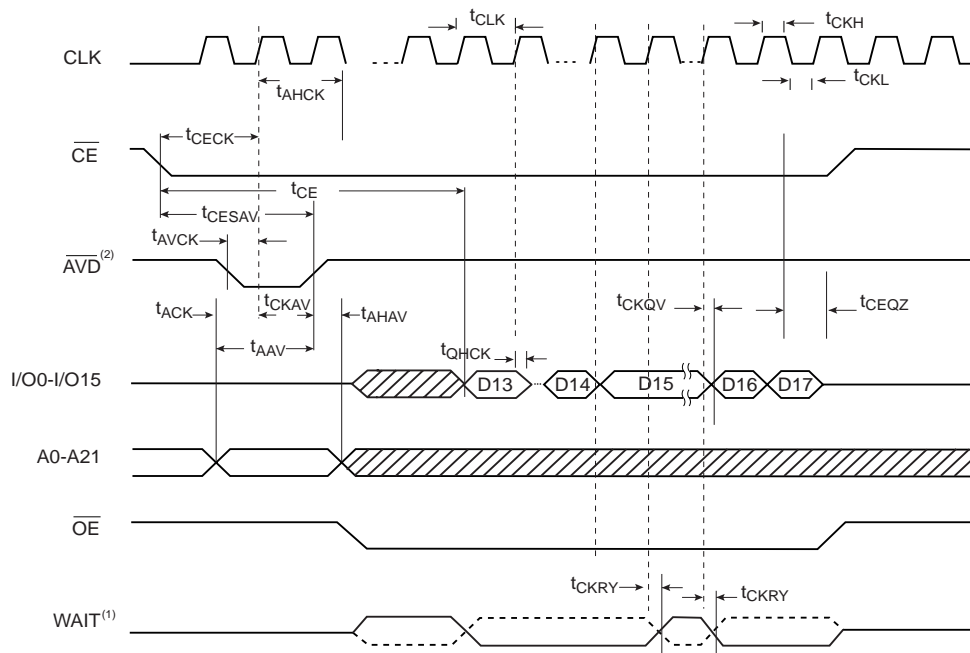
Notes: 1. The WAIT signal (dashed line) shown is for a burst configuration register setting of B10 and B8 = 0. The WAIT Signal (solid line) shown is for a burst configuration setting of B10 = 1 and B8 = 0.
2. After the high-to-low transition on $\overline{AVD}$, $\overline{AVD}$ may remain low.

AT49SN/SV12804 [Preliminary]

Burst Read Waveform (Clock Latency of 3)
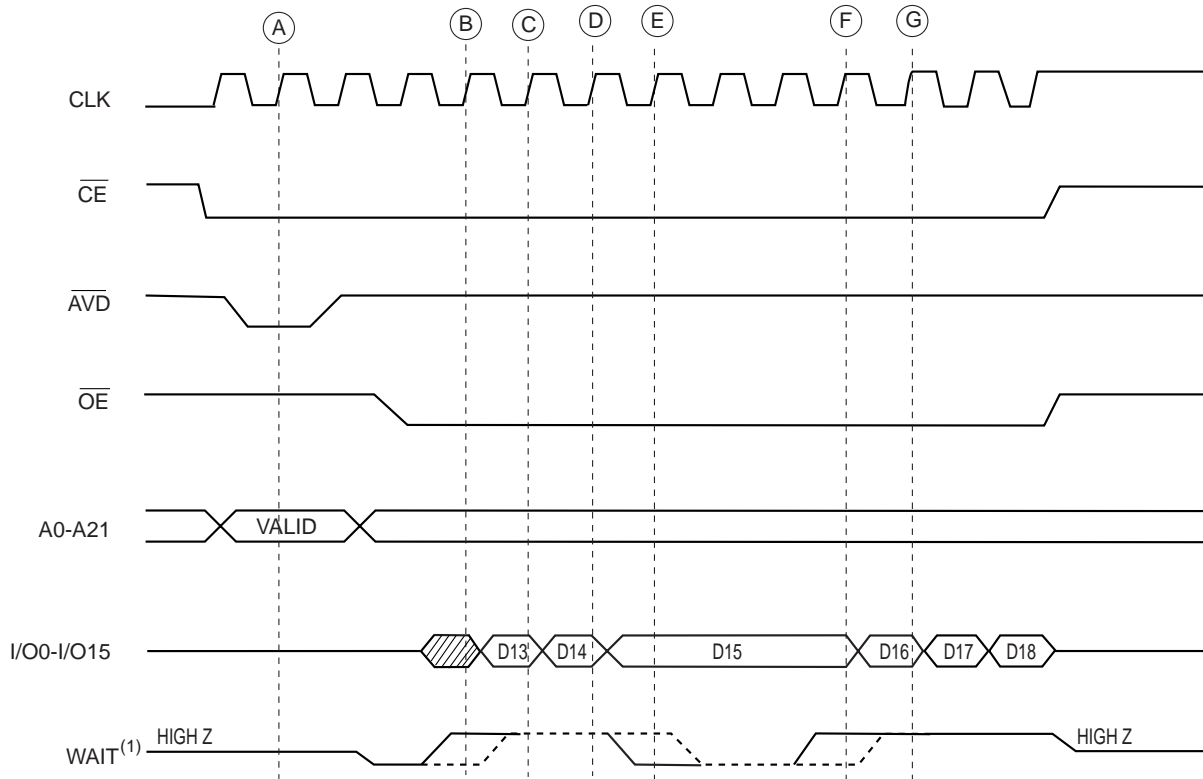
Note: 1. Dashed line reflects a B10 and B8 setting of 0 in the configuration register. Solid line reflects a B10 setting of 0 and B8 setting of 1 in the configuration register.

Hold Data for 2 Clock Cycles Read Waveform (Clock Latency of 3)
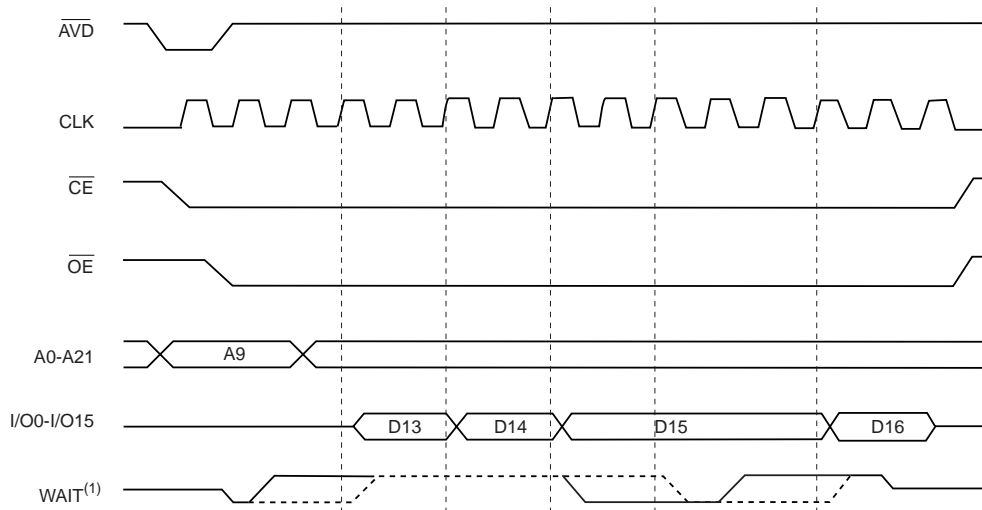
Note: 1. Dashed line reflects a burst configuration register setting of B10 and B8 = 0, B9 = 1.
Solid line reflects a burst configuration register setting of B10 = 0, B9 and B8 = 1

Four-word Burst Read Waveform (Clock Latency of 4)
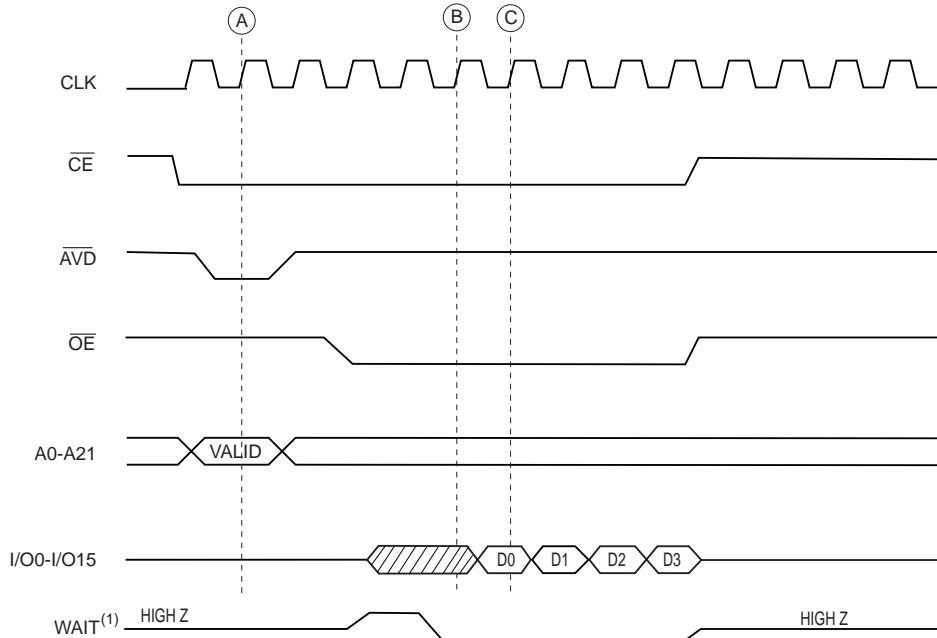
Note: 1. The WAIT signal shown is for a burst configuration register of B10 and B8 = 1.

Burst Suspend Waveform
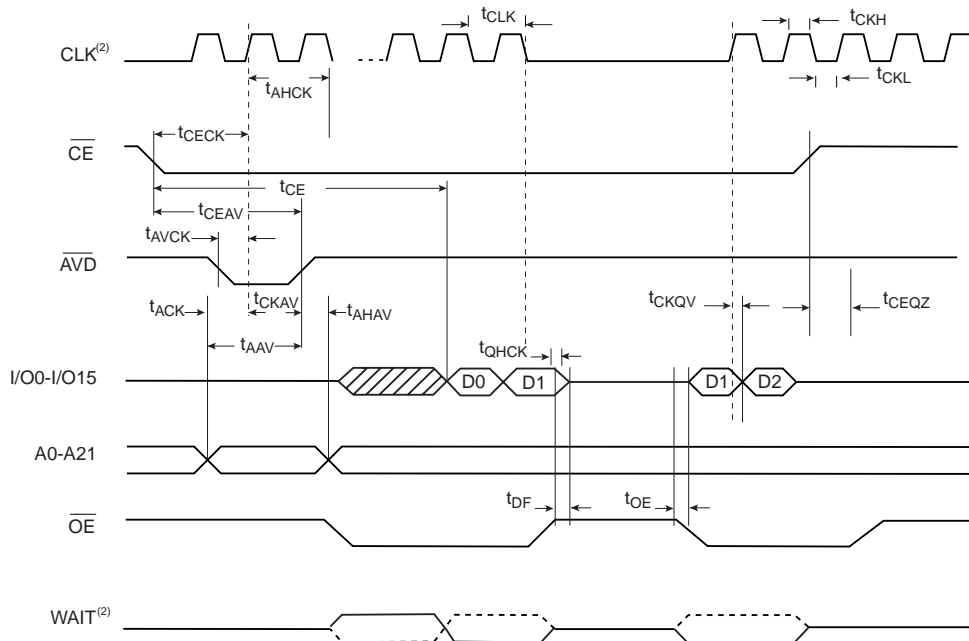
Notes: 1. The WAIT signal (dashed line) shown is for a burst configuration register setting of B10 and B8 = 0. The WAIT Signal (solid line) shown is for a burst configuration setting of B10 = 1 and B8 = 0.
2. During Burst Suspend, CLK signal can be held low or high.

AC Word Load Characteristics 1

Symbol	Parameter	Min	Max	Units
t_{AAV}	Address Valid to $\overline{AVD}$ High	10		ns
t_{AHAV}	Address Hold Time from $\overline{AVD}$ High	9		ns
t_{AVLP}	$\overline{AVD}$ Low Pulse Width	10		ns
t_{DS}	Data Setup Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{CESAV}	$\overline{CE}$ Setup to $\overline{AVD}$	10		ns
t_{WP}	$\overline{CE}$ or $\overline{WE}$ Low Pulse Width	35		ns
t_{WPH}	$\overline{CE}$ or $\overline{WE}$ High Pulse Width	25		ns
t_{WEAV}	$\overline{WE}$ High Time to $\overline{AVD}$ Low	25		ns
t_{CEAV}	$\overline{CE}$ High Time to $\overline{AVD}$ Low	25		ns

AC Word Load Waveforms 1

$\overline{WE}$ Controlled[1]
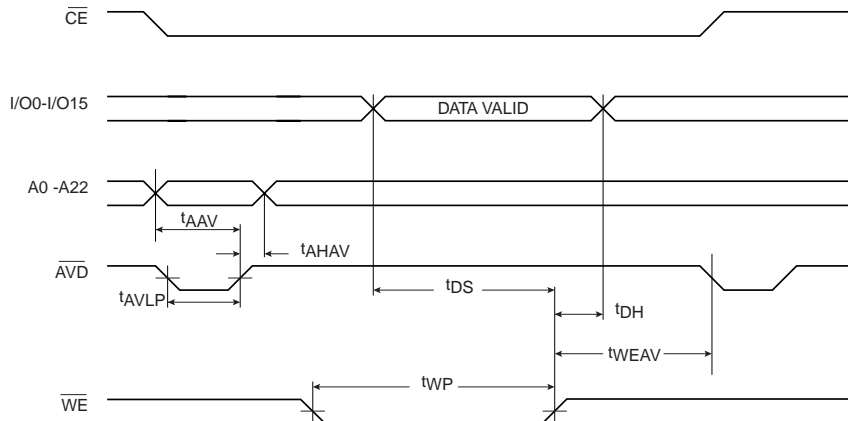
Note: 1. After the high-to-low transition on $\overline{AVD}$, $\overline{AVD}$ may remain low as long as the CLK input does not toggle.

$\overline{CE}$ Controlled[1]
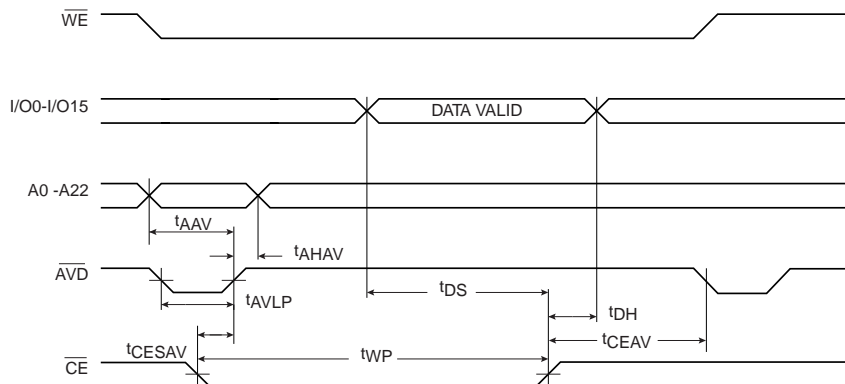
Note: 1. After the high-to-low transition on $\overline{AVD}$, $\overline{AVD}$ may remain low as long as the CLK input does not toggle.

AC Word Load Characteristics 2

Symbol	Parameter	Min	Max	Units
t_{AS}	Address Setup Time to $\overline{WE}$ and $\overline{CE}$ High	50		ns
t_{AH}	Address Hold Time	0		ns
t_{DS}	Data Setup Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	$\overline{CE}$ or $\overline{WE}$ Low Pulse Width	35		ns
t_{WPH}	$\overline{CE}$ or $\overline{WE}$ High Pulse Width	25		ns

AC Word Load Waveforms 2

$\overline{WE}$ Controlled[1]
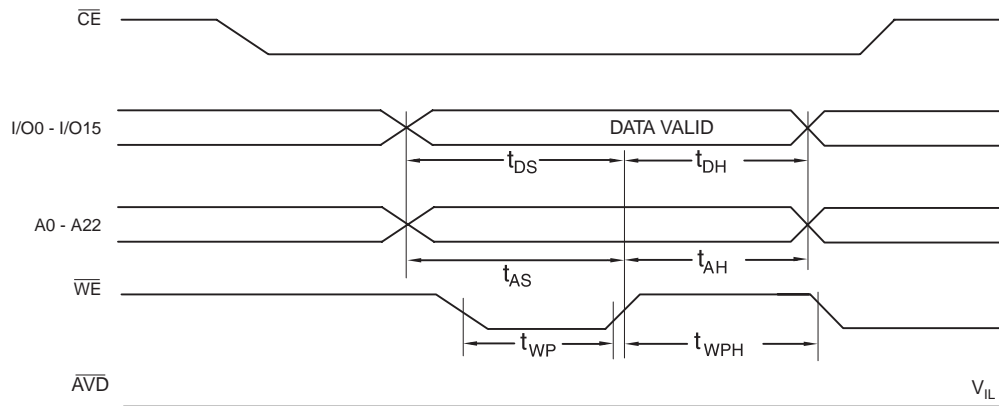
Note: 1. The CLK input should not toggle.

$\overline{CE}$ Controlled[1]
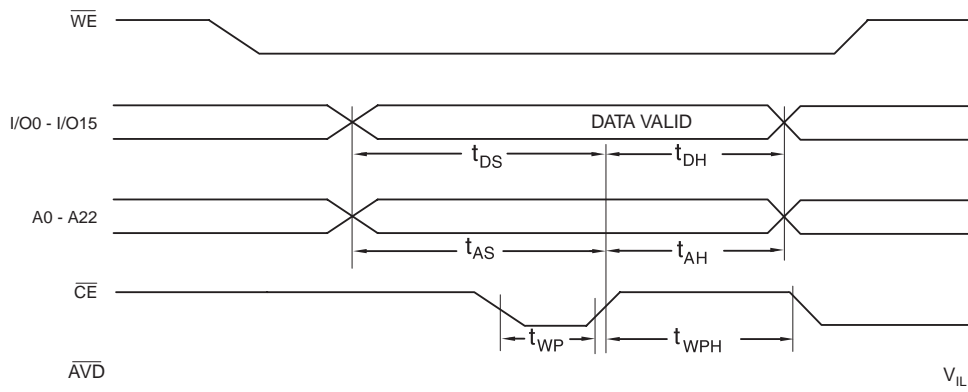
Note: 1. The CLK input should not toggle.

Program Cycle Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{BP}	Word Programming Time		22		µs
t_{SEC1}	Sector Erase Cycle Time (4K word sectors)		200		ms
t_{SEC2}	Sector Erase Cycle Time (32K word sectors)		700		ms
t_{ES}	Erase Suspend Time			15	µs
t_{PS}	Program Suspend Time			10	µs
t_{ERES}	Delay between Erase Resume and Erase Suspend	500			µs

Program Cycle Waveforms
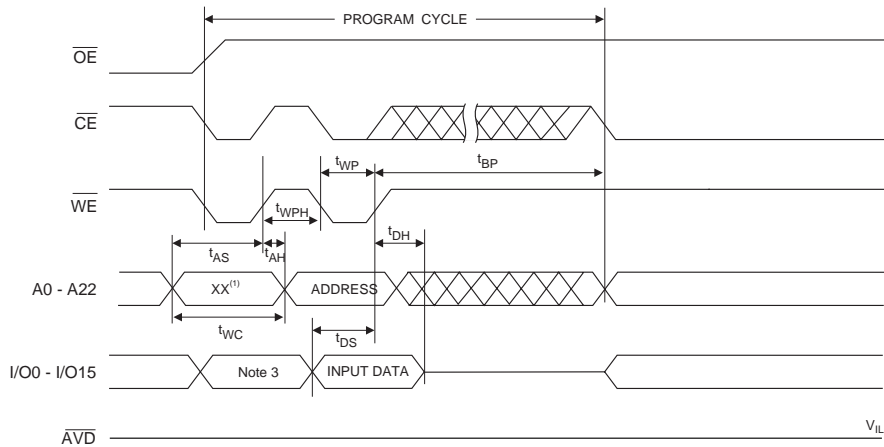
Sector, Plane or Chip Erase Cycle Waveforms
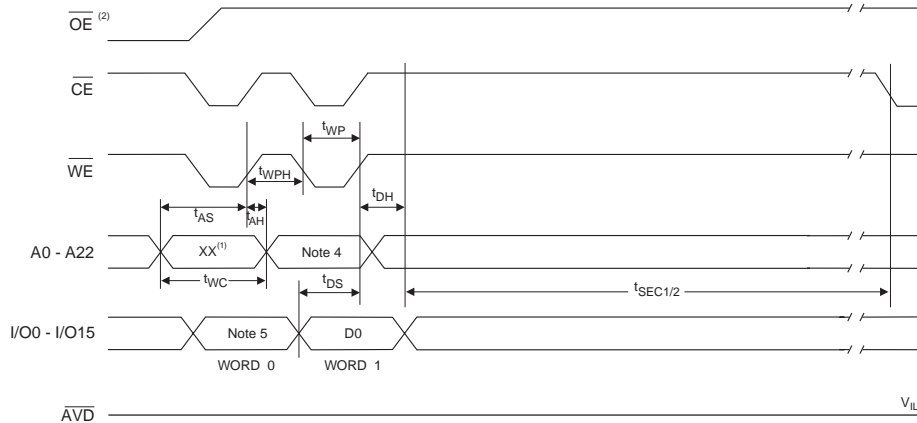
Notes: 1. Any address can be used to load data.
   2. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.
   3. The data can be 40H or 10H.
   4. For chip erase, any address can be used. For plane erase or sector erase, the address depends on what plane or sector is to be erased.
   5. For chip erase, the data should be 21H, for plane erase, the data should be 22H, and for sector erase, the data should be 20H.

Table 6. Common Flash Interface Definition for AT49SN/SV12804

Address	AT49SN/SV12804	Comments
10h	0051h	"Q"
11h	0052h	"R"
12h	0059h	"Y"
13h	0003h	
14h	0000h	
15h	0041h	
16h	0000h	
17h	0000h	
18h	0000h	
19h	0000h	
1Ah	0000h	
1Bh	0016h	VCC min write/erase
1Ch	0019h	VCC max write/erase
1Dh	00B5h	VPP min voltage
1Eh	00C5h	VPP max voltage
1Fh	0004h	Typ word write – 16 µs
20h	0000h	
21h	0009h	Typ block erase – 500 ms
22h	0011h	Typ chip erase – 131,000 ms
23h	0004h	Max word write/typ time
24h	0000h	n/a
25h	0003h	Max block erase/typ block erase
26h	0003h	Max chip erase/ typ chip erase
27h	0018h	Device size
28h	0001h	x16 device
29h	0000h	x16 device
2Ah	0000h	Multiple byte write not supported
2Bh	0000h	Multiple byte write not supported
2Ch	0003h	3 regions, x = 3
2Dh	00FDh	64K bytes, Y = 253
2Eh	0000h	64K bytes, Y = 253
2Fh	0000h	64K bytes, Z = 256
30h	0001h	64K bytes, Z = 256
31h	0007h	8K bytes, Y = 7
32h	0000h	8K bytes, Y = 7
33h	0020h	8K bytes, Z = 32
34h	0000h	8K bytes, Z = 32
35h	0007h	8K bytes, Y = 7
36h	0000h	8K bytes, Y = 7
37h	0020h	8K bytes, Z = 32
38h	0000h	8K bytes, Z = 32

Table 6. Common Flash Interface Definition for AT49SN/SV12804 (Continued)

| Address	AT49SN/SV12804	Comments
		VENDOR SPECIFIC EXTENDED QUERY
41h	0050h	"P"
42h	0052h	"R"
43h	0049h	"I"
44h	0031h	Major version number, ASCII
45h	0030h	Minor version number, ASCII
46h	00BFh	Bit 0 – chip erase supported, 0 – no, 1 – yes
		Bit 1 – erase suspend supported, 0 – no, 1 – yes
		Bit 2 – program suspend supported, 0 – no, 1 – yes
		Bit 3 – simultaneous operations supported, 0 – no, 1 – yes
		Bit 4 – burst mode read supported, 0 – no, 1 – yes
		Bit 5 – page mode read supported, 0 – no, 1 – yes
		Bit 6 – queued erase supported, 0 – no, 1 – yes
		Bit 7 – protection bits supported, 0 – no, 1 – yes
47h	0002h	Bit 8 – top ("0"), bottom ("1"), or both top and bottom ("2") boot block device Undefined bits are "0"
48h	000Fh	Bit 0 – 4 word linear burst with wrap around, 0 – no, 1 – yes Bit 1 – 8 word linear burst with wrap around, 0 – no, 1 – yes Bit 2 – 16 word linear burst with wrap around, 0 – no, 1 – yes Bit 3 – continuos burst, 0 – no, 1 – yes Undefined bits are "0"
49h	0003h	Bit 0 – 4 word page, 0 – no, 1 – yes Bit 1 – 8 word page, 0 – no, 1 – yes Undefined bits are "0"
4Ah	0080h	Location of protection register lock byte, the section's first byte
4Bh	0003h	# of bytes in the factory prog section of prot register – 2*n
4Ch	0007h	# of bytes in the user prog section of prot register – 2*n – 132
4Dh	0020h	Number of planes – 32 planes

AT49SN/SV12804 Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	30	0.01	AT49SN12804-70CI	56C3	Industrial (-40° to 85°C)
70	30	0.01	AT49SV12804-70TI	56T	Industrial (-40° to 85°C)

Package Type	
56C3	56-ball, Plastic Chip-size Ball Grid Array Package (CBGA)
56T	56-lead, Plastic Thin Small Outline Package (TSOP)

Packaging Information

56C3 – CBGA

Side View

Top View

Bottom View

1.375 mm Ref

2.75 mm Ref
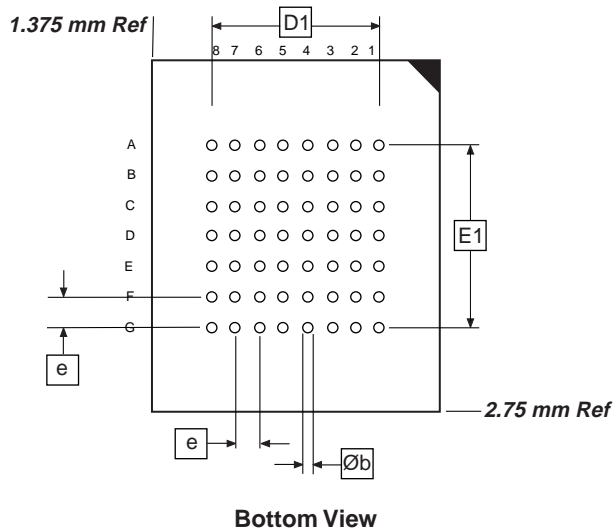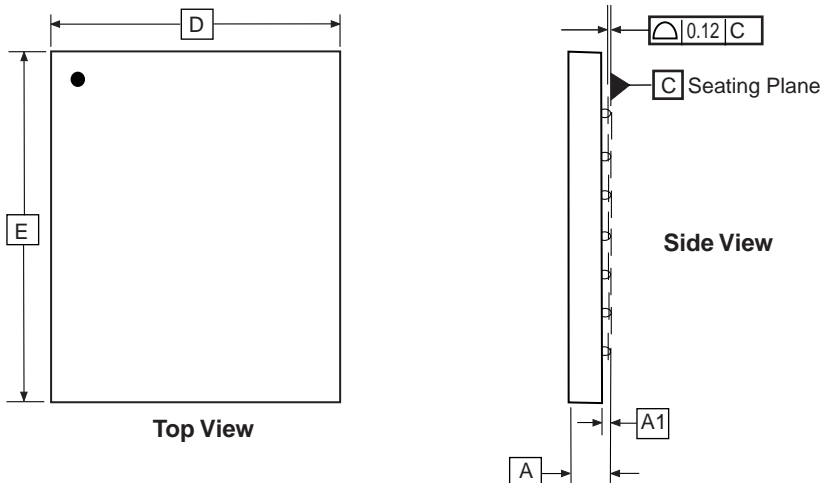
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.00	
A1	0.21	–	–	
D	7.90	8.00	8.10	
D1	5.25 TYP			
E	9.90	10.00	10.10	
E1	4.50 TYP			
e	0.75 TYP			
Øb	0.35 TYP			

1/9/04

	2325 Orchard Parkway San Jose, CA 95131	**TITLE** **56C3**, 56-ball (8 x 7 Array), 8 x 10 x 1.0 mm Body, 0.75 mm Ball Pitch Ceramic Ball Grid Array Package (CBGA)	**DRAWING NO.** 56C3	**REV.** A

56T – TSOP

PIN 1

Pin 1 Identifier

D1 D

e

b

E

A2 A

A1

0º ~ 8º

c

L

L1

SEATING PLANE

GAGE PLANE

Notes: 1. This package conforms to JEDEC reference MO-142, Variation EC.
2. Dimensions D1 and E do not include mold protrusion. Allowable
protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
3. Lead coplanarity is 0.10 mm maximum.
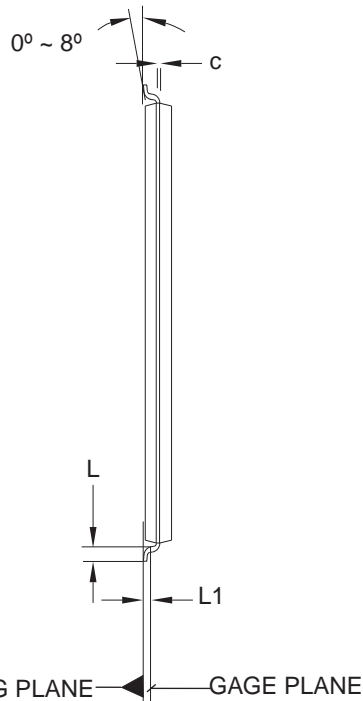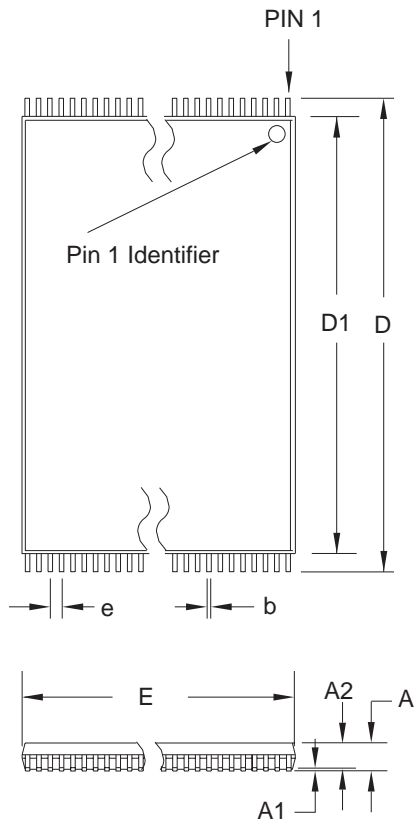
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	19.80	20.00	20.20	
D1	18.20	18.40	18.60	Note 2
E	13.80	14.00	14.20	Note 2
L	0.50	0.60	0.70	
L1	0.25 BASIC			
b	0.10	0.15	0.20	
c	0.10	–	0.21	
e	0.50 BASIC			

10/23/03

		TITLE	DRAWING NO.	REV.
	2325 Orchard Parkway San Jose, CA 95131	**56T**, 56-lead (14 x 20 mm Package) Plastic Thin Small Outline Package, Type I (TSOP)	56T	C

AT49SN/SV12804 [Preliminary]

3314A–FLASH–4/04

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