Integrated Device Technology, Inc.

4K x 36 BiCMOS SYNCHRONOUS DUAL-PORT STATIC RAM MODULE

IDT7M1024

FEATURES:

- High-density 4K x 36 Synchronous Dual-Port SRAM module
- Architecture based on Dual-Port RAM cells
  - — Allows full simultaneous access from both ports
- Synchronous operation
  - — 4ns set-up to clock, 1ns hold on all control, data, and address inputs
  - — Data input, address, and control registers
  - — Fast 20ns clock to data out
  - — Self-timed write allows fast write cycle
- Clock enable feature
- Single 5V (±10%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL-compatible

DESCRIPTION:

The IDT7M1024 is a 4K x 36 bit high-speed synchronous Dual-Port Static RAM module constructed on a co-fired ceramic substrate using four IDT7099 (4K x 9) Dual-Port RAMs. The IDT7M1024 module is designed to be used as a stand-alone 36-bit Dual-Port Static RAM.

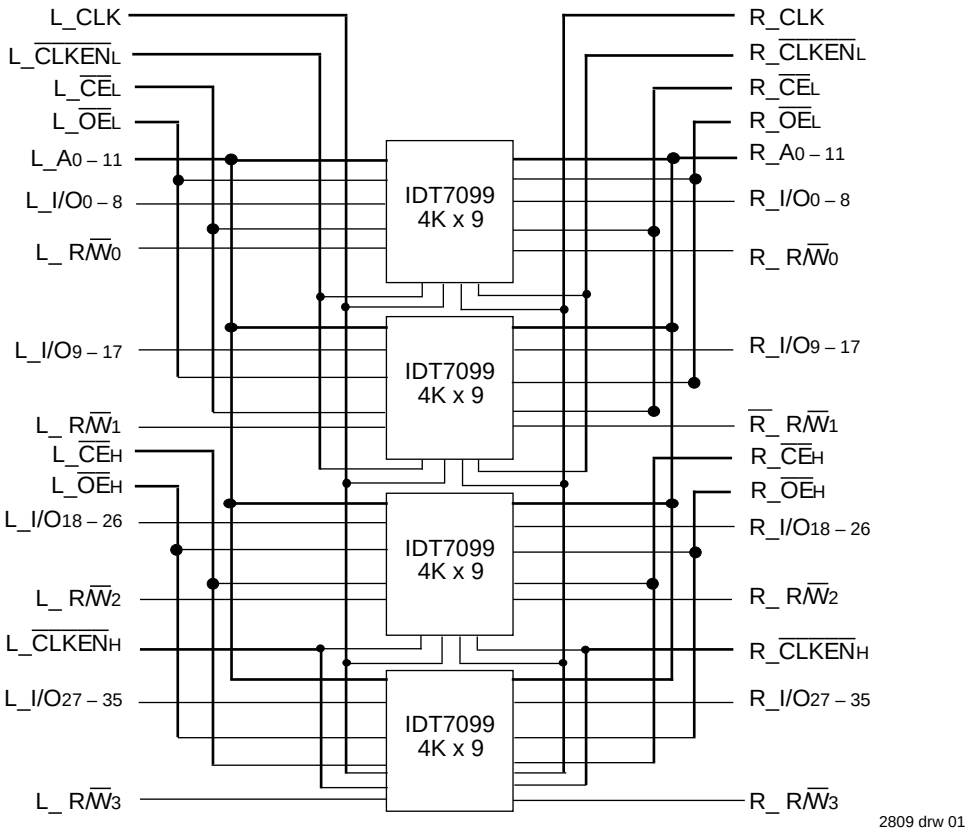
The IDT7M1024 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide very short set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal. An asynchronous output enable is provided to ease asynchronous bus interfacing.

The internal write pulse width is independent of the HIGH and LOW periods of the clock. This allows the shortest possible realized cycle times. Clock enable inputs are provided to stall the operation of the address and data input registers without introducing clock skew for very fast interleaved memory applications.

The data inputs are gated to control on-chip noise in bussed applications. The user must guarantee that the R/$\overline{W}$ pins are LOW for at least one clock cycle before any write is attempted. A HIGH on the $\overline{CE}$ input for one clock cycle will power down the internal circuitry to reduce static power consumption.

The IDT7M1024 module is packaged in a 142-lead ceramic

FUNCTIONAL BLOCK DIAGRAM



2809 drw 01

PGA (Pin Grid Array).

All IDT military modules are constructed with semiconductor components manufactured in compliance with the latest revision of MIL-STD-883, Class B making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	GND	L_I/O3	L_I/O2	GND	L_I/O1	L_I/O0	GND	R_I/O0	R_I/O1	GND	R_I/O2	R_I/O3	GND
B	L_I/O4	L_I/O5	L_I/O6	L_A2	L_A1	L_A0	L_CLK	R_A0	R_A1	R_A2	R_I/O6	R_I/O5	R_I/O4
C	L_I/O8	VCC	L_I/O7	GND	L_$\overline{\text{CLKEN}}$ L	L_$\overline{\text{CLKEN}}$ H	R_CLK	R_$\overline{\text{CLKEN}}$ H	R_$\overline{\text{CLKEN}}$ L	GND	R_I/O7	VCC	R_I/O8
D	L_I/O9	L_I/O10	L_I/O11	L_A3	GND			GND	R_A3	R_A4	R_I/O11	R_I/O10	R_I/O9
E	L_I/O12	L_$\overline{\text{CE}}$ L	L_$\overline{\text{CE}}$ H	L_A4						R_A5	R_$\overline{\text{CE}}$ H	R_$\overline{\text{CE}}$ L	R_I/O12
F	L_I/O13	L_$\overline{\text{OE}}$ L	L_$\overline{\text{OE}}$ H	L_A5						R_A6	R_$\overline{\text{OE}}$ H	R_$\overline{\text{OE}}$ L	R_I/O13
G	GND	L_R/$\overline{\text{W}}$0	L_R/$\overline{\text{W}}$1	GND						GND	R_R/$\overline{\text{W}}$1	R_R/$\overline{\text{W}}$0	GND
H	L_I/O14	L_R/$\overline{\text{W}}$2	L_R/$\overline{\text{W}}$3	L_A6						R_A7	R_R/$\overline{\text{W}}$3	R_R/$\overline{\text{W}}$2	R_I/O14
J	L_I/O15	L_I/O16	L_I/O17	L_A7						R_A8	R_I/O17	R_I/O16	R_I/O15
K	L_I/O20	L_I/O19	L_I/O18	GND	L_A10	L_A11	GND	R_A11	R_A10	GND	R_I/O18	R_I/O19	R_I/O20
L	L_I/O21	VCC	L_I/O22	L_A8	L_A9	L_I/O31	R_I/O35	R_I/O34	R_I/O30	R_A9	R_I/O22	VCC	R_I/O21
M	L_I/O23	L_I/O24	L_I/O25	L_I/O29	L_I/O30	L_I/O32	L_I/O35	R_I/O33	R_I/O31	R_I/O29	R_I/O25	R_I/O24	R_I/O23
N	GND	L_I/O26	L_I/O27	L_I/O28	GND	L_I/O33	L_I/O34	R_I/O32	GND	R_I/O28	R_I/O27	R_I/O26	GND

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PIN NAMES

Left Port	Right Port	Names
L_R/$\overline{\text{W}}$ 0-3	R_R/$\overline{\text{W}}$ 0-3	Byte Read/Write Enables
L_$\overline{\text{OE}}$ L, H	R_$\overline{\text{OE}}$ L, H	Word Output Enables
L_$\overline{\text{CE}}$ L, H	R_$\overline{\text{CE}}$ L, H	Word Chip Enables
L_$\overline{\text{CLKEN}}$ L, H	R_$\overline{\text{CLKEN}}$ L, H	Word Clock Enables
L_CLK	R_CLK	Clock Inputs
L_A 0-11	R_A 0-11	Address Inputs
L_I/O 0-35	R_I/O 0-35	Data Input/Outputs
V_{CC}		Power
GND		Ground

2809 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTES: 2809 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Inputs and Vcc terminals only.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	VCC
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2809 tbl 03

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input HIGH Voltage	2.2	—	6.0	V
V_{IL}	Input LOW Voltage	–0.5(1)	—	0.8	V

NOTE: 2809 tbl 04

1. V_{IL} = -3.0V for pulse width less than 20ns.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter(1)	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	50	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	15	pF

2809 tbl 05

TRUTH TABLES

TRUTH TABLE I: READ/WRITE CONTROL (1)

Inputs				Outputs	
Synchronous			Asynchronous		
Clk	$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	I/O_{0-35}	Mode
↑	h	h	X	High-Z	Deselected, Power Down, Data I/O Disabled
↑	h	l	X	$DATA_{IN}$	Deselected, Power Down, Data Input Enabled
↑	l	l	X	$DATA_{IN}$	Write
↑	l	h	L	$DATA_{OUT}$	Read
↑	l	h	H	High-Z	Data I/O Disabled

2809 tbl 06

TRUTH TABLE II: CLOCK ENABLE FUNCTION TABLE (1)

	Inputs		Register Inputs		Register Outputs	
Operating Mode	Clk	$\overline{CLKEN}$	ADDR	$DATA_{IN}$	ADDR	$DATA_{OUT}$
Load “1”	↑	l	h	h	H	H
Load “0”	↑	l	l	l	L	L
Hold (do nothing)	↑	h	X	X	N/C	N/C
	X	H	X	X	N/C	N/C

NOTE: 2809 tbl 07

1. H = HIGH voltage level steady state, h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition, L =LOW voltage level steady state l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition, X = Don't care, N/C = No change

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	IDT7M1024 Min.	IDT7M1024 Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	40	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = VIH, V_{OUT} = 0V to V_{CC}	—	10	µA
V_{OL}	Output LOW Voltage	I_{OL} = 4mA	—	0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} = –4mA	2.4	—	V

2809 tbl 08

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Version	IDT7M1024SxxG, IDT7M1024SxxGB –20 Typ.	–20 Max.	–25 Typ.	–25 Max.	–30 Typ.	–30 Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE} \le V_{IL}$ Outputs Open f = f_{MAX}(1)	Mil.	—	—	—	1480	—	1440	mA
			Com'l.	—	1440	—	1360	—	—	
I_{SB1}	Standby Current (Both Ports—TTL Level Inputs)	L_$\overline{CE}$ and R_$\overline{CE}$ ≥ V_{IH} f = f_{MAX}(1)	Mil.	—	—	—	680	—	560	mA
			Com'l.	—	720	—	640	—	—	
I_{SB2}	Standby Current (One Port—TTL Level Inputs)	L_$\overline{CE}$ or R_$\overline{CE}$ ≥ V_{IH} Active Port Outputs Open, f = f_{MAX}(1)	Mil.	—	—	—	1080	—	1000	mA
			Com'l.	—	1080	—	1000	—	—	
I_{SB3}	Full Standby Current (Both Ports—CMOS Level Inputs)	Both Ports R_$\overline{CE}$ and L_$\overline{CE}$ ≥ V_{CC} – 0.2V V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0(2)	Mil.	—	—	—	80	—	80	mA
			Com'l.	—	80	—	80	—	—	
I_{SB4}	Full Standby Current (One Port—CMOS Level Inputs)	One Port L_$\overline{CE}$ or R_$\overline{CE}$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs Open, f = f_{MAX}(1)	Mil.	—	—	—	1040	—	960	mA
			Com'l.	—	1040	—	960	—	—	

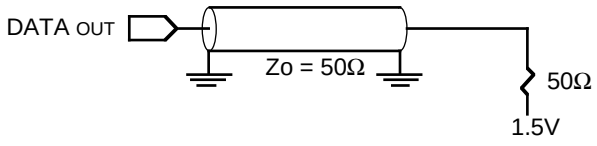
NOTES: 2809 tbl 09

1. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of 1/tCLK, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
2. f = 0 means no address, clock, or control lines change. Applies only to inputs at CMOS level standby.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 and 3

2909 tbl 10



2809 drw 03

Figure 1. Output Load

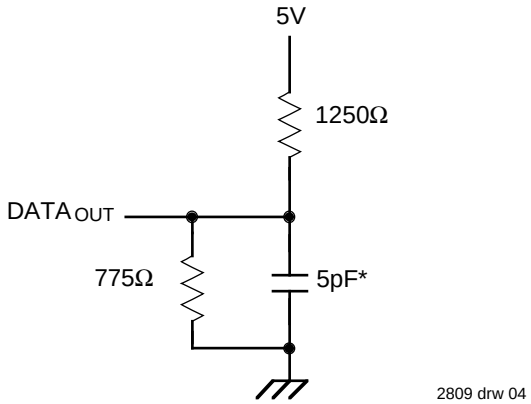


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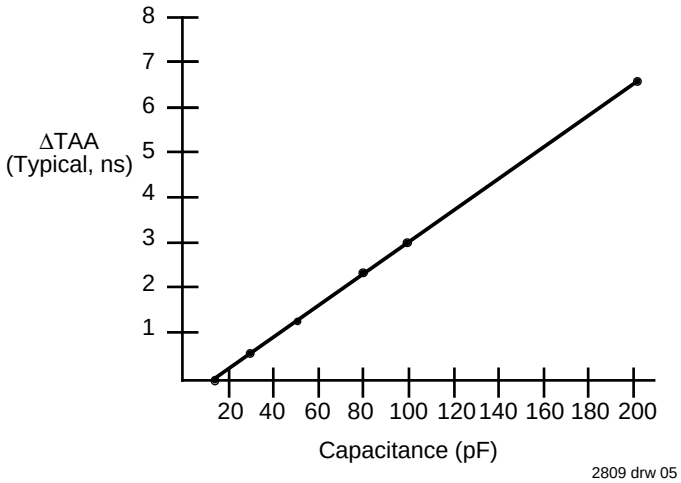
Figure 2. Output Load (for t_{CLZ}, t_{CHZ}, t_{OLZ}, and t_{OHZ})

*Including scope and jig.



2809 drw 05

Figure 3. Lumped Capacitive Load, Typical Derating

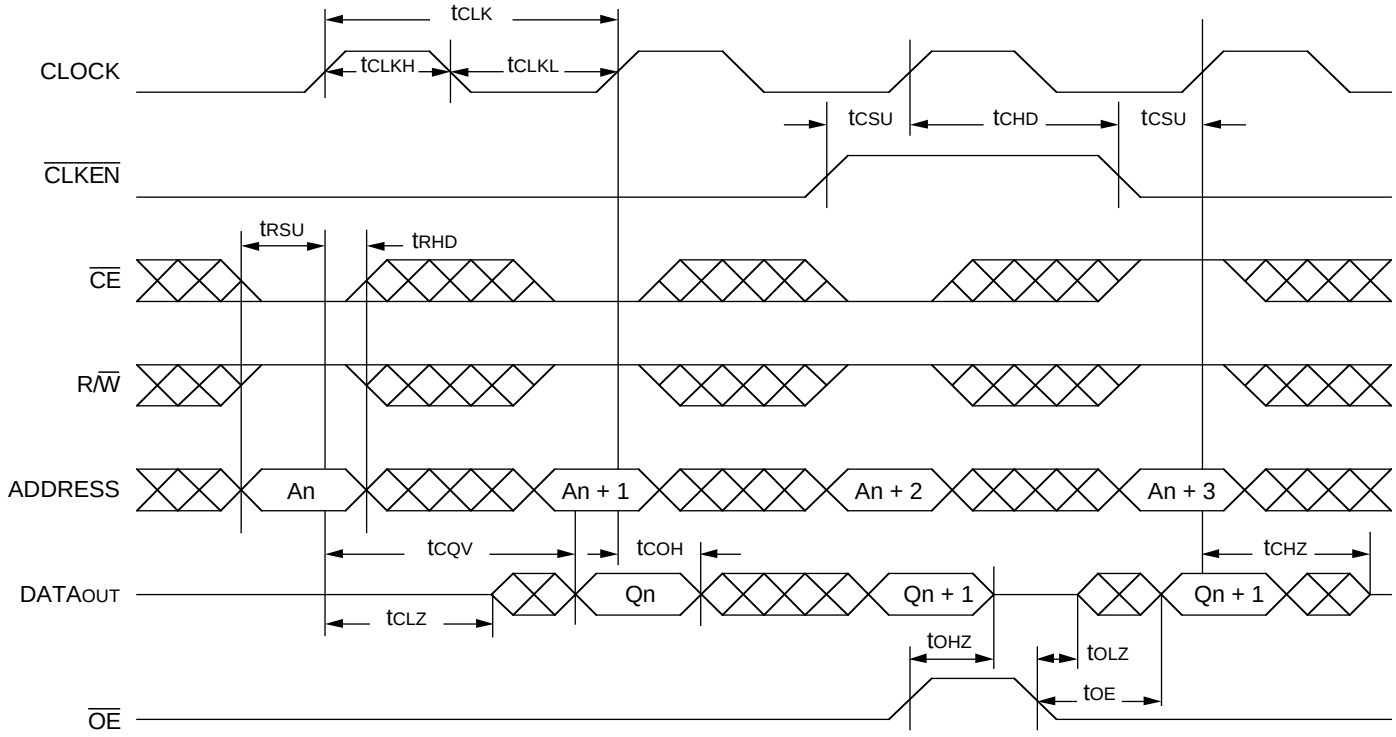
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE RANGE — (READ AND WRITE CYCLE TIMING)

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = –55°C to +125°C)

		7M1024SxxG, 7M1024SxxGB						
		–20		–25		–30		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{CLK}	Clock Cycle Time	20	—	25	—	30	—	ns
t_{CLKH}	Clock HIGH Time	8	—	10	—	12	—	ns
t_{CLKL}	Clock LOW Time	8	—	10	—	12	—	ns
t_{CQV}	Clock HIGH to Output Valid	—	20	—	25	—	30	ns
t_{RSU}	Registered Signal Set-up Time	5	—	6	—	7	—	ns
t_{RHD}	Registered Signal Hold Time	2	—	2	—	2	—	ns
t_{COH}	Data Output Hold After Clock HIGH	3	—	3	—	3	—	ns
t_{CLZ}	Clock HIGH to Output Low-Z	2	—	2	—	2	—	ns
t_{CHZ}	Clock HIGH to Output High-Z	2	9	2	12	2	15	ns
t_{OE}	Output Enable to Output Valid	—	10	—	12	—	15	ns
t_{OLZ}	Output Enable to Output Low-Z	0	—	0	—	0	—	ns
t_{OHZ}	Output Disable to Output High-Z	—	9	—	11	—	14	ns
t_{CSU}	Clock Enable, Disable Set-up Time	5	—	6	—	7	—	ns
t_{CHD}	Clock Enable, Disable Hold Time	3	—	3	—	3	—	ns
Port-to-Port Delay								
t_{CWDD}	Write Port Clock HIGH to Read Data Delay	—	35	—	45	—	55	ns

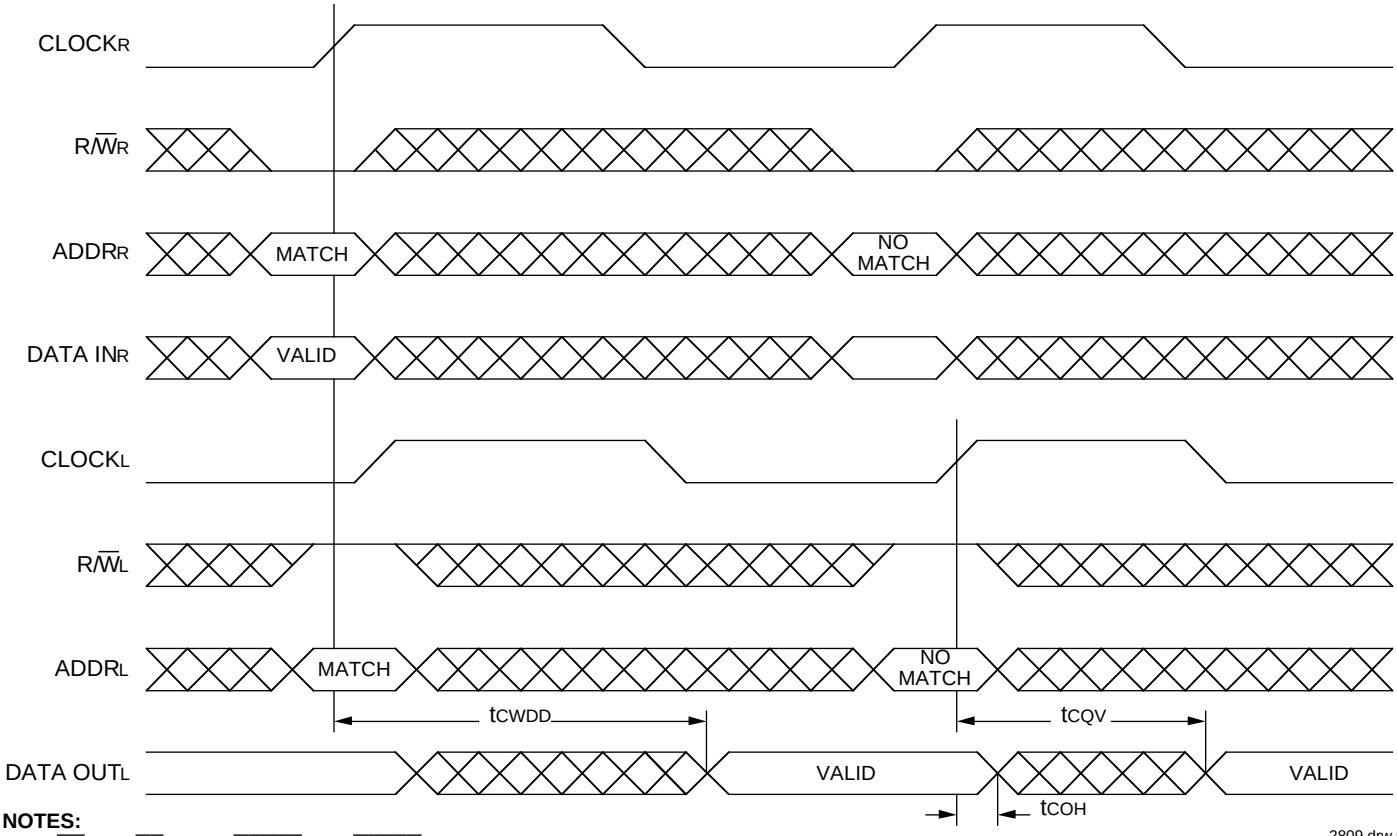
2809 tbl 11

TIMING WAVEFORM OF READ CYCLE, EITHER SIDE(1,2)



2809 drw 06

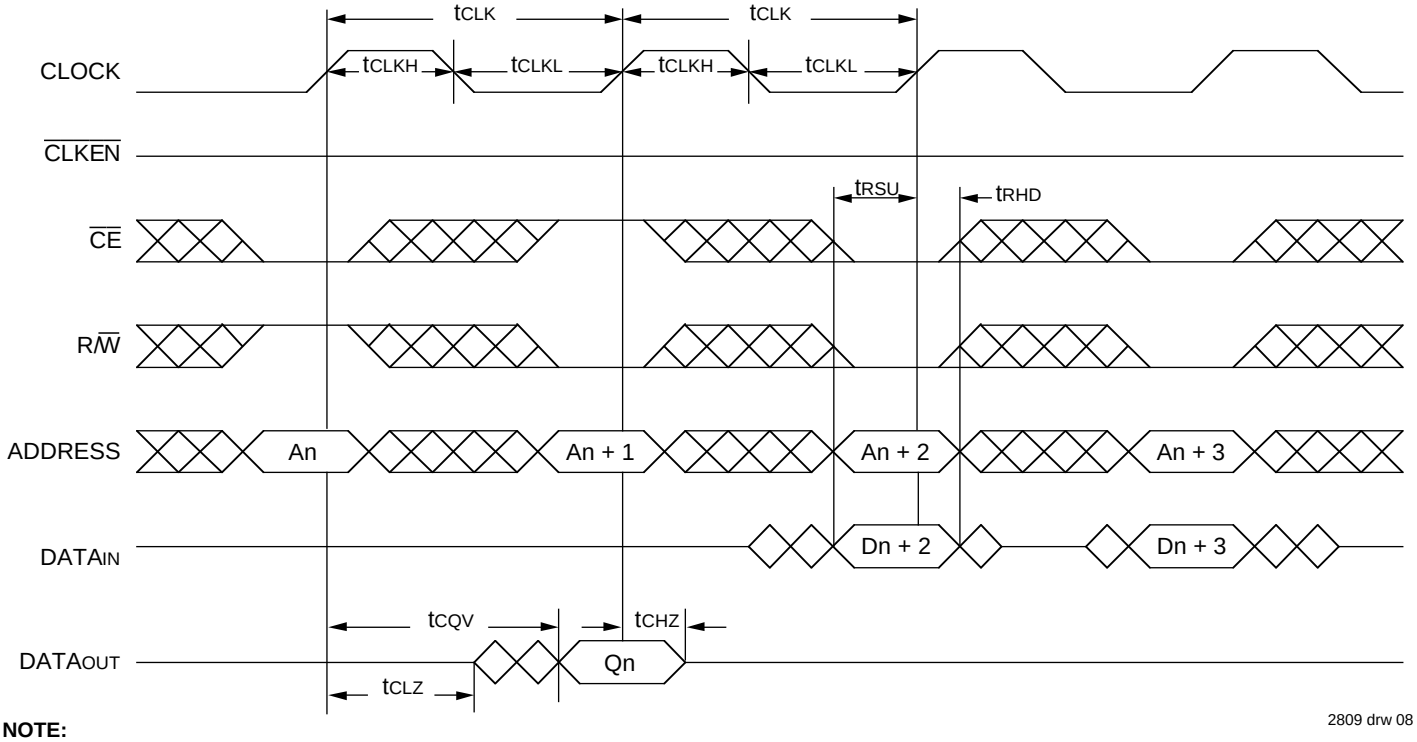
TIMING WAVEFORM OF READ CYCLE WITH PORT-TO-PORT DELAY



2809 drw 07

NOTES:
1. L_CE = R_CE = L, L_CLKEN = R_CLKEN = L
2. OE = L for the reading port.

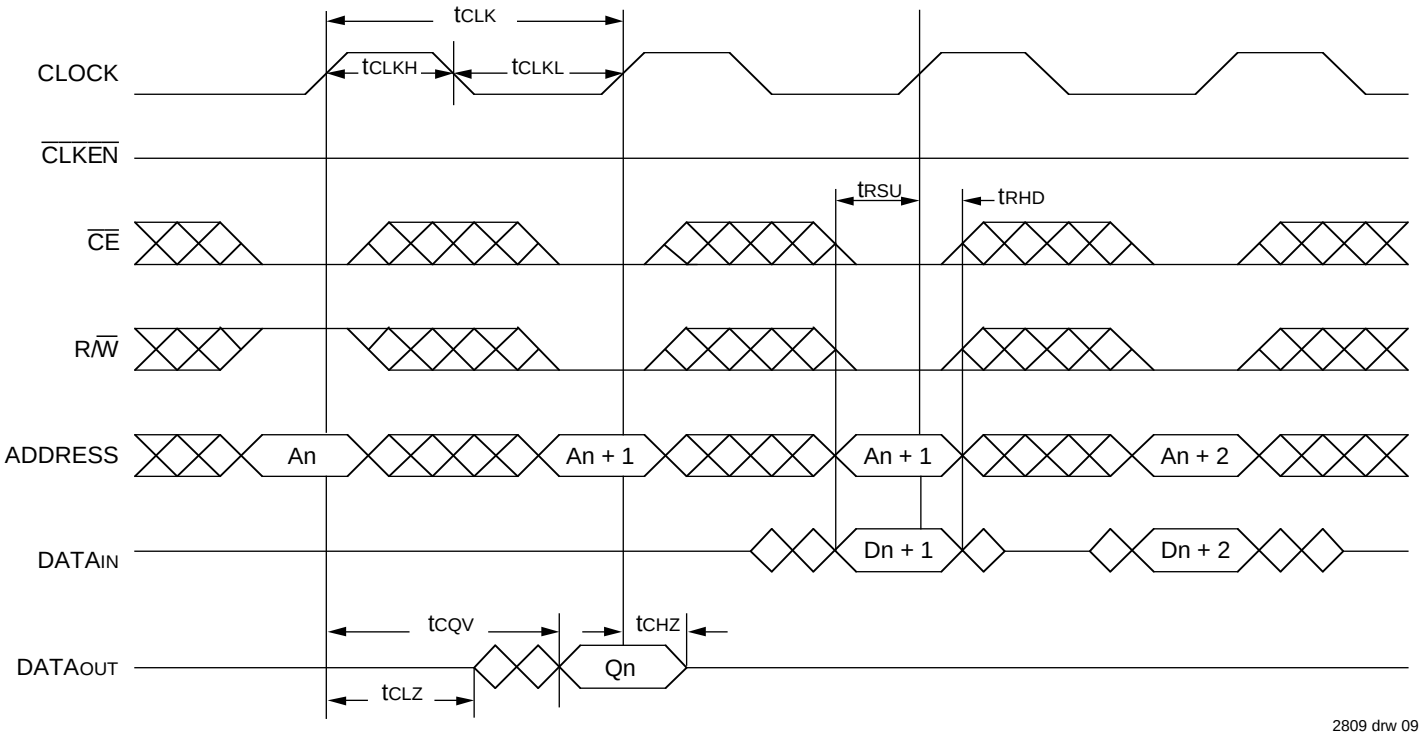
TIMING WAVEFORM OF READ-TO-WRITE CYCLE No. 1, CE HIGH(1)



2809 drw 08

NOTE:
1. $\overline{OE}$ LOW throughout.

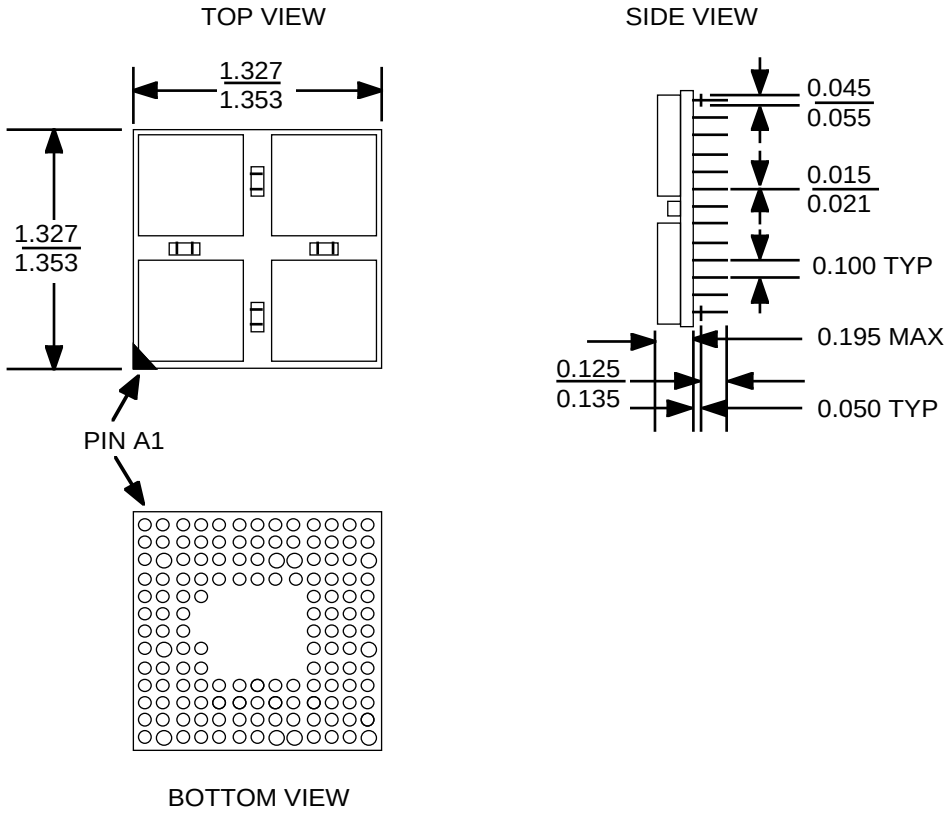
TIMING WAVEFORM OF READ-TO-WRITE CYCLE NO. 1, $\overline{CE}$ LOW(1,2)



2809 drw 09

NOTES:
1. During dead cycle, if $\overline{CE}$ is LOW, data will be written into array.
2. $\overline{OE}$ LOW throughout.

PACKAGE DIMENSIONS



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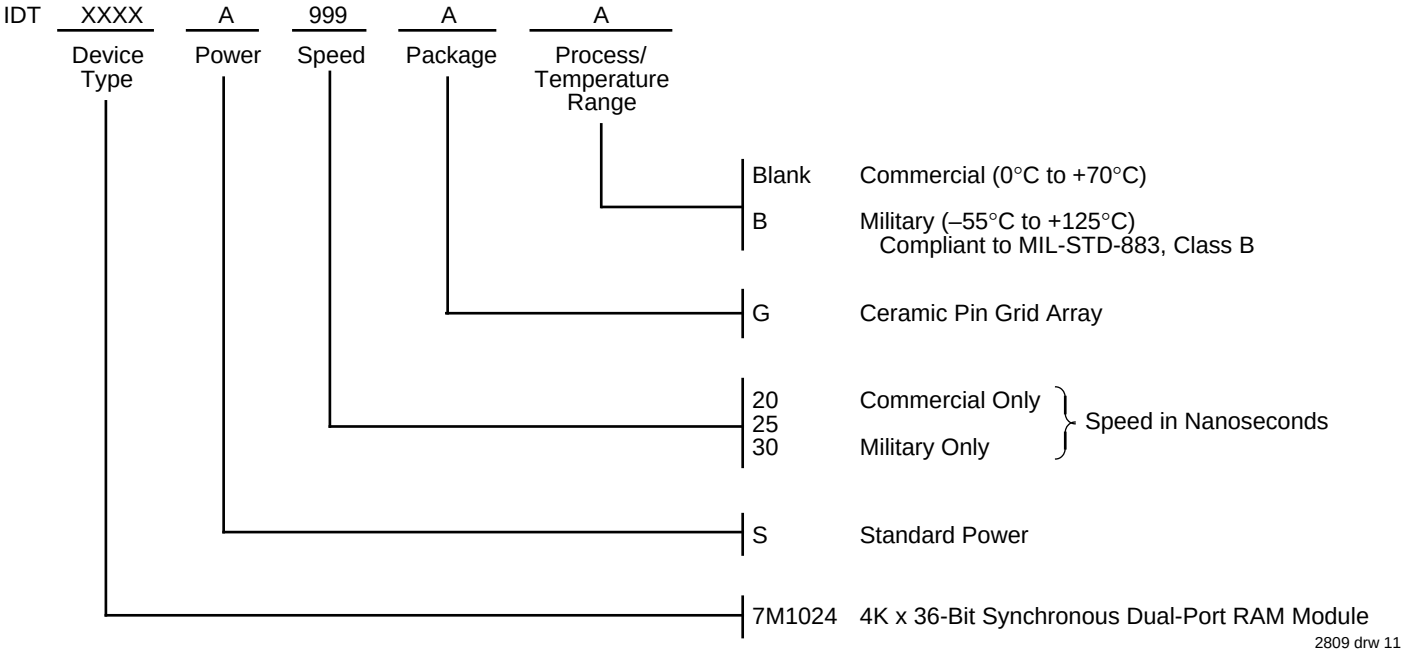
ORDERING INFORMATION



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