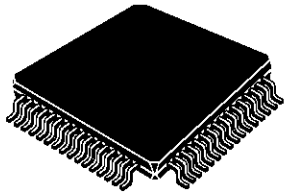
SGS-THOMSON MICROELECTRONICS

# STB4395

## CT2 RECEIVER/TRANSMITTER

**ADVANCE DATA**

- FULLY INTEGRATED DOUBLE SUPERHETERODYNE RECEIVER
- OPERATION FROM 800MHz TO 1000MHz
- RECEIVER OUTPUT AS BITSTREAM
- FULLY INTEGRATED TRANSMITTER
- TRANSMITTER INPUT I/Q/REFIQ OR *I/$\overline{I}$, Q/$\overline{Q}$*
- INTEGRATED POWER AMPLIFIER
- CT2 PA SWITCH-ON PROFILE INTEGRATED
- VCO's INTEGRATED
- SYNTHESIZERS INTEGRATED
- CHANNEL SELECT LOGIC ON CHIP
- INTEGRATED VOLTAGE REGULATION
- SUPPLY VOLTAGES FROM 3.0V TO 5.5V



**TQFP64**
(Plastic Package)

**ORDER CODE :** STB4395 or STB4395A

### DESCRIPTION

The STB4395(A) is a fully integrated receiver-transmitter designed for CT2 applications, and incorporates all the VCO's, synthesizers, PLLs, and channel select logic, to make a fully functional "single chip" radio.

The receiver is of the double superhet architecture and operates from an aerial input (via a SAW filter) to bitstream output to CT2 format, whilst the transmitter operates from I/Q inputs to +13dBm at the final frequency. A single (external) frequency reference is all that is required to give full coverage over the range of 800 to 1000MHz. The on-off slope of the Transmit PA is governed internally to give the required switch-on ramp, whilst the output can be swiched from low to high power by means of an external digital control signal.

The channel select is controlled from a digital serial input, and allows continuous channel control from 800 to 1000MHz.

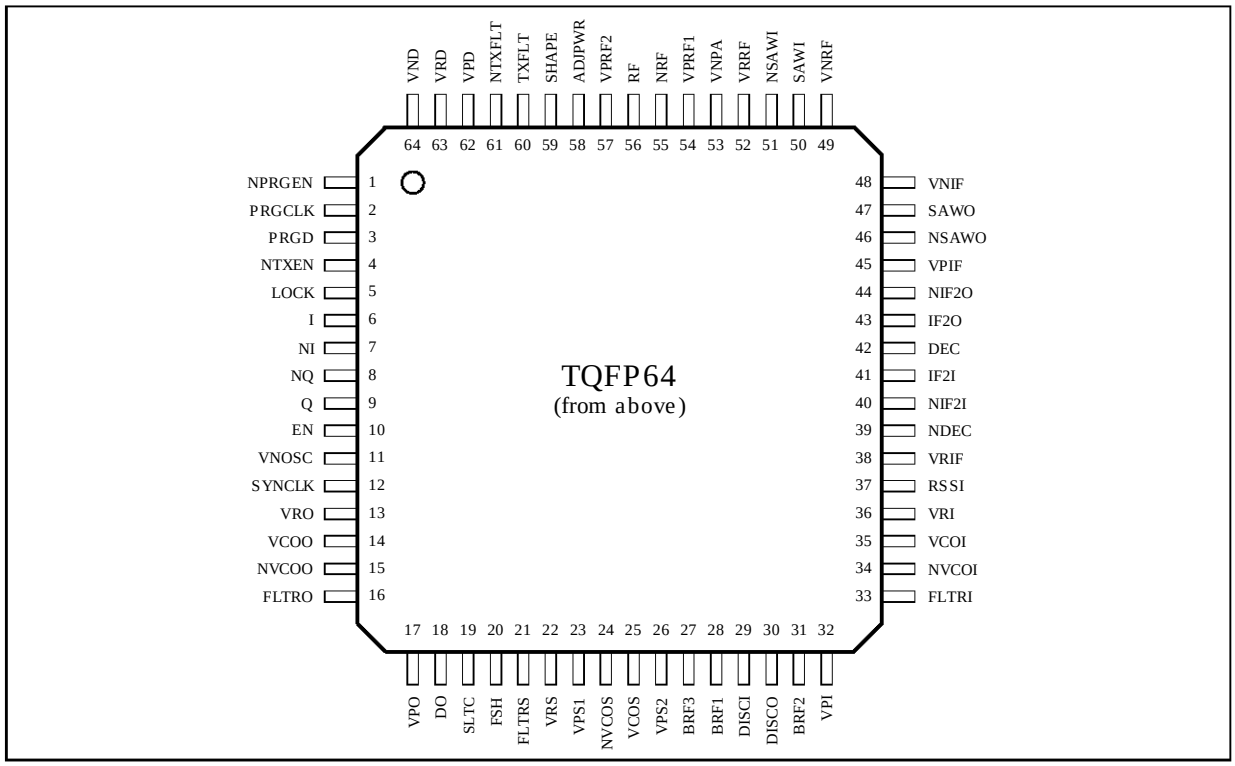
The STB4395 exists in two versions: the STB4395, which has *I/$\overline{I}$*, *Q/$\overline{Q}$* transmit data input/outputs, is designed to operate with the SGS-THOMSON baseband companion part, the ST5095. The STB4395A has a 3 wire I/Q interface and is compatible with commercially available I/Q transmit data baseband IC's.

CONTENT

## 1 - PIN DESCRIPTION

### 1.1 - Pin Connections

***STB4395***

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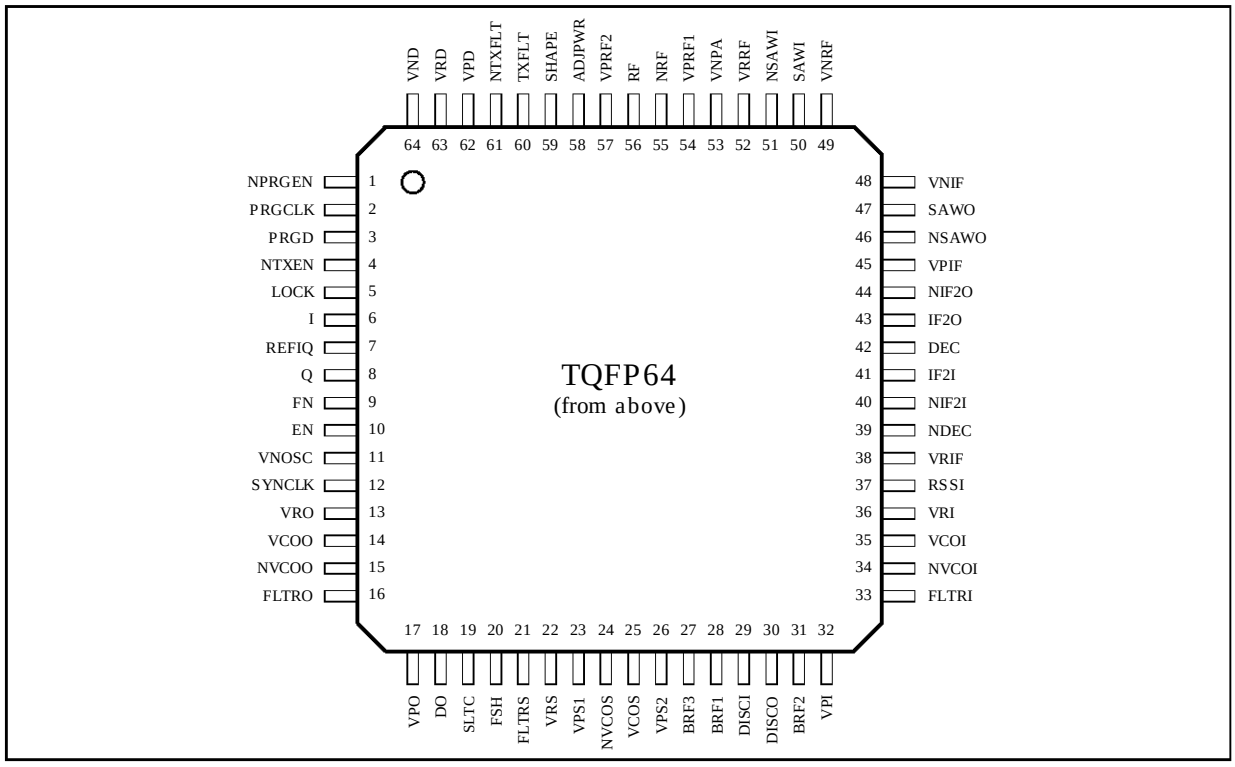
***STB4395A***

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## 1 - PIN DESCRIPTION (continued)

### 1.2 - Pin List

| Pin | Name | Description | Ext. Connection and Suppl. Information |
|---|---|---|---|
| 1 | NPRGEN | Serial Data Enable | |
| 2 | PRGCLK | Serial Data Clock | |
| 3 | PRGD | Serial Data Input | |
| 4 | NTXEN | Receive-Transmit Switch | |
| 5 | LOCK | VCO Lock Detect-all 3 PLL | |
| 6 | I | I - Transmit Quadrature Input | |
| 7 | NI | I - Transmit Quadrature Input | STB4395 only |
| 8 | NQ | Q-Transmit Quadrature Input | STB4395 only |
| 9 | Q | Q-Transmit Quadrature Input | STB4395 only |
| 7 | REFIQ | IQ Reference Quadrature Transmit Input | STB4395A only |
| 8 | Q | Q-Transmit Quadrature Input | STB4395A only |
| 9 | FN | Forces Data Slicer Reference Time Constant To fast | STB4395A only |
| 10 | EN | Power Down all functions except buffer | |
| 11 | VNOSC | Negative Power Supply all VCO 's | |
| 12 | SYNCLK | Synthesizer Clock Input | f = 14.4MHz A.C. coupled |
| 13 | VRO | PSU Regulated Negative Input for TX IF oscillator and pump circuit | |
| 14 | VCOO | TX oscillator tank circuit | |
| 15 | NVCOO | TX Oscillator Tank Circuit | |
| 16 | FLTRO | Loop Filter for TX PLL | |
| 17 | VPO | Positive Battery Supply for TX oscillator | |
| 18 | DO | Receive Data Output | |
| 19 | SLTC | Slicer Time Constant Capacitor | C= 33nF |
| 20 | FSH | Data Slicer Time Constant Setting | |
| 21 | FLTRS | Loop Filter for channel PLL | |
| 22 | VRS | Regulated Negative Supply for channel oscillator and pump circuit | |
| 23 | VPS1 | Positive Battery Input for channel oscillator and pump circuit | |
| 24 | NVCOS | Channel Oscillator Tank Input | 650 to 850MHz |
| 25 | VCOS | Channel Oscillator Tank Input | 650 to 850MHz |
| 26 | VPS2 | Positive Battery Supply Input for channel oscillator and pump circuit | |
| 27 | BRF3 | Bit Rate Filter3 | |
| 28 | BRF1 | Bit Rate Filter1 | |
| 29 | DISCI | FM Discriminator Tank Circuit | |
| 30 | DISCO | FM Discriminator Tank Circuit | |
| 31 | BRF2 | Bit Rate Filter 2 | |
| 32 | VPI | Positive Battery Supply for RXoscillator and pump circuit | |
| 33 | FLTRI | Loop Filter for RX oscillator | |
| 34 | NVCOI | RX Oscillator Tank Circuit | |
| 35 | VCOI | RX Oscillator Tank Circuit | |
| 36 | VRI | Regulated Negative Supply for RX oscillator and pump circuit | |
| 37 | RSSI | RSSI OUTPUT | |
| 38 | VRIF | Regulated Negative Supply Output for RX sections | |
| 39 | NDEC | RX IF2 Decoupling | |
| 40 | NIF2I | RX IF2 Filter Input | |
| 41 | IF2I | RX IF2 Filter Input | |
| 42 | DEC | RX IF2 Decoupling | |
| 43 | IF2O | RX IF2 Filter Output | |
| 44 | NIF2O | RX IF2 Filter Output | |
| 45 | VPIF | Positive Battery Supply Input for RX sections | |

## 1 - PIN DESCRIPTION (continued)

### 1.2 - Pin List (continued)

| Pin | Name | Description | Ext. Connection and Suppl. Information |
|---|---|---|---|
| 46 | NSAWO | RX First IF Amplifier Input | |
| 47 | SAWO | RX First IF Amplifier Input | |
| 48 | VNIF | Negative Battery Supply Input for RX sections | |
| 49 | VNRF | Negative Battery Supply Input for RF front end | |
| 50 | SAWI | RX First Mixer Output | |
| 51 | NSAWI | RX First Mixer Output | |
| 52 | VRRF | Regulated Negative Supply for RF front end | |
| 53 | VNPA | Negative Supply for power amplifier | |
| 54 | VPRF1 | Positive Battery Supply for RF front end | |
| 55 | NRF | Input LNA/Output PA | |
| 56 | RF | Input LNA/Ouput PA | |
| 57 | VPRF2 | Positive Battery Supply for RF front end | |
| 58 | ADJPWR | Transmit Power Adjust | R = 8.5kΩ to $V_{RRF}$ |
| 59 | SHAPE | Time Constant for PA on-off ramp | C = 560pF |
| 60 | TXFLT | Bandpass Filter for TX RF | |
| 61 | NTXFLT | Bandpass Filter for TX RF | |
| 62 | VPD | Positive Battery Supply for digital circuitry | |
| 63 | VRD | Regulated Negative Supply for digital circuitry | |
| 64 | VND | Negative Battery Supply for digital circuitry | |

### 1.3 - Analog and Filter Pins

| Pin | Symbol | Description |
|---|---|---|
| 58 | ADJPWR | Transmitter Output Power Adjust |
| 28 | BRF1 | Bit Rate Filter1 |
| 31 | BRF2 | Bit Rate Filter 2 |
| 27 | BRF3 | Bit Rate Filter 3 |
| 42, 39 | DEC, NDEC | RX IF2 Amplifier Decoupling |
| 29 | DISCI | FM Discriminator Tank Circuit |
| 30 | DISCO | FM Discriminator Tank Circuit |
| 33 | FLTRI | Loop Filter for RX PLL |
| 16 | FLTRO | Loop Filter for TX PLL |
| 21 | FLTRS | Loop Filter for Channel PLL |
| 6, 7 | I, NI(1) | Transmit Quadrature Inputs ((1)STB4395 only) |
| 40, 41 | IF2I, NIF2I | Inputs from 2nd IF Filter |
| 43, 44 | IF2O, NIF2O | Outputs to 2nd IF Filter |
| 8, 9 | Q, NQ(1) | Q-Transmit Quadrature Input ((1)STB4395 only) |
| 7 | REFIQ | IQ Reference Quadrature Transmit Input (STB4395A only) |
| 56, 55 | RF, NRF | Input RX LNA/Ouput TX PA |
| 37 | RSSI | Received Signal Strength Indicator Output |
| 50, 51 | SAWI, NSAWI | First Mixer Output |
| 47, 46 | SAWO, NSAWO | First IF Amplifier Input |
| 59 | SHAPE | Time Constant for PA on-off Ramp |
| 19 | SLTC | Slicer Time Constant Capacitor |
| 12 | SYNCLK | Synthesizer Clock Input 14.4MHz |
| 60, 61 | TXFLT/ NTXFLT | Bandpass Filter for TX RF |
| 35, 34 | VCOI, NVCOI | Tank Circuit for 152.1MHz RX Oscillator |
| 14, 15 | VCOO, NVCOO | Tank Circuit for 300.8MHz TX Oscillator |
| 25, 24 | VCOS, NVCOS | Tank Circuit for 650 to 850MHz Channel Oscillator |

## 1 - PIN DESCRIPTION (continued)

### 1.4- Digital, Signal and Control Pins

| Pin | Symbol | Description | Polarity |
|---|---|---|---|
| 18 | DO | Receive Data Output | |
| 20 | FSH | Data Slicer Time Constant Setting (Fast/Slow/Hold) | High: slow, tri-state: fast, low: hold DO goes high on hold (see next table) |
| 9 | FN | Forces Data Slicer Reference Time Constant to fast (STB4395A only) | low: fast (overides FSH) high: fast, slow or hold (set by FSH) |
| 5 | LOCK | VCO lock detect-all 3 PLL | high for LOCK (all three PLL's) |
| 3 | PRGD | Serial Synthesizer Data Input, 16 bits word | high for logic 1. Input sequence: LO, D14, D13,...,D0. D14 is the MSB. LO: logic 1 is low transmit power. |
| 1 | NPRGEN | Serial Synthesizer Data Enable | low to enable PRGD buffer |
| 2 | PRGCLK | Serial Data Clock | held high when no clocking, clocks in data on positive edge |
| 10 | EN | Power Down all functions except Enable Buffer | high for power up, low for standby |
| 4 | NTXEN | Receive-Transmit Switch | high for receive, low for transmit |

The time constant of the data slicer is set through the pins FSH and FN for the STB4395A and through FSH only for the STB4395(FN internally connected to High), as listed in the following table :

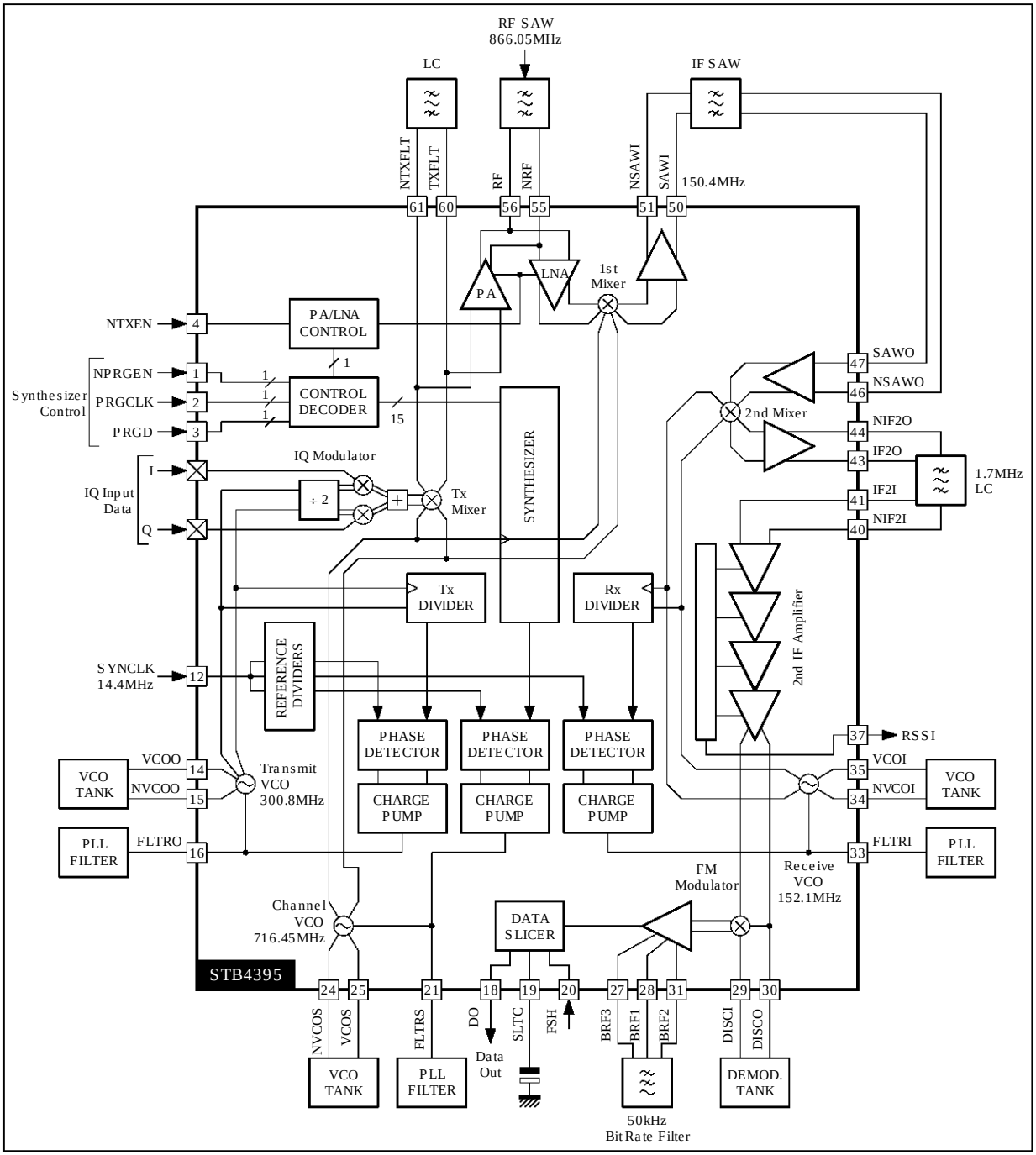
| PIN | | FN | |
|---|---|---|---|
| | | High | Low |
| FSH | High | Slow, DO active | Fast, DO active |
| | TriState | Fast, DO active | Fast, DO active |
| | Low | Hold, DO high | Fast, DO high |

### 1.5 - Power Supply Pins

| Pin | Symbol | Description |
|---|---|---|
| 64 | VND | Negative supply for digital regulators, digital input and output buffers |
| 48 | VNIF | Negative supply for IF regulators, data output buffer |
| 11 | VNOSC | Negative supply for the oscillator regulators + substrate |
| 49 | VNRF | Negative supply RF regulators, quadrature input buffers |
| 53 | VNPA | Negative supply for PA |
| 62 | VPD | Positive supply for digital circuitry |
| 32 | VPI | Positive supply for receive oscillator + charge pump |
| 45 | VPIF | Positive supply for RX IF + baseband sections |
| 17 | VPO | Positive supply for transmit oscillator + charge pump |
| 54, 57 | VPRF1 / VPRF2 | Positive supplies for RF front end |
| 23, 26 | VPS1/ VPS2 | Positive supplies for ch. select oscillator + charge pump |
| 63 | VRD | Regulated negative supply for digital circuitry |
| 36 | VRI | Regulated negative supply for receive oscillator + charge pump |
| 38 | VRIF | Regulated negative supply for RX IF + baseband sections |
| 13 | VRO | Regulated negative supply for transmit oscillator + charge pump |
| 52 | VRRF | Regulated negative supply for RF front end |
| 22 | VRS | Regulated negative supply ch. select oscillator + charge pump |

## 2 - BLOCK DIAGRAM

**Figure 1**



## 3 - FUNCTIONAL DESCRIPTION

Figure 1 is a simplified block diagram of the circuit. It shows the key on-chip and off-chip functional blocks and signal paths. For illustration purposes frequencies have been added representing the situation when receiving or transmitting a particular CT2 channel.

### 3.1 - Receiver

The receive signal enters the STB4395 via an input SAW filter (866 MHZ for CT2 in Europe). The RF filter changes the input signal from a single ended to a balanced signal, after which the signal passes through the LNA, first mixer, and mixer buffer. The mixer is driven by the channel VCO, which is in turn controlled by the synthesizer.

The signal path continues via the first IF SAW (150.4MHz), IF amplifier to the second mixer. The second mixer stage mixes down to 1.7MHz, and via an external LC IF filter, is passed to the second IF amplifier, where the main system gain takes place. The RSSI output is available from this point.The signal is then demodulated and sliced into a data stream which is the binary digital output available to the base band chip.

The channel selection is provided by the two external filters: the first IF SAW and a second IF 2-pole LC filter.

### 3.2 - Transmitter

The chip accepts 72Kbits/s data in an I/Q format. The I/Q inputs pass via the I/Q modulator to the TX mixer. The TX mixer is driven by the same channel VCO as the receive first mixer.

The on-off ramp of the transmit PA.is controlled via an external capacitor to give minimum spurious responses when switching on and off.

The PA output power can be switched from full power to -3dBm by the channel select control signal (bit LO of the 16bits serial word PRGD, see table, paragraph 1.4).

### 3.3 - Channel Select Control Logic

All channel phase locked loops and oscillators are included on chip. The channel control synthesizer is controlled externally via a 3 wire interface.

The Reference clock input of 14.4 MHz is divided using preset counters to set the phase detector /charge pump loops for the synthesizer/channel select VCO, the second receiver VCO, and the I/Q transmit VCO. The phase detector inputs for the fixed frequency VCO's are via pre set dividers also.

The channel select control and Transmit PA control is via a 16 bit serial word, which is generated by the system controller. 15 bits of this serial word are used for the channel information, and 1 bit is used to set the output power of the transmit PA. The word length is sufficient to give full channel coverage over the range from 800 to 1000MHz with integer multiples of 50KHz. The section "system clock input" gives a detailed description.

Not shown in the diagram are the voltage regulators for the receive LNA/first mixer, Transmit PA, TX mixer and the remainder of the circuit.There are 6 internal voltage regulators to ensure the minimum of mutual interference.

## 4 - ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_P$-$V_N$ | Power Supply Voltage | 7.0 | V |
| $V_P$ - $V_{IN}$ | Voltages on Input (except SYNCLK) | 5.9 | V |
| $V_P$ - $V_{IN}$ | Voltage on Input (SYNCLK) | 3.0 | V |
| $V_{IN}$ - $V_N$ | Voltages on Input | 7.0 | V |
| $V_P$- $V_{OUT}$ | Voltages on Output | 7.0 | V |
| $V_N$ - $V_{OUT}$ | Voltages on Output | 7.0 | V |
| $V_{RFO}$ | Voltage Out of RF or NRF in TX | 3.5 | $V_{PP}$ |
| $T_{stg}$ | Storage Temperature | 125 | $^oC$ |
| $T_{oper}$ | Operating Temperature | 40 | $^oC$ |

## 5 - POWER SUPPLIES

### 5.1 - Supplies

The chip operates from a power supply of 3.0 to 5.5 Volts. All interface circuits to the baseband chips are operated between these supplies.
Six on-chip regulators are included on-chip which provide to all parts of the circuit separate regulated voltage supplies of -2.85 ±0.15 Volts relative to the top rail for the RF circuitry, the IF circuitry, the digital circuitry and for the three VCO's.
The chip can be operated in 3 modes, power down, receive and transmit. Power down is activated taking the Pin EN to $V_N$ . To transfer to the receive mode, NTXEN is taken to $V_P$.
The built-in regulators can be by-passed ,if so required.

### 5.2 - Ground Plane Connections

The chip has been designed to be decoupled to the positive supply, $V_P$ , at many points. Therefore it is strongly recommended that the chip be mounted on a board with a ground plane connected to $V_P$.

Because the base band chip is specified relative to a negative ground, it is further recommended that the board used is a 4 layer board with both a positive, $V_P$ , and negative ground plane $V_N$ . This has the additional advantage of providing good high frequency decoupling between supplies.

The question as to whether to call $V_P$ or $V_N$ ground depends on which external equipment is connected. For testing the baseband section, this is $V_N$ ; for testing the radio chip, this is $V_P$. In a product, this will depend on the application.

For clarity all voltages specified in this document will be specified with respect to the supply, $V_P$ or $V_N$ , that the voltage normally tracks with when the supply is varied.

## 6 - ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_N$ | Power Supply Voltage (unregulated) | -3 | | -5.5 | V |
| $V_{REG}$ | Power Supply bypassing Internal Regulators (this is also interface supply) | -2.7 | | -3 | V |
| IRX | Receive Mode | | 32 | 40 | mA |
| ITX | Transmit Mode | | 68 | 80 | mA |
| IQ | Standby/Power Down | | | 20 | µA |

## 7 - TIMING INFORMATION

### 7.1 - Turn on-off Times

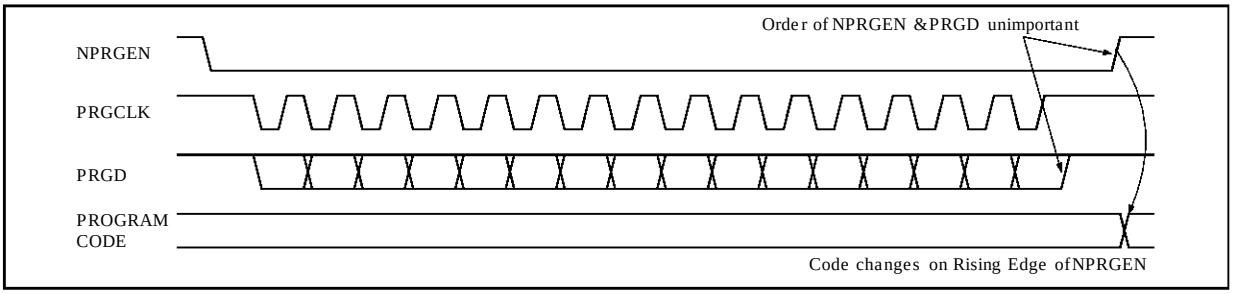
Times are relative to the NTXEN transition (high to low for receive to transmit and low to high for transmit to receive).

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{ON}$ | Turn-on Time From standby to receive | | | 10 | µs |
| $t_{RAMPON}$ | PA Power Ramp up to reach -3dB of final power | | | 27.78 | µs |
| $t_{TXRX}$ | Switchover Time Transmit to Receive (LNA/first mixer active) | | | 27.78 | µs |

### 7.2 - Channel Select Timing

PRGCLK must be high before NPRGEN goes low to programme the synthesizer.

**Figure 2 :** Timing of Serial Programming Data




Note that although a new program code is implemented on the rising edge of the NPRGEN, the transmitted power level is delayed until at the start of the next burst of transmission. In order to change transmit power during a conversation, the required power code must be serially loaded with the power change instruction.

## 8 - TRANSCEIVER SECTION

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $f_{OP}$ | Frequency Range | 800 | | 1000 | MHz |
| | Channel Frequency Accuracy | -1 | 0 | 1 | kHz |
| | Modulation Deviation (synchronised with72 Kbits/s data rate) | | 18 | | kHz |
| $P_{OUTTX}$ | Output Power (300Ω balanced) high power mode | 13 | | | dBm |
| | Sensitivity (source 300Ω balanced) for 1E-3 BER | -103 | -105 | | dBm |
| | Signal max. for 1E-3 BER | | | 0 | dBm |

### 8.1 - Receiver-Input Specification

#### *LNA, first mixer and buffer*

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| | Conversion voltage gain | | 33.7 ± 1.5 | | dB |
| | Available conversion power gain | | 21.5 ± 1.5 | | dB |
| | Input impedance | | 300Ω // 3pF | | - |
| | Output impedance | | 5kΩ // 3pF | | - |
| | Source impedance | | 300Ω // -3pF | | - |
| | Load impedance | | 5kΩ // -3pF | | - |
| | Noise figure | | 3.5 | | dB |
| | 1dB compression point (input) | | -24 | | dBm |
| | Third order intercept (input) | | -14 | | dBm |

#### *First IF amplifier, second mixer and buffer*

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| | Conversion Voltage Gain | | 22.0 ± 1.5 | | dB |
| | Available Conversion Power Gain | | 16.3 ± 1.5 | | dB |
| | Input Impedance | | 700Ω // 2pF | | - |
| | Output Impedance | | 2kΩ // 2pF | | - |
| | Source Impedance | | 700Ω // -2pF | | - |
| | Load Impedance | | 2.8kΩ // -2pF | | - |
| | Noise Figure | | 6 | | dB |
| | 1dB Compression Point (input) | | -32 | | dBm |
| | Third Order Intercept (input) | | -22 | | dBm |

#### *Second IF amplifier*

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| | Conversion Voltage Gain | | 82 ± 3 | | dB |
| | Available Power Gain (to DISCO) | | 86 ± 3 | | dB |
| | Bandwith (3dB) | | 3 | | MHz |
| | Input Impedance | | 10kΩ // pF | | - |
| | Output Impedance (to DISCO) | | 1.1kΩ // 2F | | - |
| | Source Impedance | | 2.2kΩ // -2pF | | - |
| | Load Impedance (at DISCO) | | see App. Diag. | | |
| | Noise Figure | | 6 | | dB |
| | 1dB Compression Point (input) | | -108 | | dBm |

**8 - TRANSCEIVER SECTION** (continued)

***Dataslicer time constants***

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| | Slow | | 3* | | ms |
| | Fast | | 130* | | µs |
| | Hold Drift Rate 60mV < signal < 100mV | | 1 | | mV/ms |

For 33nF capacitor at SLTC

### 8.2 - Transmitter-Output Specification

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $P_{OUT}$ | Output Power into 300Ω balanced, high power mode | 13 | | | dBm |
| | LO Rejection | 25 | | | dBC |
| | Output Control Switch | | 14 | | dB |

***TXFLT/NTXFLT output***

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| | Output Impedance | | 2 | | kΩ |
| | Load Impedance (external) | | 1.2 | | kΩ |
| | Voltage Out (channel frequency, application circuit of this D/S) | | 200 | | $mV_{PP}$ |
| | Voltage Out (channel frequency-300.8MHz, app. cct of this D/S) | | 80 | | $mV_{PP}$ |

### 8.3 - Synthesizer/Modulator/Channel Select Loop

### 8.3.1 - Synthesizer Phase Noise and Spurious

Phase noise and spurious are measured at the RF outputs RF / NRF in transmit mode, no RF SAW filter.

***Phase Noise*** *(Average)*

| Offset Frequency from carrier | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| ±100kHz | | -106 | | dBc/Hz |
| ±500kHz | | -121 | | dBc/Hz |
| ±1MHz | | -127 | | dBc/Hz |
| ±10MHz | | -145 | | dBc/Hz |

***Spurious***

| Offset Frequency from carrier | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| ±50kHz | | -55 | | dBc |
| ±100kHz | | -63 | | dBc |
| ±200kHz | | -70 | | dBc |
| ±200kHz to ±10MHz | | -75 | | dBc |
| ±10MHz to ±100MHz | | -40 | | dBc |

### 8.3.2 - Channel Select Loop

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| | Frequency | | channel - 150.4 | | MHz |
| | Frequency Steps | | 50 | | kHz |

**8 - TRANSCEIVER SECTION** (continued)

### 8.3.3 - Channel Frequency Setting

#### 8.3.3.1 - General Case

Using, from the divider ratios : and from the mixers :

$F_{CH} = CH*FX/288$ $F_{IF2} = F_{RX} - F_{IF1}$

$F_{RX} = RX*FX/16$ $F_{IF1} = F_{RF} - F_{CH}$

$F_{IFTX} = 0.5*F_{TX}$ $F_{RF} = F_{CH}+F_{IFTX}$

$F_{TX} = TX*F_{SYN}/18$

the RF frequency is related to the other frequencies by :

$F_{RF} = F_{CH} + F_{IFTX} = CH * F_{SYN}/288 + TX * F_{SYN}/18 * 0.5$

$= F_{CH} + F_{RX} - F_{IF2} = CH * F_{SYN}/288 + RX * F_{SYN}/16 - F_{IF2}$

Hence the channel select input (15 of the 16 digits, see pin table, paragraph 1.4) serial data stream :
$CH = (F_{RF} - TX*F_{SYN}/18*0.5) * 288/F_{SYN} = 288* F_{RF}/F_{SYN} - 3008$ and $CH = 288 (F_{RF} + F_{IF2})/F_{SYN} - 3042$

where :

$F_{CH}$ is the channel PLL synthesizer frequency
$F_{IF1}$ is the first if frequency (receive)
$F_{IF2}$ is the second if frequency (receive)
$F_{IFTX}$ is the transmit if frequency
$F_{RF}$ is the desired rf frequency
$F_{RX}$ is the receive offset PLL frequency
$F_{SYN}$ is the reference input frequency (on SYNCLK)
$F_{TX}$ is the transmit offset PLL frequency
RX is the fixed receive divide ratio of 169
TX is the fixed transmit divide ratio of 376
CH is the channel synthesizer divide ratio defined by the binary channel number,
e.g. D14,D13,.....D0

The channel synthesizer provides integral division for all numbers between 3968 and 32764 (binary 000111110000000 to 111111111111100). Binary numbers outside this range will cause division ratios not directly related to binary code.

#### 8.3.3.2 - Particular Case. with $F_{SYN}$ = 14.4MHz :

$F_{RX} = 152.1MHz$
$F_{TX} = 300.8MHz$
$F_{IFTX} = 150.4MHz$
$F_{IF1} = 150.4MHz$
$F_{IF2} = 1.7MHz$

Then $CH = 20 * F_{RF} - 3008$

Example : desired RF frequency, $F_{RF} = 866.05MHz$

Then substituting in : $CH = 20*866.05-3008 = 14313$ (binary 011011111101001)

## 8 - TRANSCEIVER SECTION (continued)

### 8.4 - System Clock Input

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $f_{REF}$ (*1) | Reference Frequency | | 14.4 | | MHz |
| $V_S$ | Input Voltage Swing, AC Coupled, referenced to $V_P$ | 0.4 | | 0.8 | V |
| $I_{IH}$ | Input Current-High (with respect to $V_N$) | -40 | | | µA |
| $I_{IL}$ | Input Current-low (with respect to $V_N$) | | | 40 | µA |

(*1) limits according to ETSI specification

### 8.5 - RF/NRF Receive/Transmit Pins

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $Z_{IN}$ | Input Impedance (balanced, RX) | | 300Ω // 3.5pF | | - |
| VSWR | VSWR | | | 1.5:1 | - |
| $V_{IN\ DC\ Max.}$ | DC Input Voltage | | | 0 | V |
| $P_{IN\ AC\ Max.}$ | AC Input Power | | | 0 | dBm |
| $Z_{OUT}$ | Output Impedance (balanced, TX) | | 300Ω // 3pF | | - |

### 8.6 - Digital Input Buffers NTXEN, PRGD, NPRGEN, PRGCLK, FN

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{IH}$ | Upper Level Input Voltage | $V_P$ -1 | | $V_P$ +0.4 | V |
| $V_{IL}$ | Lower Level Input Voltage | $V_N$ -0.4 | | $V_N$ + 1 | V |
| $I_{IH}$ | Input Current High | -10 | | | µA |
| $I_{IL}$ | Input Current Low | | | 40 | µA |
| Tt | Input Edge Transition | 0.1 | | 1 | µs/V |

### 8.7 - Digital Output Buffers xLOCK, DO

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{OH}$ | Upper Level Output Voltage | $V_P$ -0.3 | | $V_P$ | V |
| $V_{OL}$ | Lower Level Output Voltage | $V_N$ | | $V_N$ + 1 | V |
| $t_R$ | Rise Time (load of 5pF) | | 0.3 | | µs/V |
| $t_F$ | Fall Time (load of 5pF) | | 0.4 | | µs/V |

### 8.8 - Receiver - FSH Tri State Input

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $V_{IH}$ | Upper Level Input Voltage | $V_P$ -0.3 | | $V_P$ +0.4 | V |
| $V_{IL}$ | Lower Level Input Voltage | $V_N$-0.4 | | $V_N$ + 1 | V |
| $I_{TR}$ | Tri State Current | -10 | | 10 | µA |
| $I_{IH}$ | Input Current High | -100 | | | µA |
| $II_L$ | Input Current Low | | | 100 | µA |
| $T_t$ | Input Edge Transition | 0.1 | | 1 | µs/V |

## 8 - TRANSCEIVER SECTION (continued)

### 8.9 - Receiver-RSSI Output

The receiver output swings between $V_P$ and $V_N$.The buffer output supplies a current to an on-chip resistor connected to $V_N$. The output has to be smoothed externally with a capacitor to $V_N$.

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $P_{MIN}$ | Min RF Input Power Registered | | | -90 | dBm |
| $P_{MAX}$ | Max RF Input Power Registered | -44 | | | dBm |
| $R_{OUT}$ | Output Resistance (internally connected to $V_N$) | | 50 | | kΩ |
| $V_{MIN}$ | Voltage for $P_{MIN}$ | | $V_N$+1.25 | $V_N$+2 | V |
| $V_{MAX}$ | Voltage for $P_{MAX}$ | $V_N$ | $V_N$+0.25 | | V |
| CF | conversion factor | | -200 | | mV/decade |

### 8.10 - Power Down Buffer, EN

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{IH}$ | Upper Level Input Voltage | $V_P$ -0.3 | | $V_P$ +0.4 | V |
| $V_{IL}$ | Lower Level Input Voltage | $V_N$ -0.4 | | $V_N$ +0.3 | V |
| $I_{IH}$ | Input Current High | -350 | | | µA |
| $I_{IL}$ | Input Current Low | | | 10 | µA |
| $t_{ON}$ | Buffer Delay to LOCK HI (1) | | | 10 | ms |
| $tO_{FF}$ | Buffer Delay to min Supply Current (1) | | | 10 | ms |

(1) assumes application circuit with 100nF on each regulator.

### 8.11 - Transmitter-Data Inputs

#### 8.11.1 - I,Q,REFIQ (STB4395A)

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $R_{EXT}$ | External Input Resistance | 6.5 | 6.8 | 7 | kΩ |
| $R_{INT}$ | Internal Input Resistance | 32 | 40 | 50 | kΩ |
| $R_{IM}$ | $R_{INT}$ Matching Error | | | 1 | % |
| $V_{DC}$ | DC Bias to $R_{EXT}$ | 0.96VHS | | 1.04VHS | V |
| $V_{DC\ match}$ | $V_{DC}$ Matching Error to $R_{EXT}$ | | | 5 | mV |
| $V_S$ | Peak Voltage Swing to $R_{EXT}$ | 0.45 | 0.5 | 0.56 | V |
| $V_{S\ match}$ | $V_S$ Matching Error to $R_{EXT}$ | | | 0.5 | dB |
| | Phase(I-Q) | 88.5 | 90 | 91.5 | degrees |

VHS = ($V_P$ + $V_N$)/2

#### 8.11.2 - I,Q,NI,NQ (STB4395)

VHS = ($V_P$+$V_N$)/2 - VHR = ($V_P$+VRD)/2

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $R_{EXT}$ | External Input Resistance | | 2 | | kΩ |
| $R_{INT}$ | Internal Input Resistance | 32 | 40 | 50 | kΩ |
| $R_{IM}$ | $R_{INT}$ Matching Error | | | 1 | % |
| $V_{DC}$ | DC bias to $R_{EXT}$ | VHS-0.7 | | VHR+0.7 | V |
| $V_{DC\ match}$ | $V_{DC}$ Matching Error to $R_{EXT}$ | | | 12 | mV |
| $V_S$ | Peak Voltage Swing to $R_{EXT}$ | 0.7 | 0.75 | 0.85 | V |
| $V_{S\ match}$ | $V_S$ Matching Error to $R_{EXT}$ | | | 20 | mV |
| | Phase (I/Ibar and Q/Qbar) | 88.5 | 90 | 91.5 | degrees |
| | Phase I to Ibar or Q to Qbar | | 0 | | degrees |

## 9 - APPLICATIONS

### 9.1 - Typical DC connection schemes

#### 9.1.1 - Internal Regulator

The STB4395 has built-in internal regulators which allows 15mA to be used for external circuitry. The output of this regulator is -2.85V with respect to the positive supply rail.

#### 9.1.2 - External Regulator

The STB4395 will always generate its own supply voltage(-2.85V with respect to $V_P$), but the I/O interfaces allow the STB4395 to swing its output levels to the supply rails ($V_P$ to $V_N$). The system and baseband controller can therefore be connected from the same -unregulated- supply and be individually regulated, if required .

### 9.2 - Application Circuits

#### 9.2.1 - Introduction

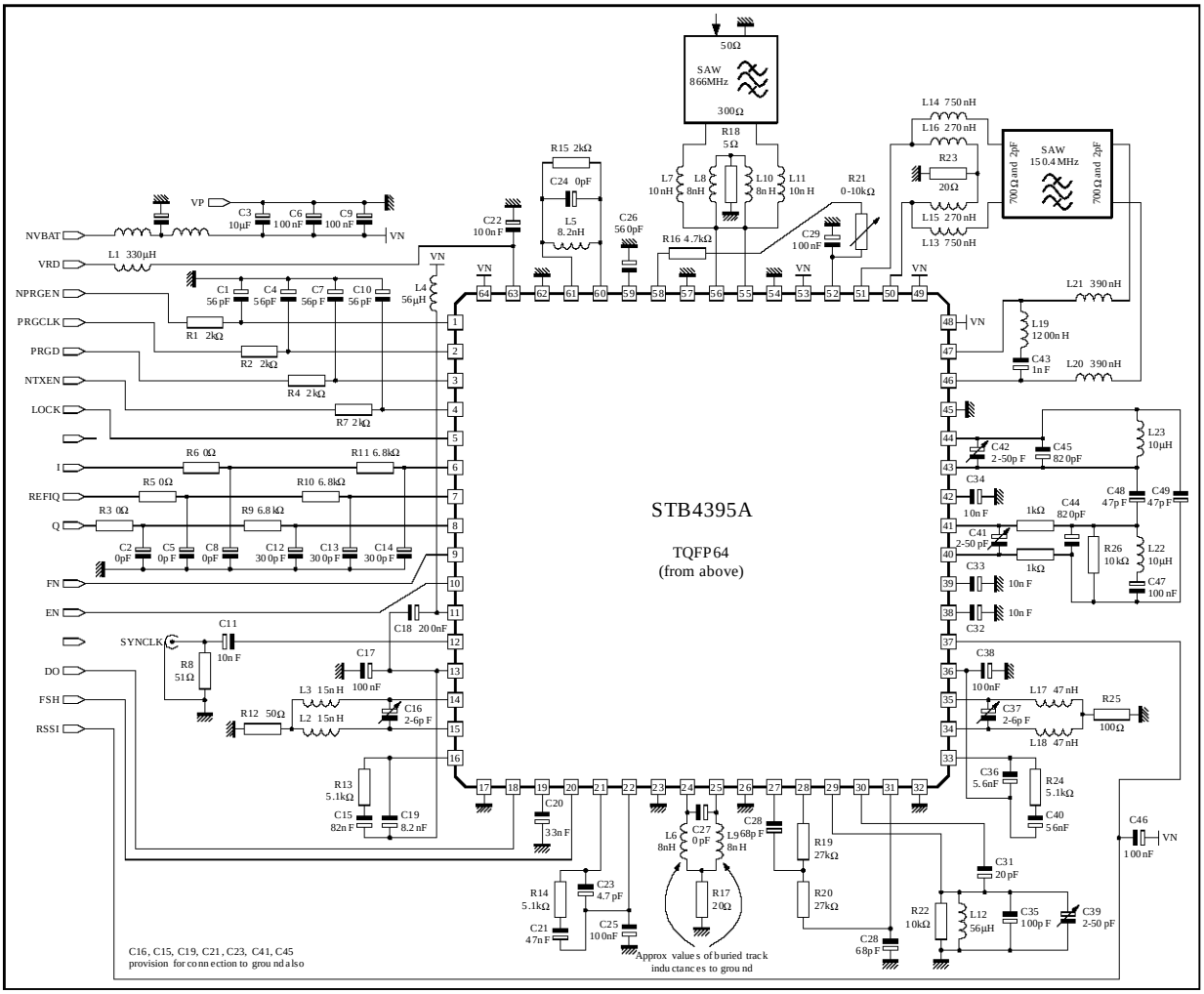
The STB4395 makes use of some unusual circuit configurations :

- The STB4395 operates from positive ground. The decoupling of the supply lines should take into account that the a.c. ground connections will be reversed with respect to the baseband circuit and/or the microcontroller. The use of multilayer PCB is recommended.
- The filters have been adapted for the best performance of the IC, although standard configurations are also considered.

#### 9.2.2 - Fully Configured Applications Example

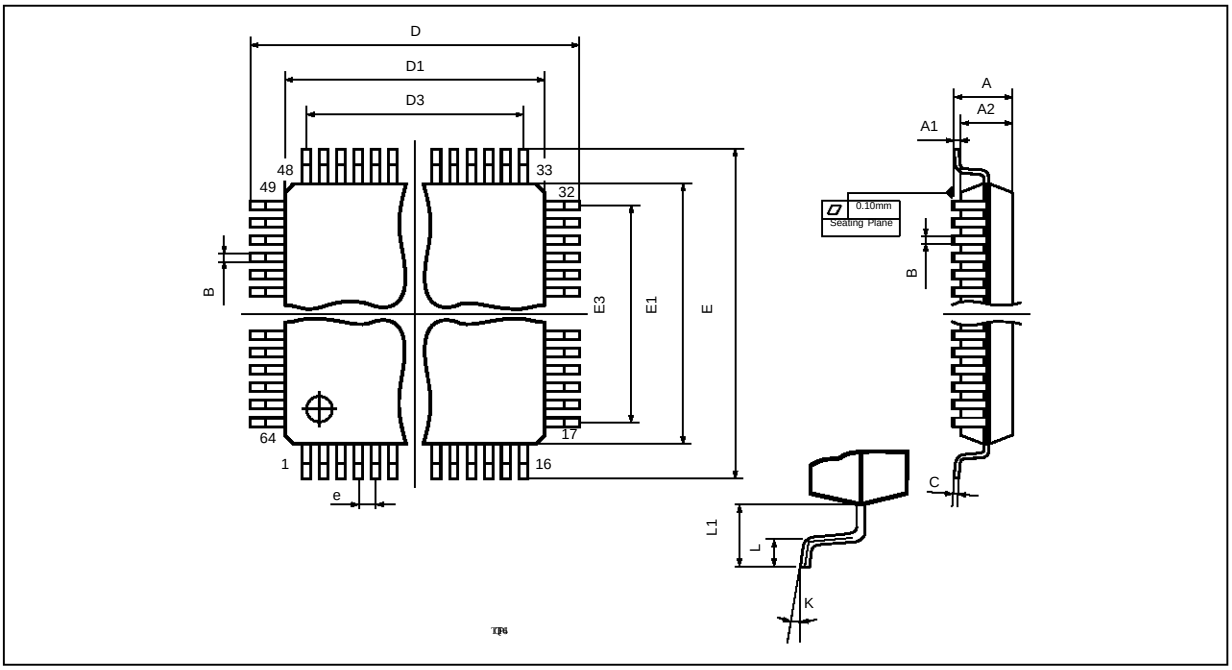
Figure 3 is a typical application circuit for a complete system. It shows the typical external components to the circuit. As the reactance of the components is critical in many locations, the use of surface mounted components is essential. A typical component list is also attached. It also shows the typical values for the the various VCO circuits. The values are very dependent on layout.

**Figure 3**



## PACKAGE MECHANICAL DATA

64 PINS - PLASTIC QUAD FLAT PACK (THIN)




| Dimensions | Millimeters | | | Inches | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | | | 1.60 | | | 0.063 |
| A1 | 0.05 | | 0.15 | 0.002 | | 0.006 |
| A2 | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| B | 0.18 | 0.23 | 0.28 | 0.007 | 0.009 | 0.011 |
| C | 0.12 | 0.16 | 0.20 | 0.0047 | 0.0063 | 0.0079 |
| D | | 12.00 | | | 0.472 | |
| D1 | | 10.00 | | | 0.394 | |
| D3 | | 7.50 | | | 0.295 | |
| e | | 0.50 | | | 0.0197 | |
| E | | 12.00 | | | 0.472 | |
| E1 | | 10.00 | 1 | | 0.394 | |
| E3 | | 7.50 | | | 0.295 | |
| K | $0^o$ (Min.), $7^o$ (Max.) | | | | | |
| L | 0.40 | 0.60 | 0.75 | 0.0157 | 0.0236 | 0.0295 |
| L1 | | 1.00 | | | 0.0393 | |

TQFP64.TBL