MN3674

Color CCD Linear Image Sensor with 512 Pixels for R and B Colors/1024 Pixels for G Color

■ Overview

The MN3674 is a high responsivity CCD color linear image sensor with 512 pixels each for R and B and 1024 G pixels, and having low dark output floating photodiodes in the photodetector region and CCD analog shift registers for read out.

It can read a 64mm-width color document with a high quality and a maximum pseudo resolution of 400dpi. In addition to being used as a color sensor, this device can also be used as a black and white sensor if only the G row is used, and in this case, it is possible to read a 64mm-width document with a full resolution of 400dpi. Since a one line delay analog memory is built in so as to compensate for the difference in the positions of reading out between the R, B rows and the G row, the configuration of the signal processing circuit becomes simpler.

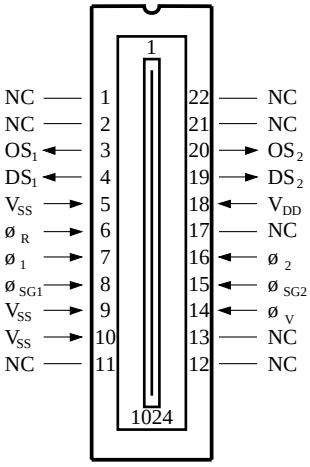
■ Features

- 2048 floating photodiodes and n-channel buried type CCD shift registers for read out are integrated in a single chip.
- RGB primary colors type on chip color filters are used for color separation.
- In order to compensate for the distance between the photodiode rows for the R, B colors and the G color, the device has a built in analog memory that can store the signals of one line of the R-B colors row.
- All clock inputs can be driven by 5V CMOS logic.
- Use of photodiodes with a new structure has made the dark output voltage very low.
- Large signal output of typically 0.8V at saturation can be obtained.

■ Application

- Color graphic read out in color image scanners, color fax machines, etc.

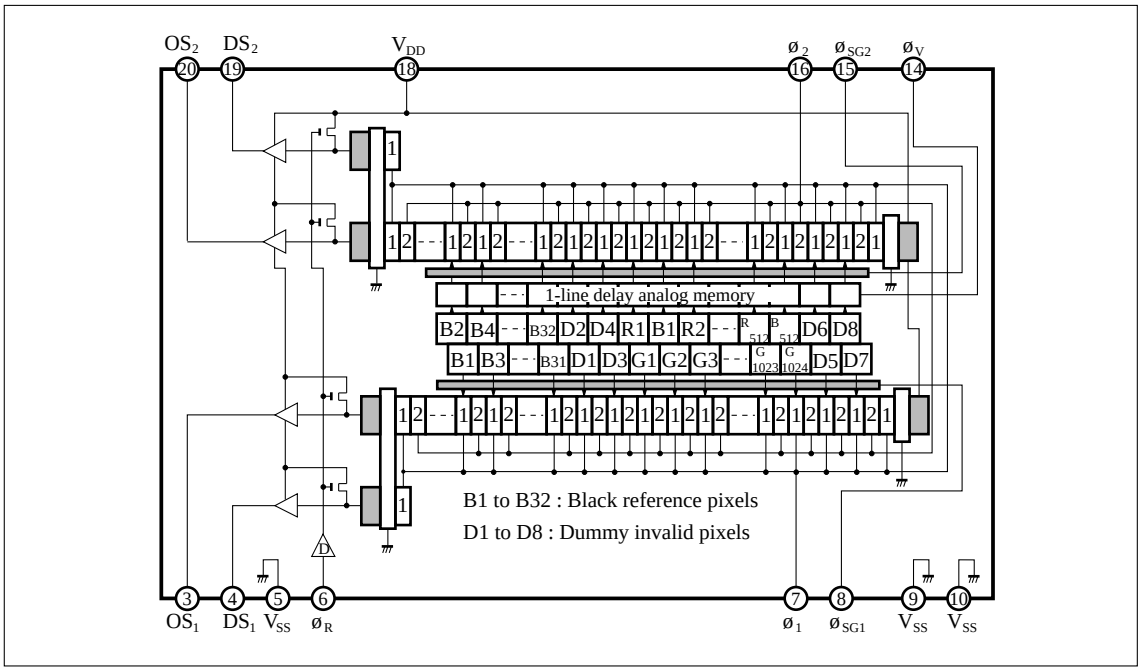
■ Pin Assignments



(Top View)

C26 WDIP022-G-0470B

■ Block Diagram



■ Absolute Maximum Ratings (Ta=25˚C, V_{SS}=0V)

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{DD}	– 0.3 to + 15	V
Input pulse voltage	V_I	– 0.3 to + 15	V
Operating temperature range	T_{opr}	0 to + 60	˚C
Storage temperature range	T_{stg}	–25 to + 85	˚C

■ Operating Conditions

• Voltage conditions (Ta=0 to + 60˚C, V_{SS}=0V)

Parameter	Symbol	Condition	min	typ	max	Unit
Power supply voltage	V_{DD}		11.4	12.0	13.0	V
CCD shift register clock High level	$V_{øH}$	($ø_1$, $ø_2$)	4.5	5.0	V_{DD}	V
CCD shift register clock Low level	$V_{øL}$		0	0.2	0.5	V
Vertical transfer clock High level	V_{VH}	($ø_V$)	4.5	5.0	V_{DD}	V
Vertical transfer clock Low level	V_{VL}		0	0.2	0.5	V
Shift gate clock High level	V_{SH}	($ø_{SG1}$, $ø_{SG2}$)	4.5	5.0	V_{DD}	V
Shift gate clock Low level	V_{SL}		0	0.2	0.5	V
Reset gate clock High level	V_{RH}	($ø_R$)	4.5	5.0	V_{DD}	V
Reset gate clock Low level	V_{RL}		0	0.2	0.5	V

• Timing conditions (without 1-line delay operation) (Ta=0 to + 60˚C)

Parameter	Symbol	Condition	min	typ	max	Unit
Shift register clock frequency	f_C	See drive timing diagram (3) f_C=1/2T	0.1	1.0	3.0	MHz
Reset clock frequency (=data rate)	f_R	See drive timing diagram (3) f_R=1/2T	0.1	1.0	3.0	MHz
Shift register clock rise time	t_{Cr}	See drive timing diagram (3)	0	20	50	ns
Shift register clock fall time	t_{Cf}		0	20	50	ns
Vertical transfer clock rise time	t_{Vr}	$ø_{SG1}$ and $ø_V$ should be the same timing. See drive timing diagram (1)	0	15	50	ns
Vertical transfer clock fall time	t_{Vf}		0	15	50	ns
Vertical transfer clock pulse width	t_{VW}		5	10	50	µs
Shift clock 1 rise time	t_{SG1r}	See drive timing diagram (1)	0	15	50	ns
Shift clock 1 fall time	t_{SG1f}		0	15	50	ns
Shift clock 1 set up time	t_{SG1s}		0.5	1.0	2.0	µs
Shift clock 1 pulse width	t_{SG1w}		5	10	50	µs
Shift clock 2 rise time	t_{SG2r}	See drive timing diagram (1)	0	15	50	ns
Shift clock 2 fall time	t_{SG2f}		0	15	50	ns
Shift clock 2 set up time	t_{SG2s}		0.5	1.0	2.0	µs
Shift clock 2 pulse width	t_{SG2w}		5	10	50	µs
Shift clock 2 hold time	t_{SG2h}		0	1	2	µs
Reset clock rise time	t_{Rr}	See drive timing diagram (3)	0	10	20	ns
Reset clock fall time	t_{Rf}		0	10	20	ns
Reset clock set up time	t_{Rs}		0.7T	—	—	ns
Reset clock pulse width	t_{Rw}		100	200	—	ns
Reset clock hold time	t_{Rh}		10	125	—	ns

• Timing conditions (during 1-line delay operation) (Ta=0 to + 60˚C)

Parameter	Symbol	Condition	min	typ	max	Unit
Shift register clock frequency	f_C	See drive timing diagram (3) f_C=1/2T	0.1	1.0	3.0	MHz
Reset clock frequency (=data rate)	f_R	See drive timing diagram (3) f_R=1/2T	0.1	1.0	3.0	MHz
Shift register clock rise time	t_{Cr}	See drive timing diagram (3)	0	20	50	ns
Shift register clock fall time	t_{Cf}		0	20	50	ns
Vertical transfer clock rise time	t_{Vr}	$ø_{SG1}$ and $ø_V$ should be the same timing. See drive timing diagram (2)	0	15	50	ns
Vertical transfer clock fall time	t_{Vf}		0	15	50	ns
Vertical transfer clock set up time	t_{Vs}		0.5	1.0	2.0	µs
Vertical transfer clock pulse width	t_{Vw}		5	10	50	µs
Vertical transfer clock hold time	t_{Vh}		0	1	2	µs
Shift clock 1 rise time	t_{SG1r}	See drive timing diagram (2)	0	15	50	ns
Shift clock 1 fall time	t_{SG1f}		0	15	50	ns
Shift clock 1 pulse width	t_{SG1w}		5	10	50	µs
Shift clock 2 rise time	t_{SG2r}	See drive timing diagram (2)	0	15	50	ns
Shift clock 2 fall time	t_{SG2f}		0	15	50	ns
Shift clock 2 set up time	t_{SG2s}		0.5	1.0	2.0	µs
Shift clock 2 pulse width	t_{SG2w}		5	10	50	µs
Reset clock rise time	t_{Rr}	See drive timing diagram (3)	0	10	20	ns
Reset clock fall time	t_{Rf}		0	10	20	ns
Reset clock set up time	t_{Rs}		0.7T		—	ns
Reset clock pulse width	t_{Rw}		100	200	—	ns
Reset clock hold time	t_{Rh}		100	125	—	ns

■ Electrical Characteristics

• Clock input capacitance (Ta=–20 to + 60˚C)

Parameter	Symbol	Condition	min	typ	max	Unit
CCD Shift register clock input capacitance	C_1, C_2	V_{IN}=5V f=1MHz	—	200	—	pF
Vertical transfer clock input capacitance	C_V		—	100	—	pF
Reset clock input capacitance	C_{RS}		—	20	—	pF
Shift clock input capacitance	C_{SG1}, C_{SG2}		—	100	—	pF

• DC characteristics

Parameter	Symbol	Condition	min	typ	max	Unit
Power supply current	I_{DD}	V_{DD}= +12V	—	10	20	mA

• AC characteristics

Parameter	Symbol	Condition	min	typ	max	Unit
Signal output delay time	t_{OS}	(a reference value)	—	50	—	ns

■ Optical Characteristics

<Inspection conditions>

- Ta=25˚C, V_{DD}=12V, $V_{øH}$=V_{VH}=V_{SH}=V_{RH}=5V (pulse), f_C=f_R=1MHz, T_{int} (accumulation time)=10ms
- Light source: Daylight fluorescent lamp with IR/UV cutting filter
- Optical system: A slit with an aperture dimensions of 20mm × 20mm is used at a distance of 200mm from the sensor (equivalent to F=10).
- Load resistance = 100k Ohms
- These specifications apply to the 512 valid R and G pixels and the 1024 valid G pixels excluding the dummy pixels D1 to D8.

Parameter	Symbol	Condition	min	typ	max	Unit
Responsivity	R_R	Note 1	0.70	0.95	1.20	V/lx · s
	R_G	Note 1	1.40	1.80	2.20	
	R_B	Note 1	0.90	1.20	1.50	
Photo response non-uniformity	PRNU	Note 2	—	6	15	%
Saturation output voltage	V_{SAT}	Note 3	650	800	—	mV
Saturation exposure	SE_R	Note 4	0.67	0.84	—	lx · s
	SE_G	Note 4	0.36	0.44	—	
	SE_B	Note 4	0.53	0.67	—	
Dark signal output voltage	V_{DRK1}	OS1, Dark condition, see Note 5	—	0.5	1.0	mV
	V_{DRK2}	OS2, Dark condition, see Note 5	—	1.0	2.0	
Dark signal output non-uniformity	$DSNU_1$	OS1, Dark condition, see Note 6	—	0.1	2.0	mV
	$DSNU_2$	OS2, Dark condition, see Note 6	—	0.2	4.0	
Shift register total transfer efficiency	STTE		92	99	—	%
Dynamic range	DR	Note 7	—	800	—	

Note 1) Responsivity (R)
This is the value obtained by dividing the average output voltage (V) of the all pixels by the exposure (lx· s).
The exposure (lx· s) is the product of the illumination intensity (lx) and the accumulation time (s).
Since the responsivity changes with the spectral distribution of the light source used, care should be taken when using a light source other than the daylight type fluorescent lamp specified in the inspection conditions.

Note 2) Photo response non-uniformity (PRNU)
This is defined by the following equation where X_{ave} is the average output voltage of the valid pixels of each of the colors R, G, and B, and Δx is the difference between the output voltage of the maximum (or minimum) output pixel and X_{ave}, when the photodetector region is illuminated with light of a uniform illumination intensity distribution.

$$PRNU = \frac{\triangle x}{X_{ave}} \times 100\ (\%)$$

The incident light intensity shall be 50% of the standard saturation llight intensity.

■ Optical Characteristics (continued)

Note 3) Saturation output voltage:
This is the output voltage at the point beyond which it is not possible to maintain the linearity of the photoelectric conversion characteristics as the exposure is increased. (The exposure at this point is called the saturation exposure.)

Note 4) Saturation Exposure (SE)
This is the exposure beyond which it is not possible to maintain the linearity of the output voltage as the exposure is increased. When designing the equipment using these devices, make sure that the incident light exposure is set with sufficient margin so that the CCD never gets saturated.

Note 5) Dark signal output voltage (V_{DRK})
This is defined as the average of the output from all the valid pixels in the dark condition at Ta=25˚C, T_{int}=10ms. Normally, the dark signal output voltage gets doubled for every 8 to 10˚C increase in Ta and is proportional to T_{int}. The dark signal output voltage (V_{DRK2}) on the OS_2 side will be larger than the dark signal output voltage (V_{DRK1}) on the OS_1 side because there is a delay memory on the OS_2 side.

Note 6) Dark signal non-uniformity (DSNU)
This is defined as the difference between the maximum value among the output voltages of the all valid pixels at Ta=25˚Cand T_{int}=10ms and V_{DRK}.

Note 7) Dynamic range (DR)
This is defined by the following equation.

$$DR = \frac{V_{SAT}}{V_{DRK}}$$

Since the dark signal output voltage is proportional to the accumulation time, the dynamic range becomes wider when the accumulation time is shorter.

■ Pin Descriptions

Pin No.	Symbol	Pin name	Condition
1	NC	Non connection	
2	NC	Non connection	
3	OS_1	Signal output 1	Green pixel output
4	DS_1	Compensation output 1	
5	V_{SS}	Ground	
6	$ø_R$	Reset clock	
7	$ø_1$	CCD clock (Phase 1)	
8	$ø_{SG1}$	CCD shift register clock 1	
9	V_{SS}	Ground	
10	V_{SS}	Ground	
11	NC	Non connection	
12	NC	Non connection	
13	NC	Non connection	
14	$ø_V$	Vertical transfer clock	
15	$ø_{SG2}$	Shift clock gate 2	
16	$ø_2$	CCD clock (Phase 2)	
17	NC	Non connection	
18	V_{DD}	Power supply	
19	DS_2	Compensation output 2	
20	OS_2	Signal output 2	Red and Blue pixel output
21	NC	Non connection	
22	NC	Non connection	

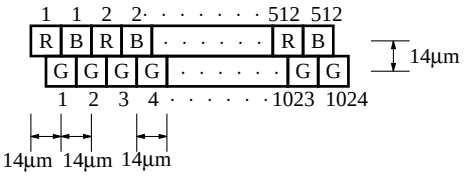
Note) Connect all NC pins externally to V_{SS} (GND).

■ Construction of the Image Sensor

The MN3674 can be made up of the three sections of—a) photo detector region, b) CCD transfer region (shift register), and c) output region.

a) Photo detector region

- The photoelectric conversion device consists of an 11µm floating photodiode and a 3µm channel stopper (isolation region) per pixel, and such pixels are arranged in a linear row with a pitch of 14µm along the main scanning direction.
- The R-B row has 512 pixels each of the red and blue colors arranged alternatingly, and the G row has1024 pixels. The R-B row and G row are placed with a spacing of one line (14µm) along the sideways scanning direction. The pixels of the G row are displaced by half the pixel pitch (7µm) relative to the pixels of the R-B row in the main scanning direction.



- A one line analog delay memory is built in the chip in order to compensate for the difference in the positions of the R-B and G rows in the sideways scanning direction.
- The photodetector window is a rectangle of dimensions 9µm (Horizontal) × 11µm (Vertical), and the areas other than the photodetector window are optically shielded.
- The photodetector region has a total of 32 optically shielded (black reference) pixels that can be used as the black level reference, with 16 pixels each for the R-B row and the G row.

b) CCD Transfer region (shift register)

- The signal charges obtained by photoelectric conversion are transferred to the CCD transfer regions of the respective colors during the period when the shift gate ($ø_{SG}$) is at the High level. The signal charges transferred to this analog shift register are successively transferred to the output region.
- A buried type CCD that can be driven by a two phase clock ($ø_1$, $ø_2$) is used for the analog shift register.

c) Output region

- The signal charge transferred to the output region is first sent to the charge to voltage conversion region where it is converted into a voltage level corresponding to the amount of the signal charge, and then output after impedance conversion in a two stage source follower amplifier.
- The DC level component not containing the optical signal and the clock noise component are output at the DS pin.
- It is possible to obtain a signal with a high S/N ratio with reduced clock noise, etc., by carrying out differential amplification of the OS and DS outputs externally.

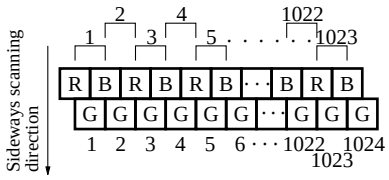
■ 1-Line delay analog memory

- In order to compensate for the distance between the photodiode rows for the R, B colors and the G color, the device has a built in analog memory that can store the signals of one line. It is possible to select either to use or not use the delay memory by the timings of the pulses $ø_V$, $ø_{SG1}$, and $ø_{SG2}$, and the two types of read out operation of 512 pixel operation and pseudo 1024 pixel operation can be obtained accordingly.

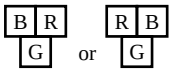
(1) 512-pixel operation (no delay memory)

is taken as one pixel thereby making this device a 512-pixel color CCD.
(Each pixel of the color sensor will be a parallelogram of 28µm (horizontal) × 28µm (vertical).)

(2) Pseudo 1024-pixel operaation (delay memory is used)



A 1-line delay operation and interpolation signal processing shown in the figure at left are made for the R-B colors.

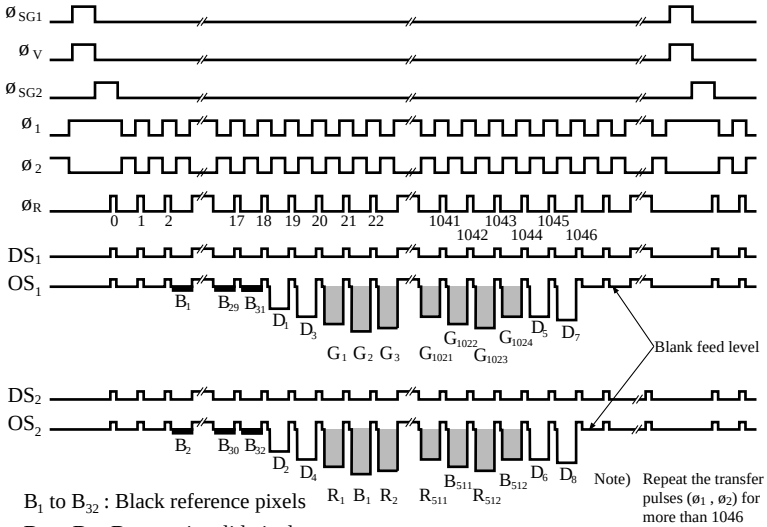


becomes one pixel during color sensing operation.

* Since the signal from the R-B row gets delayed, configure the optical system and mechanisms so that the sideways scanning is done first from the R-B row. The R-B row and the G row of the same line will be read out due to the one line delay.
The weighted center of one color pixel can be considered to be at the position of the G pixel.

■ Timing Diagram

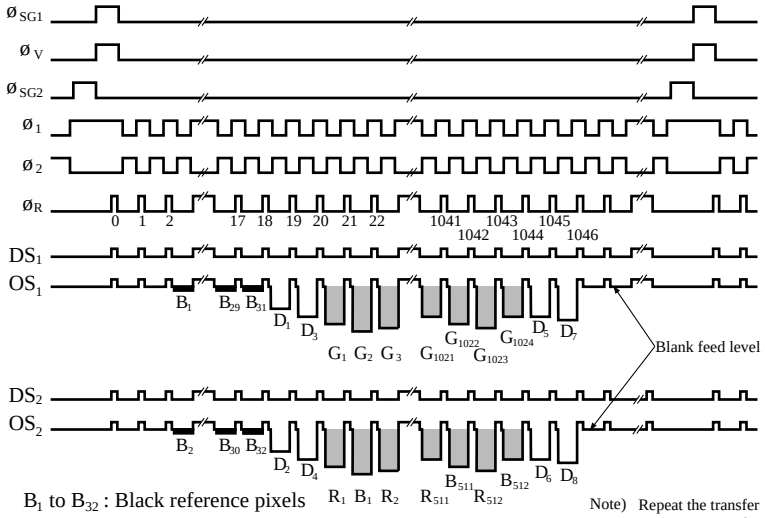
• I/O timing (1) (without 1-line delay operation)



B_1 to B_{32} : Black reference pixels

D_1 to D_8 : Dummy invalid pixels

• I/O timing (2) (during 1-line delay operation)

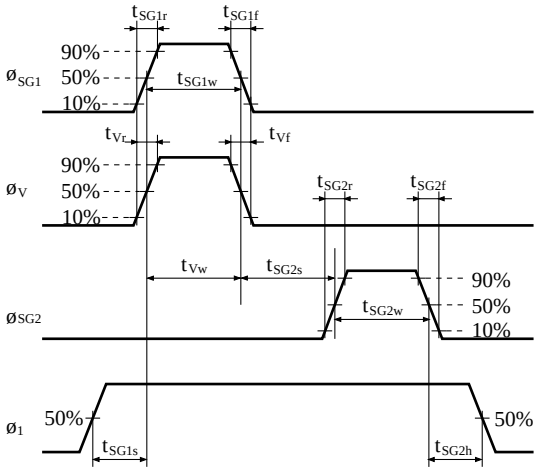


B_1 to B_{32} : Black reference pixels

D_1 to D_8 : Dummy invalid pixels

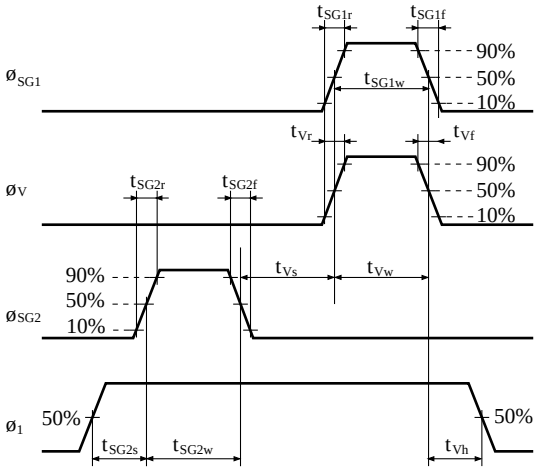
* OS_2 outputs the previous line signal.

• Drive timing (1) (read-out during no 1-line delay operation)



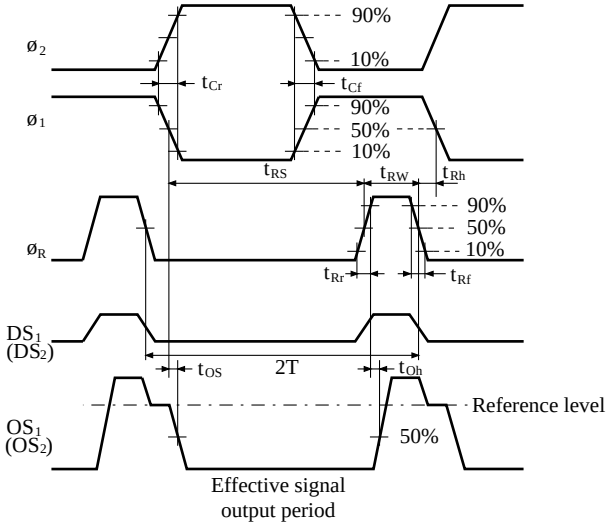
Note) Make sure that the timings of $ø_{SG}$ and $ø_V$ are identical.
(If these are not identical, the accumulation time gets shifted and hence the data on the same line cannot be obtained.)

• Drive timing (2) (read-out during 1-line delay operation)



Note) Make sure that the timings of $ø_{SG}$ and $ø_V$ are identical.
(If these are not identical, the accumulation time gets shifted and hence the data on the same line cannot be obtained.)

• Drive timing (3) (during repeated pattern)



■ Graphs and Characteristics

Spectral Response Characteristics