DATA SHEET

SUNPLUS

SPLC563A

320-Channel Low-Voltage Segment Driver for Dot-Matrix STN Liquid Crystal Display

MAY. 16, 2005

Version 1.0

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320-CHANNEL LOW-VOLTAGE SEGMENT DRIVER FOR DOT-MATRIX STN LIQUID CRYSTAL DISPLAY

1. GENERAL DESCRIPTION

The SPLC563A is a 320-channel segment driver for driving a dot-matrix STN liquid-crystal panel at a low voltage. The driver can also correspond to 240-channel output by switching mode. It operates at a low voltage: a liquid-crystal drive voltage of 5.0V and a logic drive voltage of 3.0V, and is used together with common driver SPLC564A. The package, which adopts a flexible TCP, can be applied to various liquid crystal panels.

2. FEATURES

- Display duty: Up to 1/240
- Liquid crystal drive voltage: 2.6V to 5.5V
- Number of liquid crystal drive circuits: 320 circuits
- Operating voltage: 2.5V to 5.5V
- Number of data bits: 4 or 8 bits
- Shift clock speed: 8.0MHz max @ 5.0V, 6.5MHz max @ 3.0V
- Together with the common drivers SPLC564A
- Low power consumption
- Switching output mode: 320 output mode, 240 output mode
- Display-off function
- Flexible TCP
- Automatic generation of chip-enable signals
- Standby function

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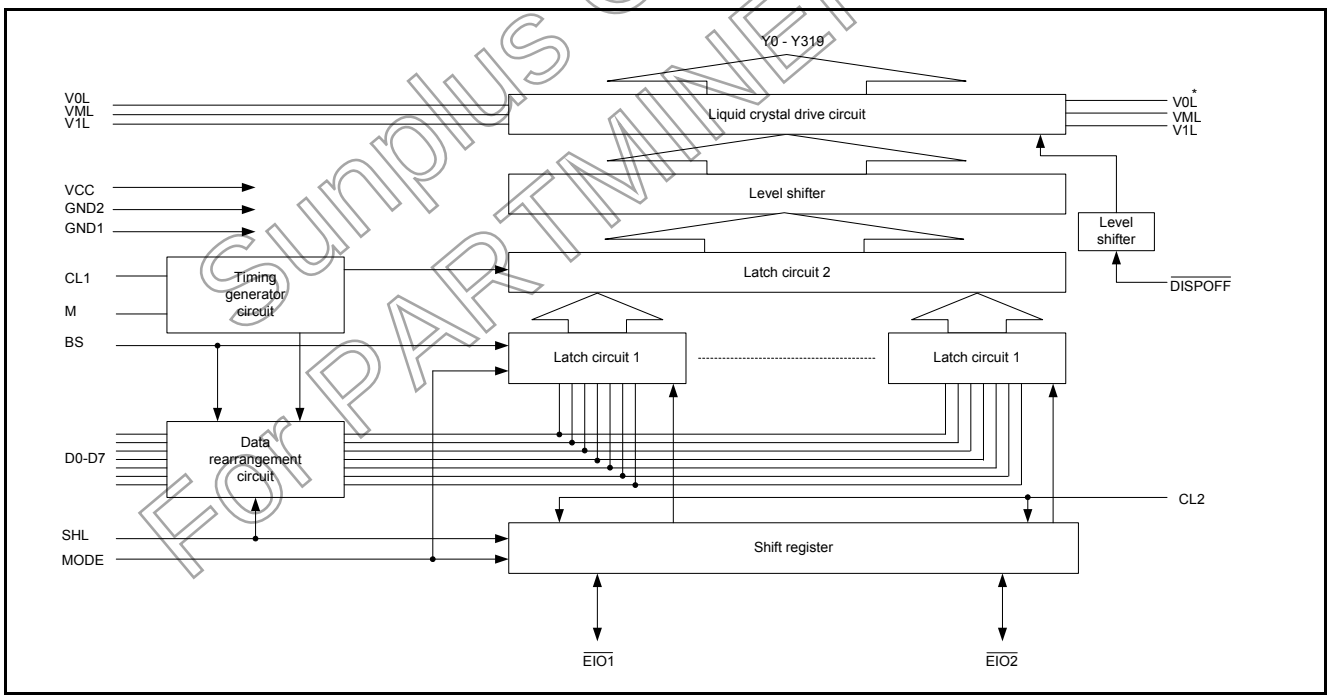
3. BLOCK DIAGRAM



Note: PINs V0L, VML, and V1L are internally connected to pins V0R, VMR, and V1R, respectively.

3.1. Block Function Descriptions

3.1.1. Liquid crystal drive circuit

Selects and outputs the liquid crystal drive level V0, VM, or V1 by $\overline{\text{DISPOFF}}$ and a combination of data for latch circuit 2 and signal M.

3.1.2. Level shifter

Converts logic signals to liquid crystal drive signals.

3.1.3. Latch circuit 2

320-bit latch circuit, which latches the data of latch circuits 1 at the fall of CL1 and outputs the data to the level shifter.

3.1.4. Latch circuit 1

4/8-bit parallel data latch circuit, which latches display data D0 to D7 according to signals transmitted from the shift register.

3.1.5. Shift register

80-bit shift register, which generates data-capture signals for latch circuits 1 at the fall of CL2.

3.1.6. Data rearrangement circuit

Inverts the order of data output crosswise.

3.1.7. Timing generator circuit

The timing generator circuit generates data latch pulses for latch circuit2 and changes pulse the LCD drive outputs to AC.

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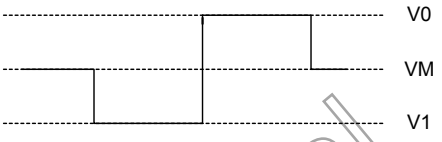
4. SIGNAL DESCRIPTIONS

<table>
<tr><th>Classification</th><th>Symbol</th><th>PAD No.</th><th>Connected to</th><th>I/O</th><th>Functions</th></tr>
<tr><td rowspan="2">Power supply</td><td>VCC
GND1
GND2</td><td>347
353
385</td><td>VCC
GND</td><td>-</td><td>VCC - GND: Power supply for logic.</td></tr>
<tr><td>V0L
V0R
VML
VMR
V1L
V1R</td><td>342
391
339
394
345
388</td><td>V0L
V0R
VML
VMR
V1L
V1R</td><td>Input</td><td>Liquid crystal drive level power supply
 
</td></tr>
<tr><td rowspan="8">Control signal</td><td>CL1</td><td>379</td><td>Clock 1</td><td>Input</td><td>Latch signal of display data: A liquid crystal drive signal corresponding to display data is output at the fall of CL1.</td></tr>
<tr><td>CL2</td><td>377</td><td>Clock 2</td><td>Input</td><td>Capture signal of display data: Display data is captured at the fall of CL2.</td></tr>
<tr><td>M</td><td>381</td><td>M</td><td>Input</td><td>A.C. signal of liquid crystal drive output</td></tr>
<tr><td>D0 to D7</td><td>361, 369
363, 371
365, 373
367, 375</td><td>DATA0 to DATA7</td><td>Input</td><td><table><tr><th>Display data</th><th>Liquid crystal drive output</th><th>Liquid crystal drive output</th></tr><tr><td>1 (VCC level)</td><td>Selected level</td><td>ON</td></tr><tr><td>0 (GND level)</td><td>Not-selected level</td><td>OFF</td></tr></table></td></tr>
<tr><td>SHL</td><td>355</td><td>Shift Left</td><td>Input</td><td>Control signal for inverting the order of data output (see the following page)</td></tr>
<tr><td>$\overline{EIO1}$</td><td>357</td><td>Enable IO1</td><td>I/O</td><td><table><tr><th>SHL</th><th>$\overline{EIO1}$</th><th>$\overline{EIO2}$</th></tr><tr><td>GND</td><td>Enable input</td><td>Enable Output</td></tr><tr><td>VCC</td><td>Enable output</td><td>Enable input</td></tr></table></td></tr>
<tr><td>$\overline{EIO2}$</td><td>383</td><td>Enable IO2</td><td>I/O</td><td>Enable input: The enable input of the first IC is connected to the GND and another is connected to the enable output of the second IC.
Enable output: Connected to the enable input of the second IC at cascade output.</td></tr>
<tr><td>$\overline{DISPOFF}$</td><td>359</td><td>Disp off</td><td>Input</td><td>Grounding $\overline{DISPOFF}$ sets liquid crystal drive output Y0 - Y319 to the VM level.</td></tr>
<tr><td>BS</td><td>351</td><td>Bus Select</td><td>Input</td><td>Switches the number of input bits for the display data.<table><tr><td>VCC</td><td>8-bit input mode</td></tr><tr><td>GND</td><td>4-bit input mode (Captures data from D0 - D3. At this time, connect D4 - D7 to the GND.)</td></tr></table></td></tr>
<tr><td>MODE</td><td>349</td><td>MODE</td><td>Input</td><td>Switches the number of input bits for the display data.<table><tr><td>VCC</td><td>320 output mode</td></tr><tr><td>GND</td><td>240 output mode (Y40 - Y279 are valid output. The other 80 pins output the not-selected-level signals synchronized every time; release these pins.)</td></tr></table></td></tr>
</table>

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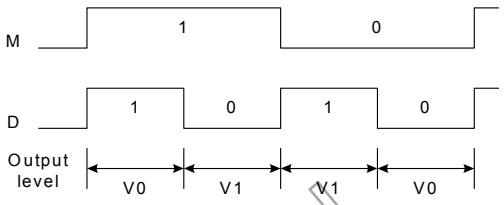
Classification	Symbol	PAD No.	Connected to	I/O	Functions
Liquid crystal drive output	Y0 to Y319	328 to 9	Y0 to Y319	Output	Liquid crystal drive output: Selects and outputs level V0 or V1 according to the combination of the M signal and display data when $\overline{\text{DISPOFF}}$ is connected to VCC. 

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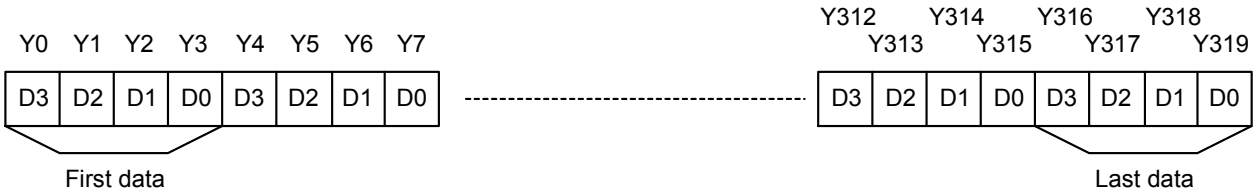
5. REARRANGING OUTPUT DATA (SHL)

SHL = GND, BS = GND



Enable input: $\overline{EIO1}$

Enable output: $\overline{EIO2}$

SHL = VCC, BS = GND

Enable input: $\overline{EIO2}$

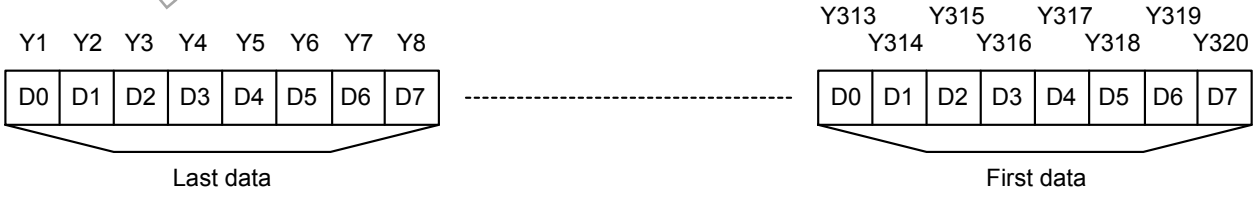
Enable output: $\overline{EIO1}$

SHL=GND, BS = VCC

Enable input: $\overline{EIO1}$

Enable output: $\overline{EIO2}$

SHL = VCC, BS = VCC



Enable input: $\overline{EIO2}$

Enable output: $\overline{EIO1}$

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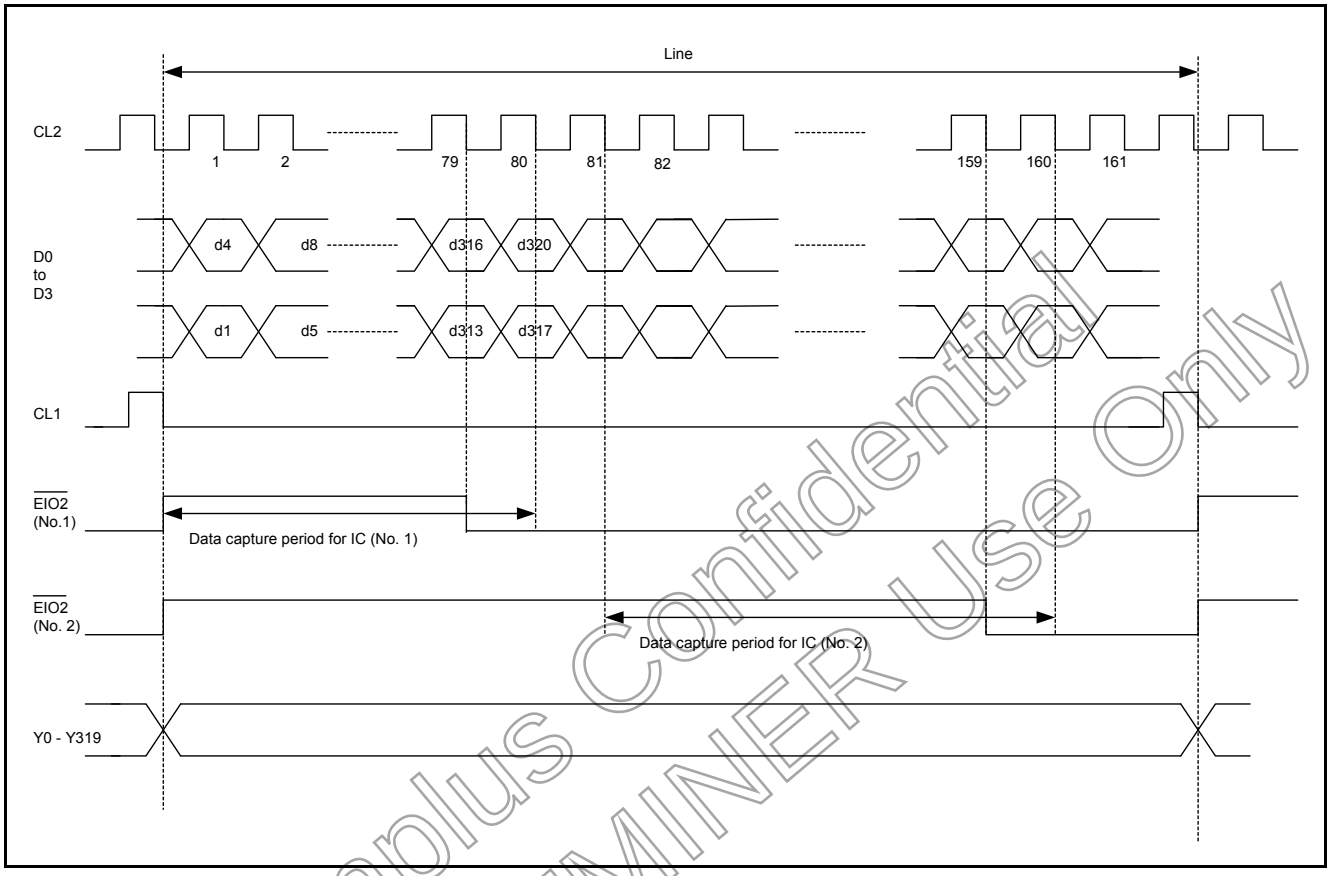
6. OPERATION TIMING

6.1. 4-Bit Capture Mode (1line, 640 dots)



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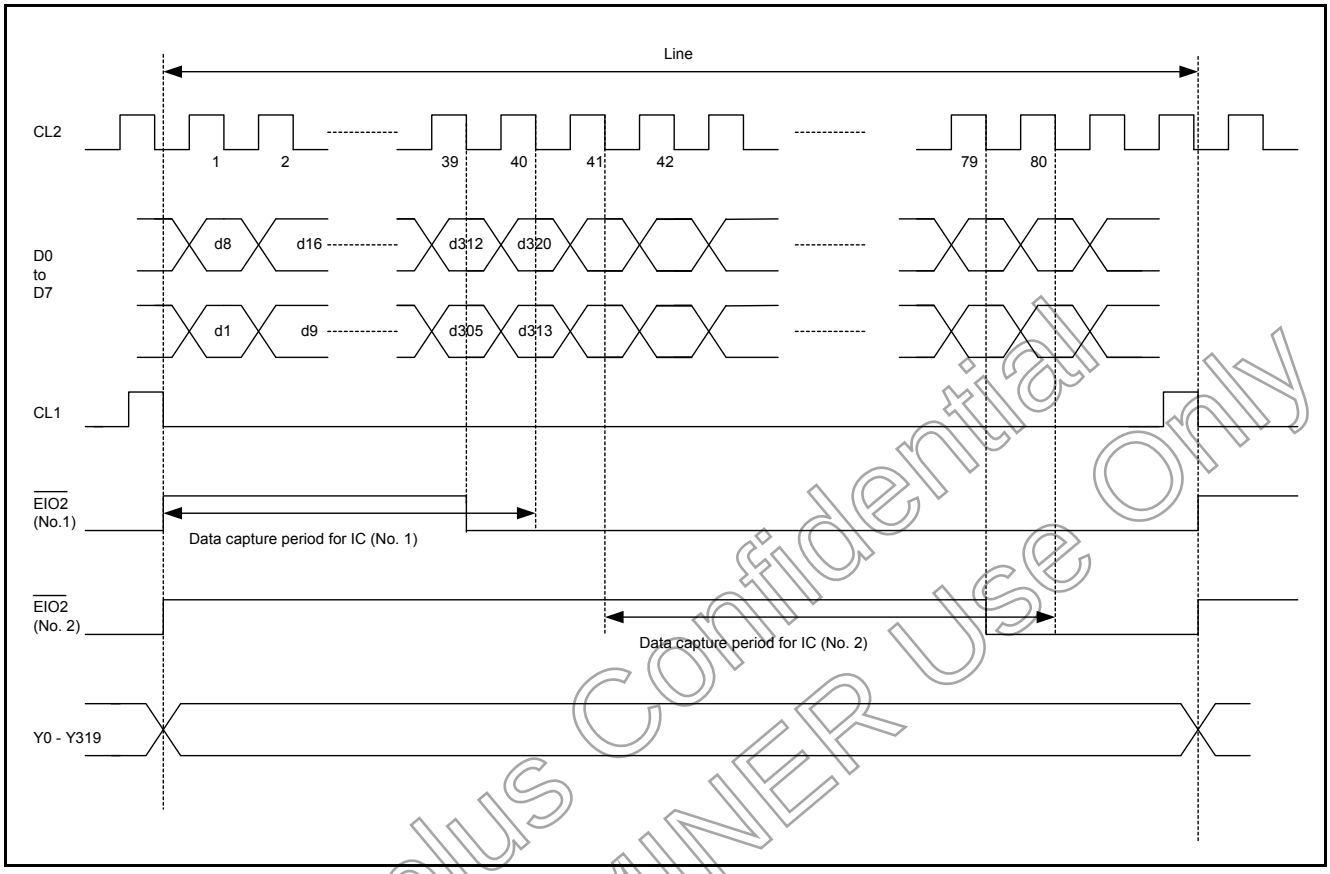
BS = GND (4-bit capture mode)

During the data standby state when the data capture operation enable signal is low (SHL = GND: $\overline{EIO1}$), the next data capture clock (CL2) cancels the standby state. The 4-bit data is captured at the fall of CL2. When 316 bits are captured, the enable signal becomes the GND level (SHL = GND: $\overline{EIO2}$). When 320 bits are captured, the operation automatically stops (the standby state is entered). The second IC is then activated when pin $\overline{EIO2}$ is connected to pin $\overline{EIO1}$ of the second IC.

Data output changes at the fall of CL1.

During SHL = GND, captured data d1 and d320 are output to Y0 and Y319, respectively. During SHL = VCC, data d1 and d320 are output to Y319 and Y0, respectively.

6.2. 8-Bit Capture Mode (1line, 640 dots)



BS = VCC (8-bit capture mode)

The 8-bit display data is captured at the fall of CL2. Other basic operations are the same as those of the 4-bit capture mode.

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7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

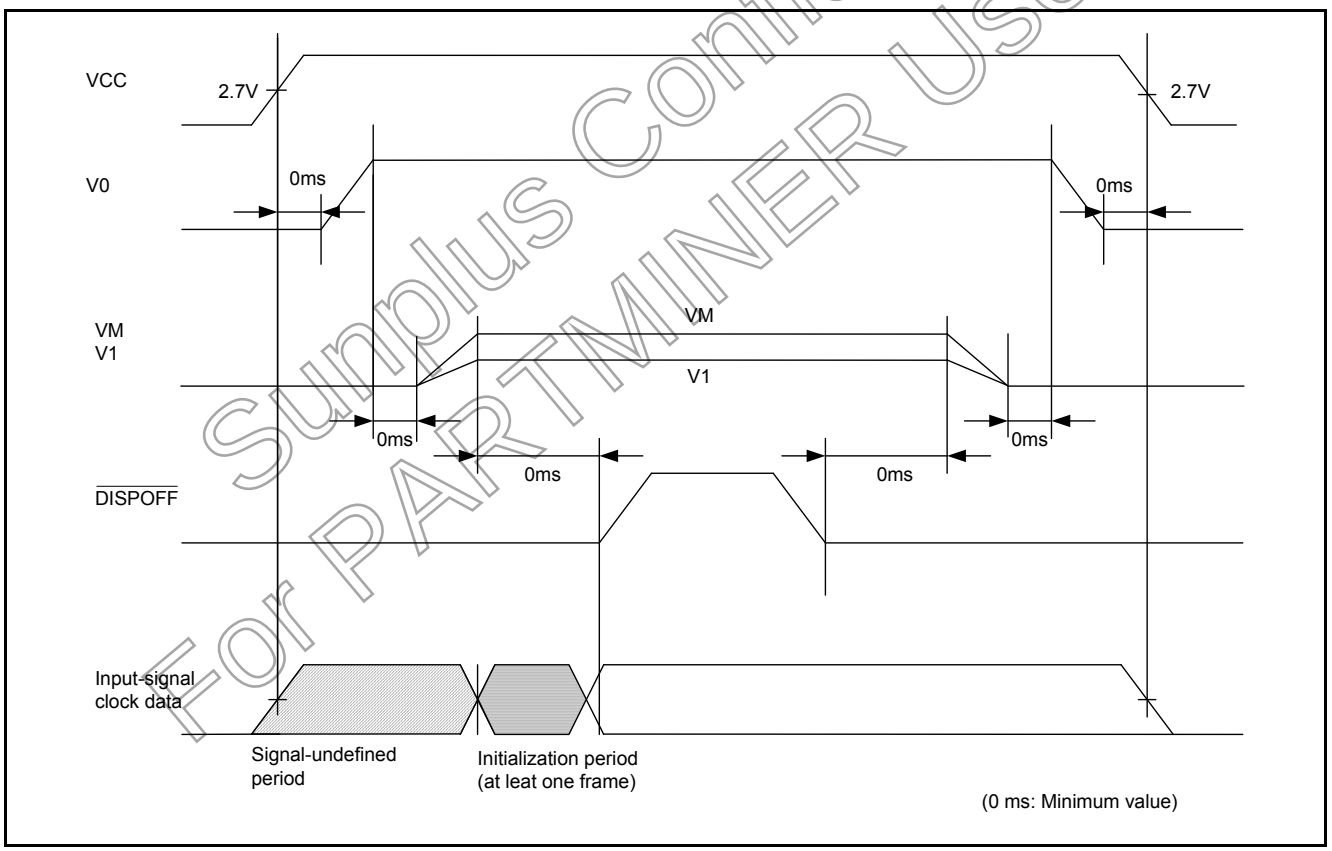
Item	Symbol	Rating	Unit	Notes
Power supply voltage for logic circuits	VCC	– 0.3 to + 7.0	V	1, 4
Power supply voltage for LCD drive circuits	V_0	– 0.3 to + 7.0	V	1, 4
Input voltage 1	VT1	– 0.3 to VCC + 0.3	V	1, 2
Input voltage 2	VT2	– 0.3 to V_0 + 0.3	V	1, 3, 4
Operating temperature	T_{OPR}	– 30 to +75	°C	
Storage temperature	T_{STG}	– 55 to +110	°C	

Note1: Potential from the GND

Note2: Applied to pins SHL, $\overline{EIO1}$, $\overline{EIO2}$, $\overline{DISPOFF}$, D0 to D7, CL1, CL2, M, BS, and MODE.

Note3: Applied to VML, VMR, V1L, and VMR.
Operating the LSI in excess of the absolute maximum rating will result in permanent damage. Use the LSI observing electrical characteristic conditions in normal operation. Exceeding the conditions will cause malfunctions or will affect LSI reliability.

Note4: Conform to the following turn-on/off sequence of the power and signals. Otherwise, the LSI will malfunction or will be permanently damaged. In addition, LSI reliability will be affected.



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7.1.1. Turning on the power

1). Turn on the power in the order of GND- VCC, GND-V0, and VM/V1. Then, ground the $\overline{\text{DISPOFF}}$ pin.

2). The LCD forcibly outputs the VM level by the DISPOFF function.

3). Even if an input signal is disturbed immediately after VCC is applied, the DISPOFF function has priority.

4). Input the specific signal to initialize registers in the driver. The initialization period must be at least one frame.

5). The preparation of normal display is completed. Input the VCC level to the $\overline{\text{DISPOFF}}$ pin to cancel the DISPOFF function. At this time, the level of pins V0, VM, and V1 must rise to the specific potential.

7.1.2. Turning off the power

The procedure is basically the reverse for turning on the power.

1). Ground the $\overline{\text{DISPOFF}}$ pin.

2). Turn off the liquid crystal power in the order of VM/V1 and GND-V0.

3). Ground VCC and an input signal.
At this time, the level of pins V0, VM, and V1 must fall to 0 V. Since the DISPOFF function stops when VCC falls to 0 V, the LCD may output a level other than VM. Therefore, a display failure may occur when the power is turned off or on.

7.2. DC Characteristics 1

(V_{CC} = 2.5 to 4.5V, V0 - GND = 2.6V to 5.5V, T_A = -30°C to +75°C)

Item	Symbol	Pins	Min.	Typ.	Max.	Unit	Test Condition	Notes
Input high voltage	V_{IH}	CL1, CL2, SHL, M, $\overline{\text{EIO1}}$, $\overline{\text{EIO2}}$	0.8 x VCC	-	VCC	V		
Input low voltage	V_{IL}	MODE, $\overline{\text{DISPOFF}}$, D0 to D7, BS	0	-	0.2 x VCC	V		
Output high voltage	V_{OH}	$\overline{\text{EIO1}}$, $\overline{\text{EIO2}}$	VCC - 0.4	-	-	V	I_{OH} = -0.4mA	
Output low voltage	V_{OL}	$\overline{\text{EIO1}}$, $\overline{\text{EIO2}}$	-	-	0.4	V	I_{OL} = 0.4mA	
Vi-Yj on resistance	R_{ON}	Y0 to Y319, V0L, R	-	0.7	2.0	KΩ	I_{ON} = 150μA	1
		Y0 to Y319, VML, R	-	2.0	3.0	KΩ		
		Y0 to Y319, V1L, R	-	0.7	2.0	KΩ		
Input leakage current 1	I_{IL1}	CL1, CL2, SHL, M, $\overline{\text{EIO1}}$, $\overline{\text{EIO2}}$, MODE, $\overline{\text{DISPOFF}}$, D0 to D7, BS	-5.0	-	5.0	μA	VIN = VCC to GND	
Input leakage current 2	I_{IL2}	VML, R, V1L, R	-25	-	25	μA	VIN = V0 to GND	
Current consumption 1	I_{CC}	VCC	-	150	300	μA	VCC = 3.3V V0 = 2.7V	2
Current consumption 2	I_{V0}	V0L, R	-	60	200	μA	f_{CL2} = 3.5MHz f_{CL1} = 19.2KHz	
Current consumption	I_{ST}	VCC	-	50	100	μA	fM = 1.5KHz	2,3

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7.3. DC Characteristics 2

(VCC = 4.5 to 5.5V, V0 - GND = 2.6V to 5.5V, T_A = -30°C to +75°C)

Item	Symbol	Pins	Min.	Typ.	Max.	Unit	Test Condition	Notes
Input high voltage	V_{IH}	CL1, CL2, SHL, M, $\overline{EIO1}$, $\overline{EIO2}$	0.8 x VCC	-	VCC	V		
Input low voltage	V_{IL}	MODE, $\overline{DISPOFF}$, D0 to D7, BS	0	-	0.2 x VCC	V		
Output high voltage	V_{OH}	$\overline{EIO1}$, $\overline{EIO2}$	VCC - 0.4	-	-	V	I_{OH} = -0.4mA	
Output low voltage	V_{OL}	$\overline{EIO1}$, $\overline{EIO2}$	-	-	0.4	V	I_{OL} = 0.4mA	
Vi-Yj on resistance	R_{ON}	Y0 to Y319, V0L, R	-	0.7	2.0	KΩ	I_{ON} = 150μA	1
		Y0 to Y319, VML, R	-	2.0	3.0	KΩ		
		Y0 to Y319, V1L, R	-	0.7	2.0	KΩ		
Input leakage current 1	I_{IL1}	CL1, CL2, SHL, M, $\overline{EIO1}$, $\overline{EIO2}$, MODE, $\overline{DISPOFF}$, D0 to D7, BS	-5.0	-	5.0	μA	V_{IN} = VCC to GND	
Input leakage current 2	I_{IL2}	VML, R, V1L, R	-25	-	25	μA	V_{IN} = V0 to GND	
Current consumption 1	I_{CC}	VCC	-	230	450	μA	VCC = 5.0V V0 = 2.7V	2
Current consumption 2	I_{V0}	V0L, R	-	60	200	μA	f_{CL2} = 3.5MHz f_{CL1} = 19.2KHz	
Current consumption	I_{ST}	VCC	-	80	150	μA	fM = 1.5KHz	2,3

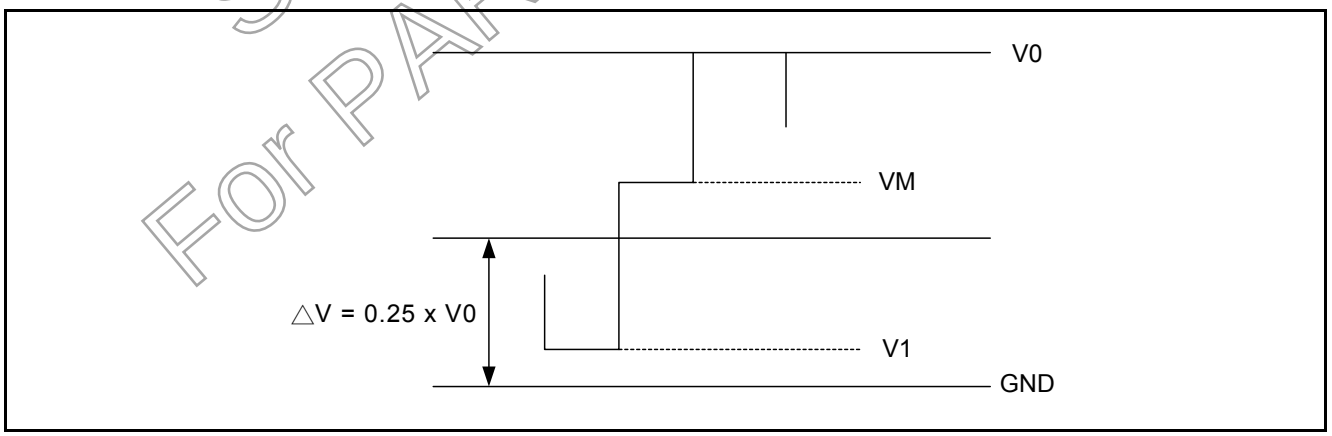
Note1: Resistance between pins Y and V when a load current flows to one of the pins from Y0 to Y319. The following conditions are defined:

V0 - GND = 5.5V

VM = (V0 + V1)/2

V1 = GND + 1.0

The voltage range of the liquid crystal drive level power supply is described. A voltage around the GND is applied to pin V1, and an intermediate voltage of about V0 and V1 is applied to pin VM. Use the V1 in the range of DV = 0.25 x V0, in which the impedance Ron of driver output is stable.



Relationship between the driver output waveform and each level voltage.

Note2: A current flowing in the input or output section is excluded. If an input signal is at an intermediate level for the CMOS, a through-current flows in the input circuit and power supply current increases. Therefore, VIH must be at the VCC level and VIL must be at the GND level.

Note3: Current at standby

Note4: The voltage of each signal is shown below.

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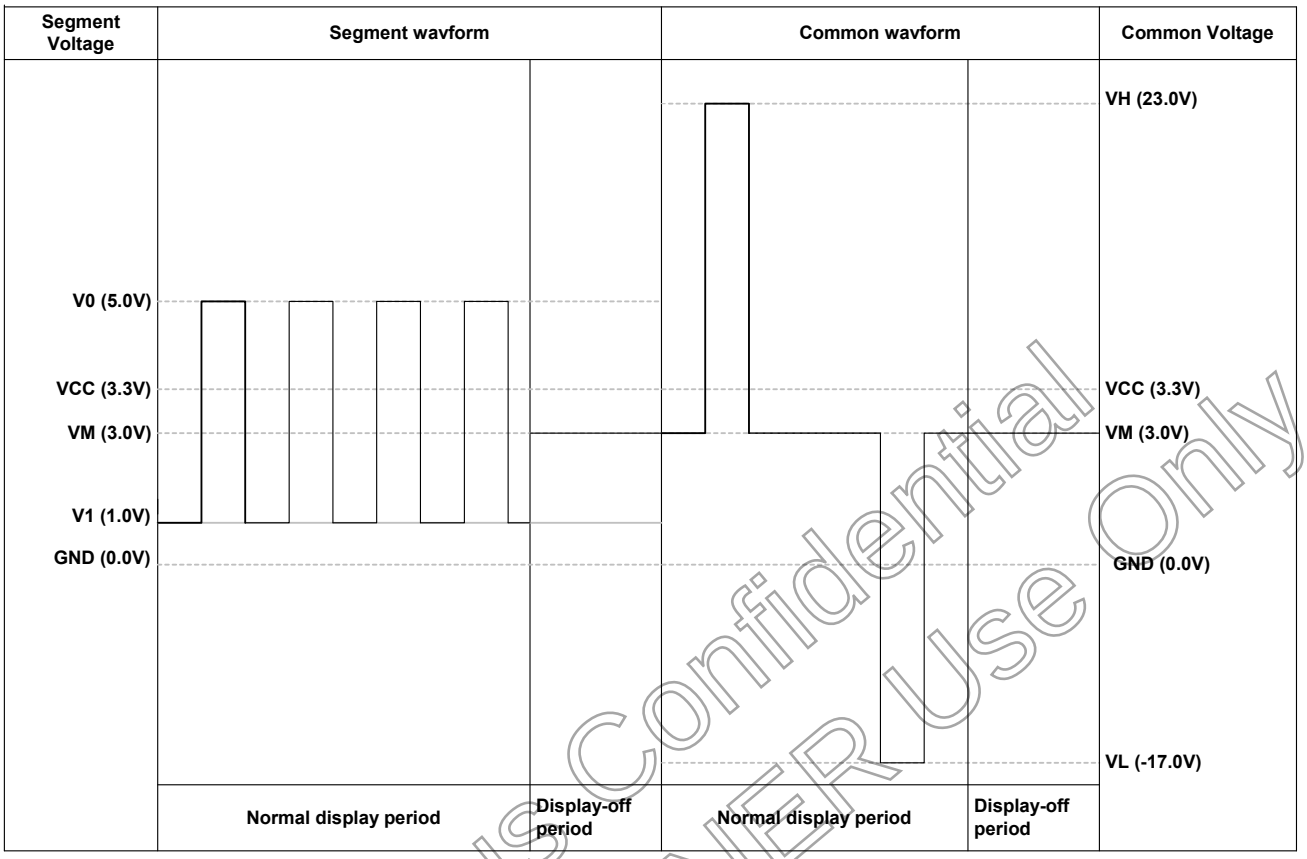

7.4. AC Characteristics 1

(VCC = 2.5V to 4.5V, V0 - GND = 2.6V to 5.5V, T_A = -30°C to +75°C)

Item	Symbol	Pins	Min.	Max.	Unit
Clock cycle time	t_{CYC}	CL2	152	-	ns
Clock high pulse width 1	t_{CWH2}	CL2	65	-	ns
Clock low pulse width 1	t_{CWL2}	CL2	65	-	ns
Clock high pulse width 2	t_{CWH1}	CL1	65	-	ns
Clock setup time	t_{SCL}	CL1, CL2	80	-	ns
Clock hold time	t_{HCL}	CL1, CL2	80	-	ns
Clock rise time	t_r	CL1, CL2	-	30	ns
Clock fall time	t_f	CL1, CL2	-	30	ns
Data setup time	t_{DS}	D0 to D7, CL2	50	-	ns
Data hold time	t_{DH}	D0 to D7, CL2	50	-	ns
M setup time	t_{MS}	M, CL1	20	-	ns
M hold time	t_{MH}	M, CL1	20	-	ns
Output delay time 1	t_{pd1}	CL1, Y0 to Y319	-	1000	ns

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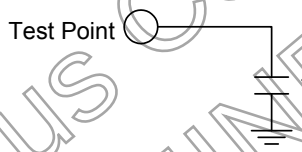
7.5. AC Characteristics 2

(VCC = 4.5V to 5.5V, V0 - GND = 2.6V to 5.5V, T_A = -30°C to +75°C)

Item	Symbol	Pins	Min.	Max.	Unit
Clock cycle time	t_{CYC}	CL2	125	-	ns
Clock high pulse width 1	t_{CWH2}	CL2	45	-	ns
Clock low pulse width 1	t_{CWL2}	CL2	45	-	ns
Clock high pulse width 2	t_{CWH1}	CL1	45	-	ns
Clock setup time	t_{SCL}	CL1, CL2	80	-	ns
Clock hold time	t_{HCL}	CL1, CL2	80	-	ns
Clock rise time	t_4	CL1, CL2	-	20	ns
Clock fall time	t_f	CL1, CL2	-	20	ns
Data setup time	t_{DS}	D0 to D7, CL2	20	-	ns
Data hold time	t_{DH}	D0 to D7, CL2	20	-	ns
M setup time	t_{MS}	M, CL1	20	-	ns
M hold time	t_{MH}	M, CL1	20	-	ns
Output delay time 1	t_{pd1}	CL1, Y0 to Y319	-	1000	ns

Note1: A load must be 10pF or less for EI/O connection between drivers.

Note2: For output delay time 1 and 2, connect the load circuit shown below.



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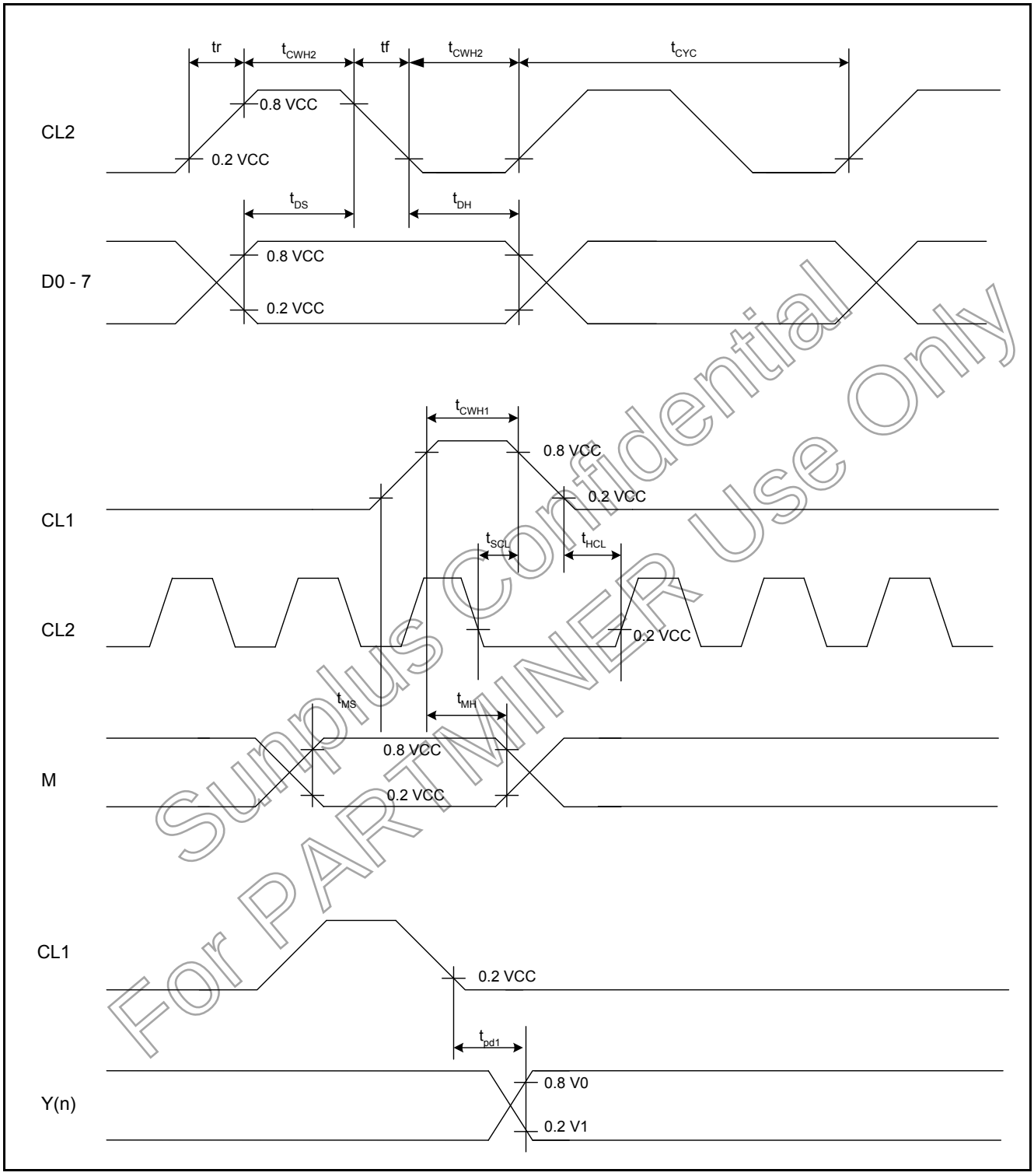

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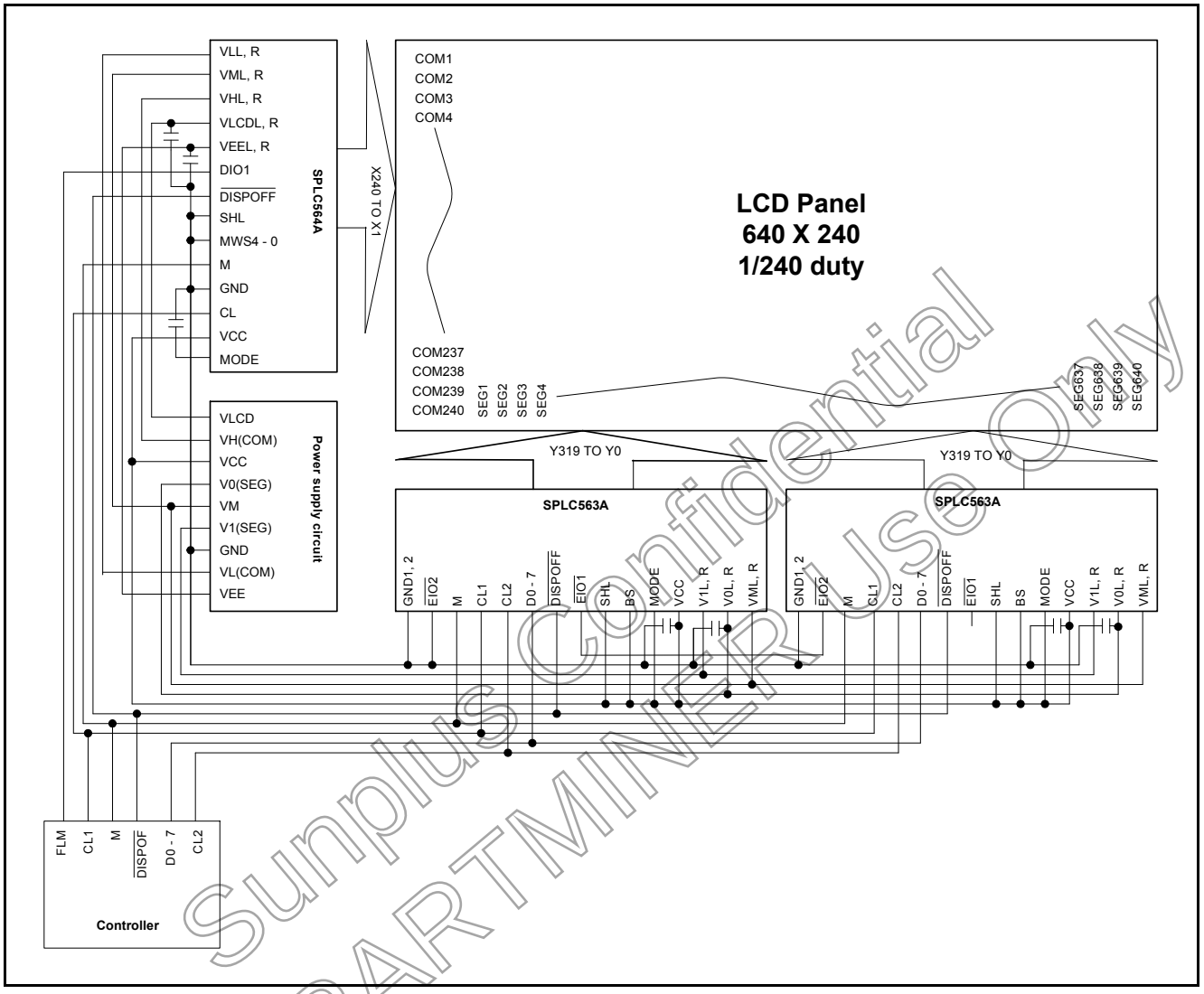
8. APPLICATION CIRCUIT



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Note1: When designing the board, connect a capacitor near the IC to stabilize power supply. Use two capacitors of about 0.1μF for each IC (between VCC and GND, V0 and GND, VLCD and GND, and VEE and GND).

Note2: In addition, for the power supply circuit, connect a capacitor of several μF or several tens of μF between the liquid crystal power supply and GND. For set evaluation, confirm that there is no inversion of liquid crystal drive power supply and level power supply in the period between when the liquid crystal drive power supply is turned on and when it is turned off.

Note3: Configuring the LCD panel using the SPLC563A when using the select COMMON driver.

9. PACKAGE/PAD LOCATIONS

9.1. PAD Assignment and Locations

Please contact Sunplus sales representatives for more information.

9.2. Ordering Information

Product Number	Package Type
SPLC563A-C	Chip form
SPLC563A-PT122	Package form - TCP 4SP, 70W

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11. REVISION HISTORY

Date	Revision #	Description	Page
MAY. 16, 2005	1.0	1. Correct PIN No. in section “4. SIGNAL DESCRIPTIONS” 2. Delete Pin Map 3. Correct VCC connection in “8. APPLICATION CIRCUIT”	5 - 6 6 16
JUN. 13, 2003	0.2	Modify “*9. PACKAGE/PAD LOCATIONS*”	17
JUL. 12, 2001	0.1	Original	25

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