Integrated Circuit Systems, Inc.

ICS87949I-147

LOW SKEW, ÷1, ÷2 LVCMOS/LVTTL CLOCK GENERATOR

GENERAL DESCRIPTION

The ICS87949I-147 is a low skew, ÷1, ÷2 LVCMOS/LVTTL Clock Generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS87949I-147 has selectable single ended clock or LVPECL clock inputs. The single ended clock input accepts LVCMOS or LVTTL input levels. The PCLK, nPCLK pair can accept LVPECL, CML, or SSTL input levels. The low impedance LVCMOS/LVTTL outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased from 15 to 30 by utilizing the ability of the outputs to drive two series terminated lines.

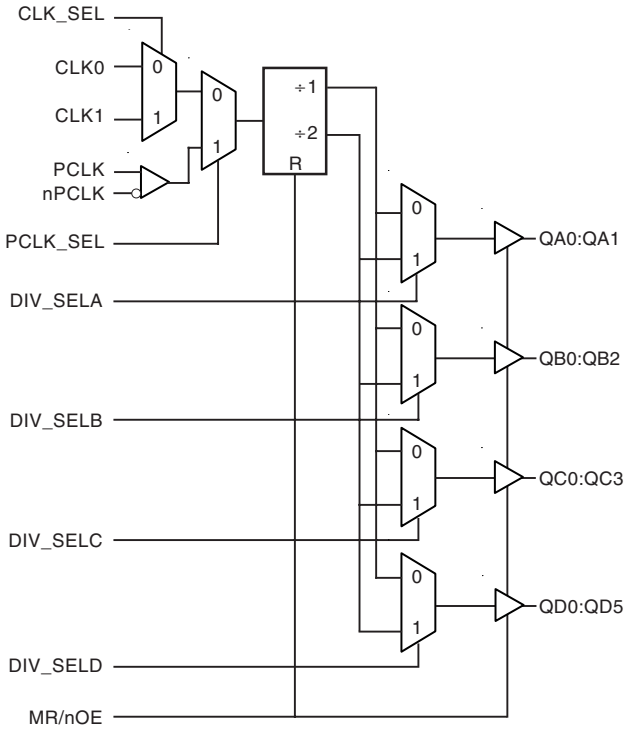
The divide select inputs, DIV_SELx, control the output frequency of each bank. The outputs can be utilized in the ÷1, ÷2 or a combination of ÷1 and ÷2 modes. The master reset input, MR/nOE, resets the internal frequency dividers and also controls the active and high impedance states of all outputs.

The ICS87949I-147 is characterized at 3.3V and 2.5V. Guaranteed output and part-to-part skew characteristics make the ICS87949I-147 ideal for those clock distribution applications demanding well defined performance and repeatability.

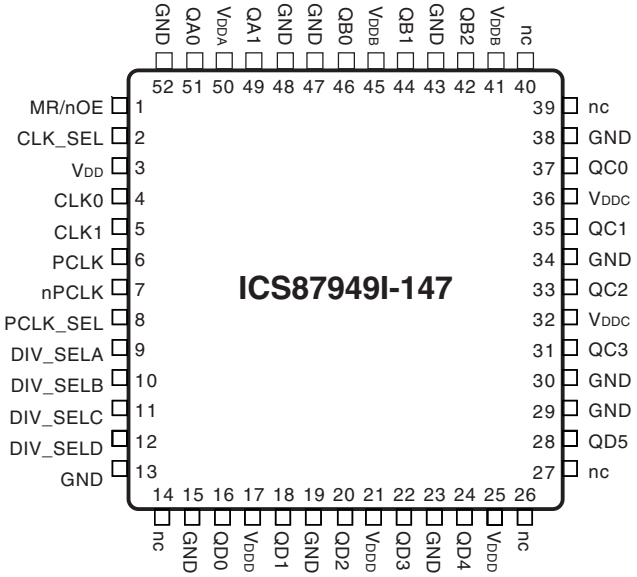
FEATURES

- 15 single ended LVCMOS/LVTTL outputs, 7Ω typical output impedance
- Selectable LVCMOS/LVTTL or LVPECL clock inputs
- CLK0 and CLK1 can accept the following input levels: LVCMOS and LVTTL
- PCLK, nPCLK supports the following input types: LVPECL, CML, SSTL
- Maximum input frequency: 250MHz
- Output skew: 250ps (maximum)
- Part-to-part skew: 1.0ns (maximum)
- Bank skew: 65ps (maximum)
- 3.3V or 2.5V supply voltage
- -40°C to 85°C ambient operating temperature
- Lead-Free package fully RoHS compliant

BLOCK DIAGRAM



PIN ASSIGNMENT



52-Lead LQFP
10mm x 10mm x 1.4mm package body
Y Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	MR/nOE	Input	Pulldown	Active High Master Reset. Active Low output enable. When logic HIGH, the internal dividers are reset and the outputs are tri-stated (HiZ). When logic LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTL interface levels.
2	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK1. When LOW, selects CLK0. LVCMOS / LVTTL interface levels.
3	V_{DD}	Power		Core supply pin.
4, 5	CLK0, CLK1	Input	Pullup	LVCMOS / LVTTL clock inputs.
6	PCLK	Input	Pulldown	Non-inverting differential LVPECL clock input.
7	nPCLK	Input	Pullup	Inverting differential LVPECL clock input.
8	PCLK_SEL	Input	Pulldown	PCLK select input. When HIGH, selects LVPECL clock input. When LOW, selects single ended clock input. LVCMOS / LVTTL interface levels.
9	DIV_SELA	Input	Pulldown	Controls frequency division for Bank A outputs. LVCMOS / LVTTL interface levels.
10	DIV_SELB	Input	Pulldown	Controls frequency division for Bank B outputs. LVCMOS / LVTTL interface levels.
11	DIV_SELC	Input	Pulldown	Controls frequency division for Bank C outputs. LVCMOS / LVTTL interface levels.
12	DIV_SELD	Input	Pulldown	Controls frequency division for Bank D outputs. LVCMOS / LVTTL interface levels.
13, 15, 19, 23, 29, 30, 34, 38, 43, 47, 48, 52	GND	Power		Power supply ground.
14, 26, 27, 39, 40	nc	Unused		No connect.
16, 18, 20, 22, 24, 28	QD0, QD1, QD2, QD3, QD4, QD5	Output		Bank D outputs. LVCMOS / LVTTL interface levels. 7Ω typical output impedance.
17, 21, 25	V_{DDD}	Power		Positive supply pins for Bank D outputs.
31, 33, 35, 37	QC3, QC2, QC1, QC0	Output		Bank C outputs. LVCMOS / LVTTL interface levels. 7Ω typical output impedance.
32, 36	V_{DDC}	Power		Positive supply pins for Bank C outputs.
41, 45	V_{DDB}	Power		Positive supply pins for Bank B outputs.
42, 44, 46	QB2, QB1, QB0	Output		Bank B outputs. LVCMOS / LVTTL interface levels. 7Ω typical output impedance.
49, 51	QA1, QA0	Output		Bank A outputs. LVCMOS / LVTTL interface levels. 7Ω typical output impedance.
50	V_{DDA}	Power		Positive supply pin for Bank A outputs.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
C_{PD}	Power Dissipation Capacitance (per output)	3.47V		23		pF
		2.625V		16		pF
R_{OUT}	Output Impedance		5	7	12	Ω

TABLE 3. FUNCTION TABLE

Inputs					Outputs			
MR/nOE	DIV_SELA	DIV_SELB	DIV_SELC	DIV_SELD	QA0, QA1	QB0:QB2	QC0:QC3	QD0:QD5
1	X	X	X	X	Hi Z	Hi Z	Hi Z	Hi Z
0	0	X	X	X	fIN/1	Active	Active	Active
0	1	X	X	X	fIN/2	Active	Active	Active
0	X	0	X	X	Active	fIN/1	Active	Active
0	X	1	X	X	Active	fIN/2	Active	Active
0	X	X	0	X	Active	Active	fIN/1	Active
0	X	X	1	X	Active	Active	fIN/2	Active
0	X	X	X	0	Active	Active	Active	fIN/1
0	X	X	X	1	Active	Active	Active	fIN/2

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	42.3°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDx}$ = 3.3V ± 0.3V, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDx}	Output Supply Voltage; NOTE 1		3.135	3.3	3.465	V
I_{DD}	Core Power Supply Current				60	mA
I_{DDx}	Output Power Supply Current; NOTE 2				20	mA

NOTE 1: V_{DDx} denotes V_{DDA}, V_{DDB}, V_{DDC}, V_{DDD}.
NOTE 2: I_{DDx} denotes the sum of I_{DDA}, I_{DDB}, I_{DDC}, I_{DDD}.

TABLE 4B. DC CHARACTERISTICS, $V_{DD} = V_{DDx}$ = 3.3V ± 0.3V, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	DIV_SELA:DIV_SELD, PCLK_SEL, CLK_SEL, MR/nOE		-0.3		0.8	V
		CLK0, CLK1		-0.3		1.3	V
V_{PP}	Peak-to-Peak Input Voltage			0.3		1	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 1.5		V_{DD}	V
I_{IH}	Input High Current	DIV_SELA:DIV_SELD, CLK_SEL, PCLK_SEL, MR/nOE	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		CLK0, CLK1	$V_{DD} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	DIV_SELA:DIV_SELD, CLK_SEL, PCLK_SEL, MR/nOE	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		CLK0, CLK1	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage		I_{OH} = -20mA	2.5			V
V_{OL}	Output Low Voltage		I_{OL} = 20mA			0.4	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for PCLK and nPCLK is V_{DD} + 0.3V.

TABLE 4C. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDx}$ = 2.5V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDx}	Output Supply Voltage; NOTE 1		2.375	2.5	2.625	V
I_{DD}	Core Power Supply Current				60	mA
I_{DDx}	Output Power Supply Current; NOTE 2				20	mA

NOTE 1: V_{DDx} denotes V_{DDA}, V_{DDB}, V_{DDC}, V_{DDD}.
NOTE 2: I_{DDx} denotes the sum of I_{DDA}, I_{DDB}, I_{DDC}, I_{DDD}.

TABLE 4D. DC CHARACTERISTICS, $V_{DD} = V_{DDx}$ = 2.5V±5%, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	DIV_SELA:DIV_SELD, PCLK_SEL, CLK_SEL, MR/nOE		-0.3		0.8	V
		CLK0, CLK1		-0.3		1.3	V
V_{PP}	Peak-to-Peak Input Voltage			0.3		1	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 1.5		V_{DD}	V
I_{IH}	Input High Current	DIV_SELA:DIV_SELD, CLK_SEL, PCLK_SEL, MR/nOE	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		CLK0, CLK1	$V_{DD} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	DIV_SELA:DIV_SELD, CLK_SEL, PCLK_SEL, MR/nOE	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		CLK0, CLK1	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage		I_{OH} = -20mA	1.8			V
V_{OL}	Output Low Voltage		I_{OL} = 20mA			0.4	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for PCLK and nPCLK is V_{DD} + 0.3V.

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDx} = 3.3V \pm 0.3V$, $T_A =$ -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Input Frequency					200	MHz
t_{PD}	Propagation Delay; NOTE 1	PCLK, nPCLK		2.1		4.2	ns
		CLK0, CLK1		2.1		5	ns
*t*sk(b)	Bank Skew: NOTE 2		Measured on the rising edge at $V_{DDx}/2$			65	ps
*t*sk(o)	Output Skew; NOTE 3, 6		Measured on the rising edge at $V_{DDx}/2$			300	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 6		Measured on the rising edge at $V_{DDx}/2$			1	ns
t_R	Output Rise Time		20% to 80%	400		950	ps
t_F	Output Fall Time		20% to 80%	400		950	ps
odc	Output Duty Cycle			40		60	%
t_{PZL}, t_{PZH}	Output Enable Time; NOTE 5					5	ns
t_{PLZ}, t_{PHZ}	Output Disable Time; NOTE 5					5	ns

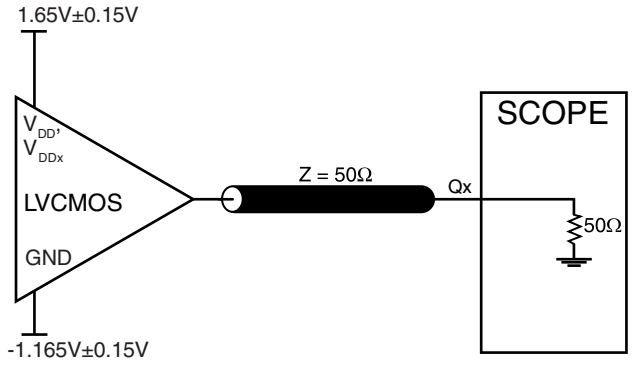
NOTE 1: Measured from the $V_{DD}/2$ or crosspoint of the input to $V_{DDx}/2$ of the output.
NOTE 2: Defined as skew within a bank of outputs at the same supply voltages and with equal load conditions.
NOTE 3: Defined as skew across banks of outputs at the same supply voltages and with equal load conditions. Measured at $V_{DDx}/2$.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages, same temperature, and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDx}/2$.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.
NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5B. AC CHARACTERISTICS, $V_{DD} = V_{DDx} = 2.5V \pm 5\%$, $T_A =$ -40°C TO 85°C

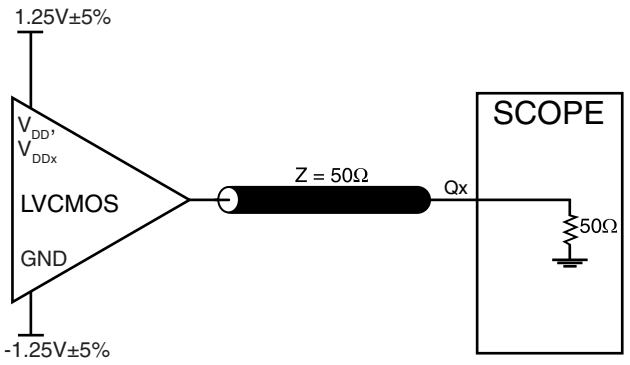
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Input Frequency				250	MHz
t_{PD}	Propagation Delay; NOTE 1		2.5		5.2	ns
*t*sk(b)	Bank Skew: NOTE 2	Measured on the rising edge at $V_{DDx}/2$			55	ps
*t*sk(o)	Output Skew; NOTE 3, 6	Measured on the rising edge at $V_{DDx}/2$			250	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 6	Measured on the rising edge at $V_{DDx}/2$			1.5	ns
t_R	Output Rise Time	20% to 80%	400		950	ps
t_F	Output Fall Time	20% to 80%	400		950	ps
odc	Output Duty Cycle		40		60	%
t_{PZL}, t_{PZH}	Output Enable Time; NOTE 5				5	ns
t_{PLZ}, t_{PHZ}	Output Disable Time; NOTE 5				5	ns

NOTE 1: Measured from the $V_{DD}/2$ or crosspoint of the input to $V_{DDx}/2$ of the output.
NOTE 2: Defined as skew within a bank of outputs at the same supply voltages and with equal load conditions.
NOTE 3: Defined as skew across banks of outputs at the same supply voltages and with equal load conditions. Measured at $V_{DDx}/2$.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages, same temperature, and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDx}/2$.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.
NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

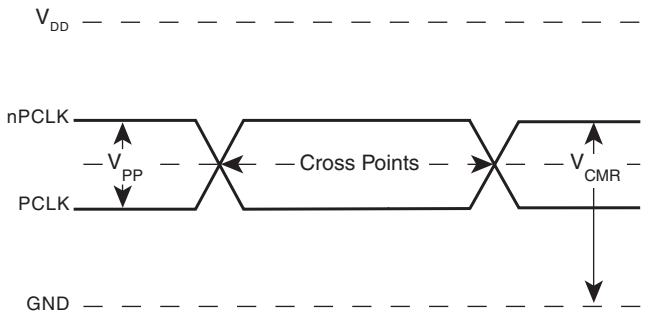
PARAMETER MEASUREMENT INFORMATION



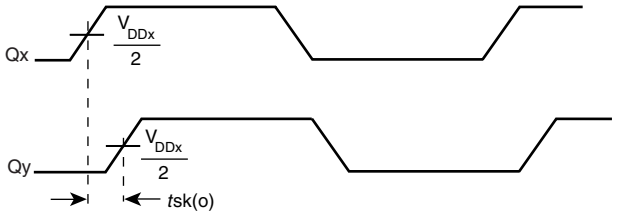
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



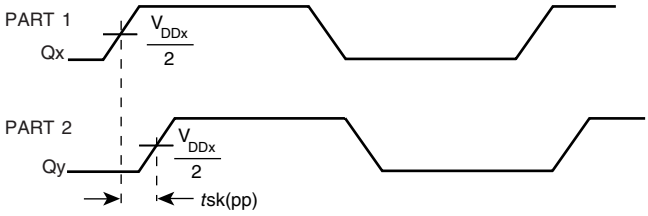
2.5V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



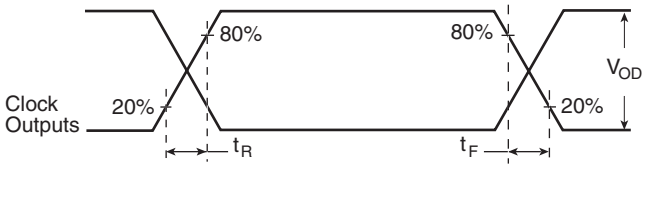
DIFFERENTIAL INPUT LEVEL



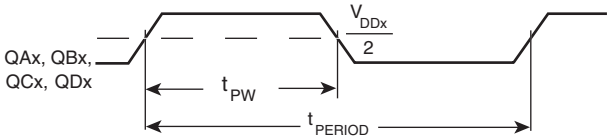
OUTPUT SKEW



PART-TO-PART SKEW

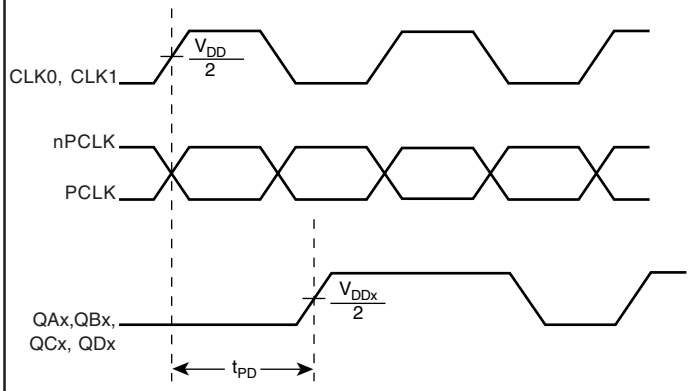


OUTPUT RISE/FALL TIME



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



PROPAGATION DELAY

APPLICATION INFORMATION

LVPECL CLOCK INPUT INTERFACE

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 1A to 1F* show interface examples for the HiPerClockS PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

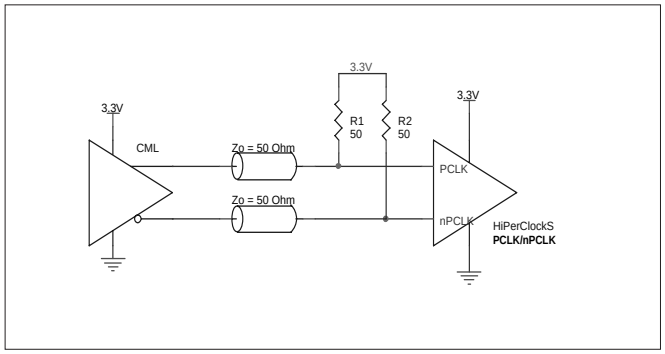


FIGURE 1A. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY AN OPEN COLLECTOR CML DRIVER

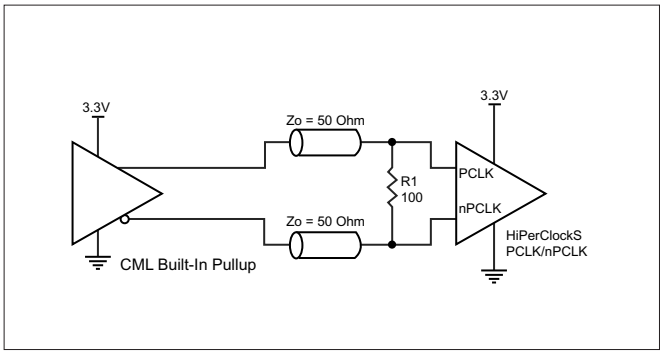


FIGURE 1B. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A BUILT-IN PULLUP CML DRIVER

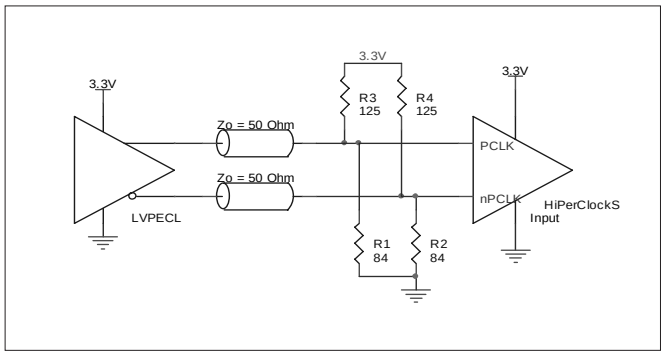


FIGURE 1C. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER

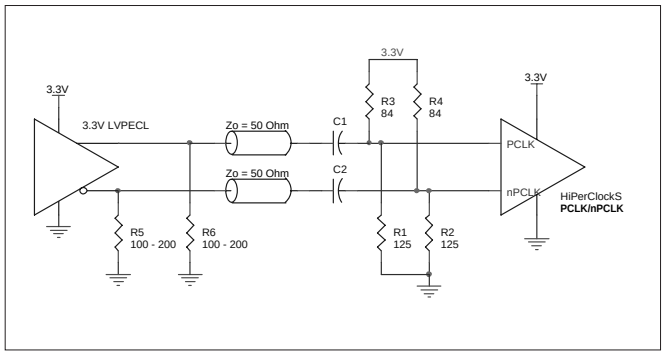


FIGURE 1D. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER WITH AC COUPLE

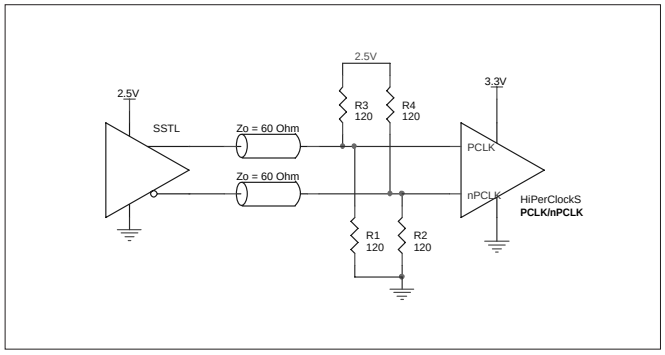


FIGURE 1E. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY AN SSTL DRIVER

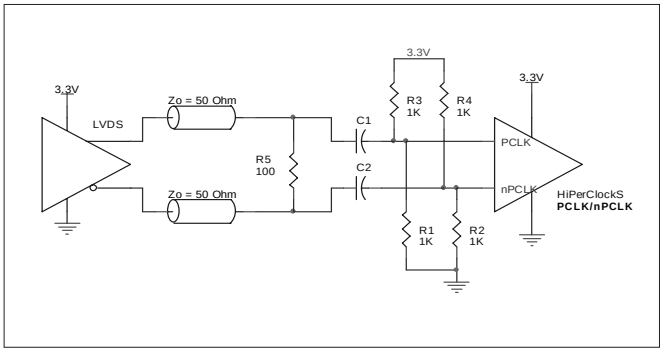


FIGURE 1F. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A 3.3V LVDS DRIVER

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 52 LEAD LQFP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	58.0°C/W	47.1°C/W	42.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	42.3°C/W	36.4°C/W	34.0°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS87949I-147 is: 1545

Pin compatible to the MPC949

PACKAGE OUTLINE - Y SUFFIX FOR 52 LEAD LQFP

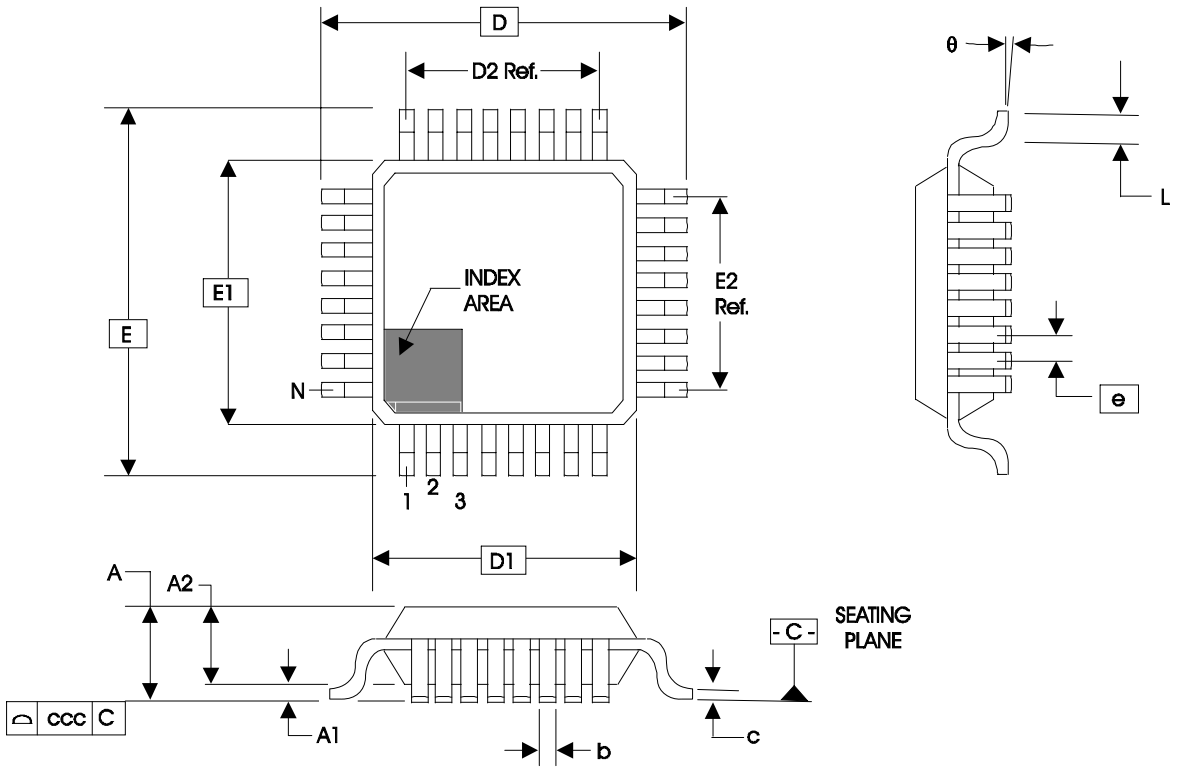


TABLE 7. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BCC		
	MINIMUM	NOMINAL	MAXIMUM
N		52	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.22	0.32	0.38
b1	0.22	0.30	0.33
D		12.00 BASIC	
D1		10.00 BASIC	
E		12.00 BASIC	
E1		10.00 BASIC	
e		0.65 BASIC	
ccc	0.45	--	0.10
ddd	--	--	0.13

Reference Document: JEDEC Publication 95, MS-026

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS87949AYI-147	7949AI147	52 Lead LQFP	tray	-40°C to 85°C
ICS87949AYI-147T	7949AI147	52 Lead LQFP	500 tape & reel	-40°C to 85°C
ICS87949AYI-147LF	TBD	52 Lead "Lead-Free" LQFP	tray	-40°C to 85°C
ICS87949AYI-147LFT	TBD	52 Lead "Lead-Free" LQFP	500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
B	1	2	Pin Description Table - revised MR/nOE description.	08/27/02
	4A, 4B, 5A	4, 5	In 3.3V DC and AC tables, changed $V_{DD} = V_{DDx}$ from 3.3V ± 5% to 3.3V ± 0.3V.	
	4B, 4D	4, 6	In 3.3V & 2.5V DC Characteristics tables - V_{IL} row, spec input controls separately from input clocks.	
		7	3.3V Output Load Test Circuit Diagram, changed V_{DD} equation to read 1.65V±0.15V from 1.65V±5%.	
B		9	Revised and replaced Package Outline diagram to correspond with Package Dimensions table.	11/21/02
	T1	2	Pin Description Table - changed V_{DD} description to read Core supply pin from Positive supply pin.	
	T4A, T4C	4, 5	Power Supply Characteristics table - changed V_{DD} description to read Core Supply Voltage from Positive Supply Voltage.	
C		1	Listed Bank Skew in Features Section.	09/15/03
	T1	2	Updated MR/nOE description.	
	T2	3	Pin Characteristics Table - change C_{IN} to read 4pF typ. from 4pF max. R_{OUT} added 5Ω min. and 12Ω max.	
	T5A, T5B	6	AC Characteristics Tables, added Bank Skew entries.	
C		1	Features Section - added Lead-Free bullet.	6/13/05
		8	Added LVPECL Clock Input Interface section.	
	T8	11	Ordering Information Table - added Lead-Free part number.	