

IRFZ48NS

IRFZ48NL

HEXFET® Power MOSFET

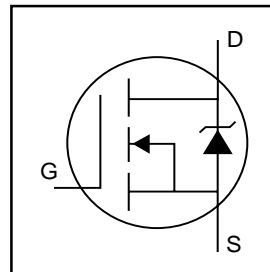
- Advanced Process Technology
- Surface Mount (IRFZ48NS)
- Low-profile through-hole (IRFZ48NL)
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated

Description

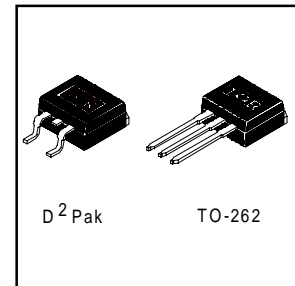
Advanced HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D²Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.

The through-hole version (IRFZ48NL) is available for low-profile applications.



$V_{DSS} = 55V$
$R_{DS(on)} = 0.014\Omega$
$I_D = 64A$



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	64	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	45	
I_{DM}	Pulsed Drain Current ①	210	
$P_D @ T_A = 25^\circ C$	Power Dissipation	3.8	W
$P_D @ T_C = 25^\circ C$	Power Dissipation	130	W
	Linear Derating Factor	0.83	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
I_{AR}	Avalanche Current ①	32	A
E_{AR}	Repetitive Avalanche Energy ①	13	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
R_{qJC}	Junction-to-Case	—	1.15	°C/W
R_{qJA}	Junction-to-Ambient (PCB Mounted, steady-state)**	—	40	

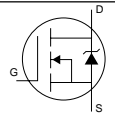
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Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	55	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.058	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	14	mΩ	V _{GS} = 10V, I _D = 32A ④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA
g _{fs}	Forward Transconductance	24	—	—	S	V _{DS} = 25V, I _D = 32A④
I _{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V _{DS} = 55V, V _{GS} = 0V
		—	—	250		V _{DS} = 44V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -20V
Q _g	Total Gate Charge	—	—	81	nC	I _D = 32A
Q _{gs}	Gate-to-Source Charge	—	—	19		V _{DS} = 44V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	30		V _{GS} = 10V, See Fig. 6 and 13
t _{d(on)}	Turn-On Delay Time	—	12	—	ns	V _{DD} = 28V
t _r	Rise Time	—	78	—		I _D = 32A
t _{d(off)}	Turn-Off Delay Time	—	34	—		R _G = 0.85Ω
t _f	Fall Time	—	50	—		V _{GS} = 10V, See Fig. 10 ④
L _S	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
C _{iss}	Input Capacitance	—	1970	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	470	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	120	—		f = 1.0MHz, See Fig. 5
E _{AS}	Single Pulse Avalanche Energy②	—	700⑤	190⑥	mJ	I _{AS} = 32A, L = 0.37mH

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	64	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode)①	—	—	210		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 32A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	68	100	ns	T _J = 25°C, I _F = 32A
Q _{rr}	Reverse Recovery Charge	—	220	330	nC	di/dt = 100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting T_J = 25°C, L = 0.37mH
R_G = 25Ω, I_{AS} = 32A. (See Figure 12)
- ③ I_{SD} ≤ 32A, di/dt ≤ 220A/μs, V_{DD} ≤ V_{(BR)DSS},
T_J ≤ 175°C
- ④ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ⑤ This is the destructive value not limited to the thermal limit.
- ⑥ This is the thermal limited value.

** When mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended soldering techniques refer to application note #AN-994.

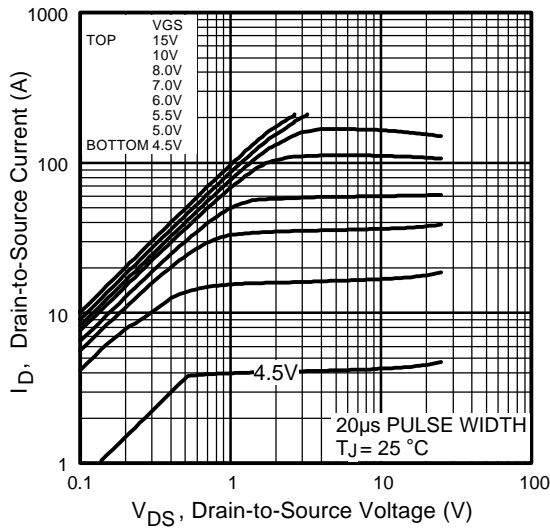


Fig 1. Typical Output Characteristics

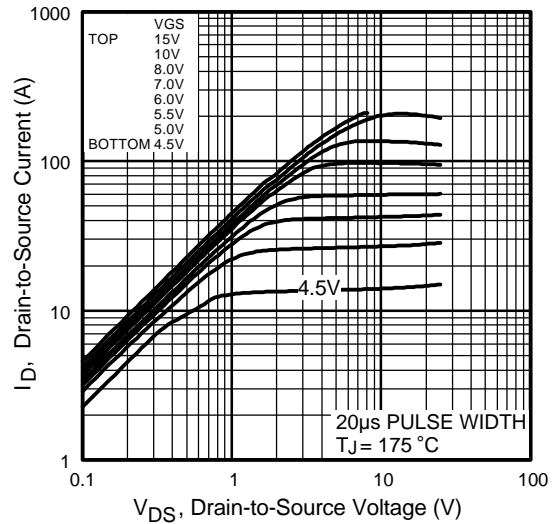


Fig 2. Typical Output Characteristics

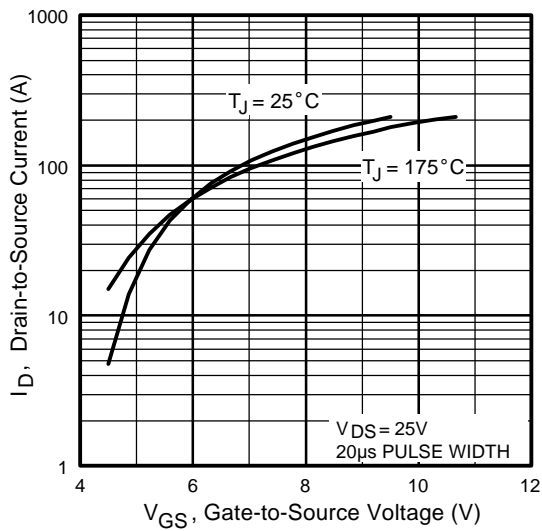


Fig 3. Typical Transfer Characteristics

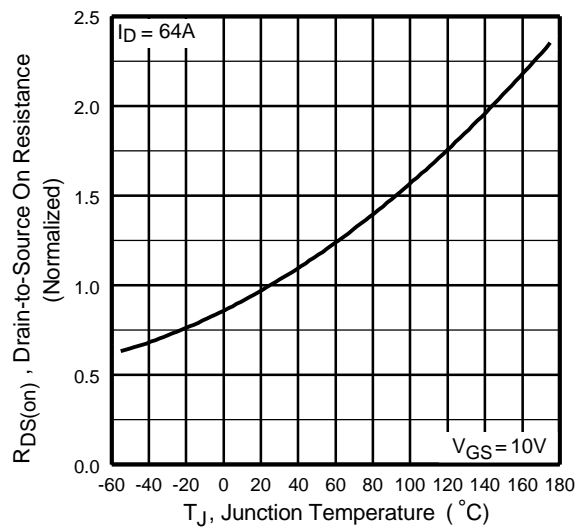


Fig 4. Normalized On-Resistance Vs. Temperature

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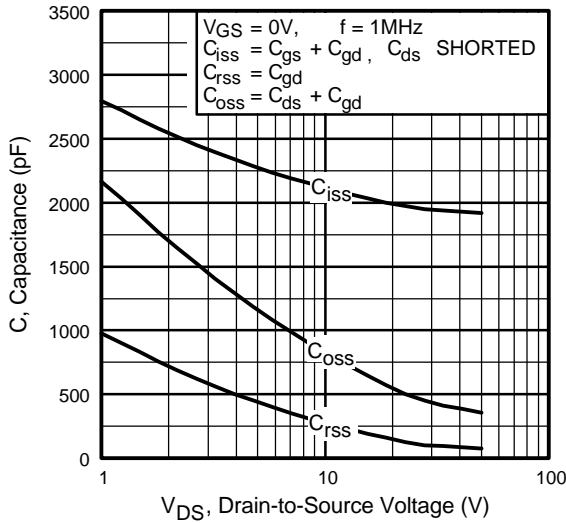


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

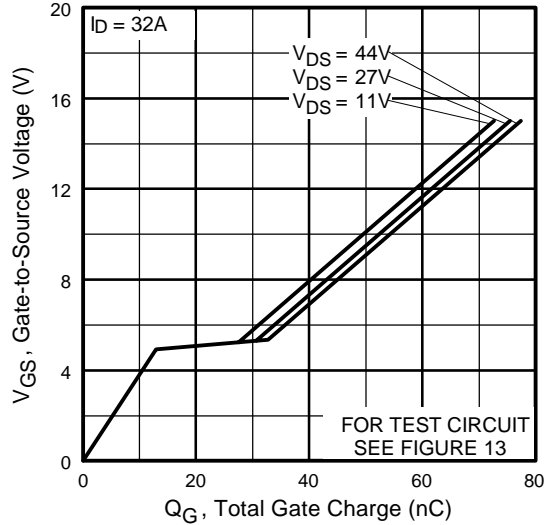


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

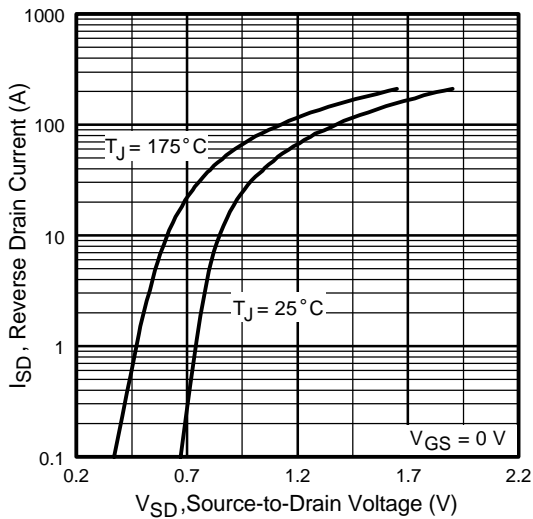


Fig 7. Typical Source-Drain Diode Forward Voltage

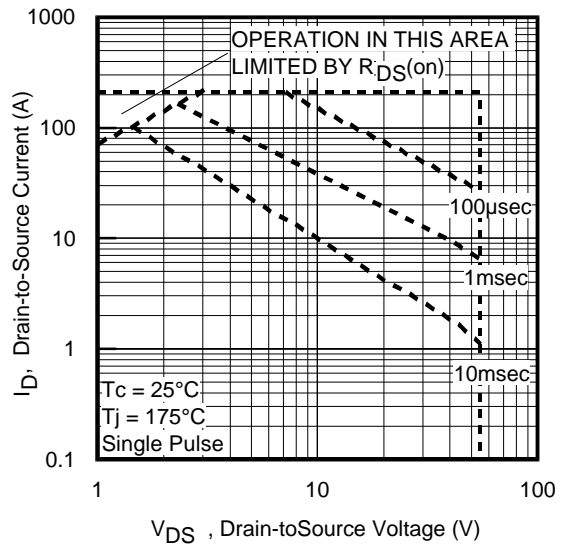


Fig 8. Maximum Safe Operating Area

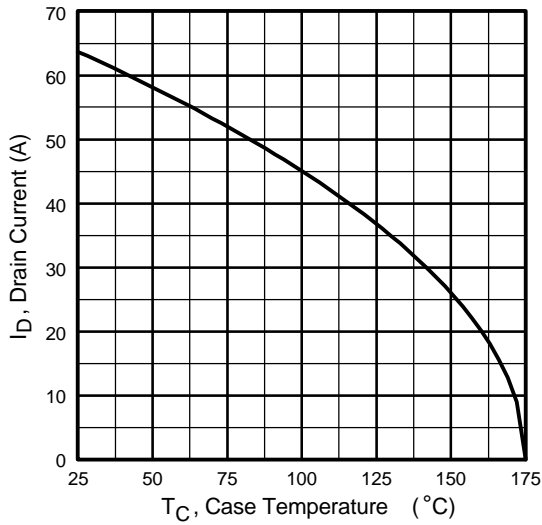


Fig 9. Maximum Drain Current Vs. Case Temperature

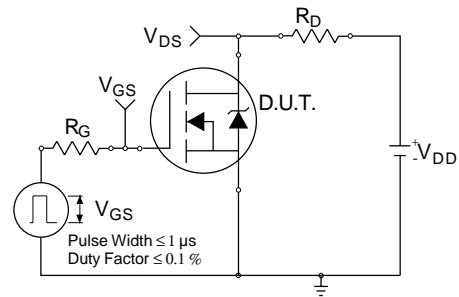


Fig 10a. Switching Time Test Circuit

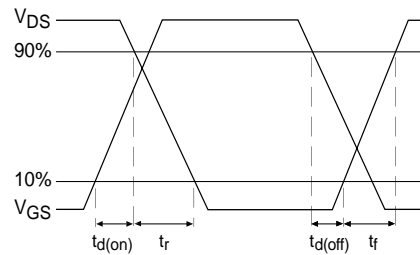


Fig 10b. Switching Time Waveforms

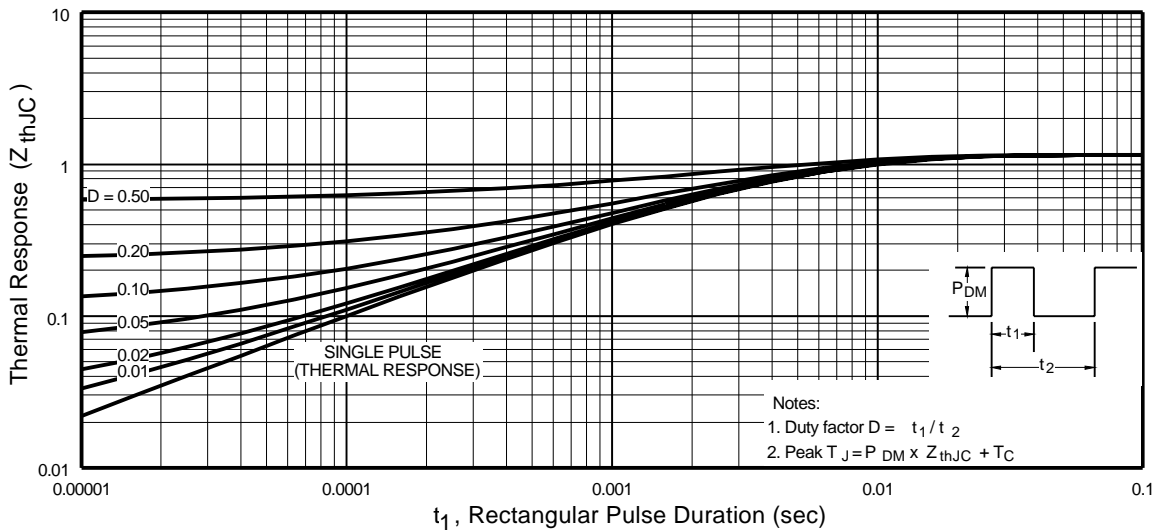


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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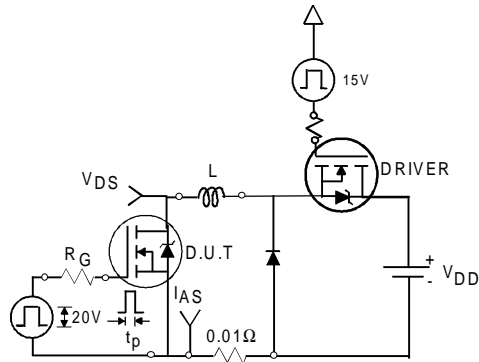


Fig 12a. Unclamped Inductive Test Circuit

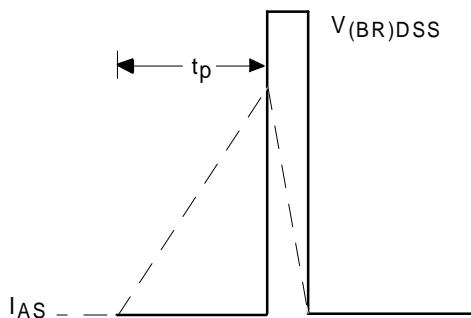


Fig 12b. Unclamped Inductive Waveforms

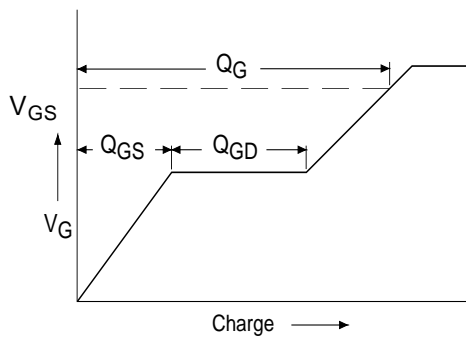


Fig 13a. Basic Gate Charge Waveform

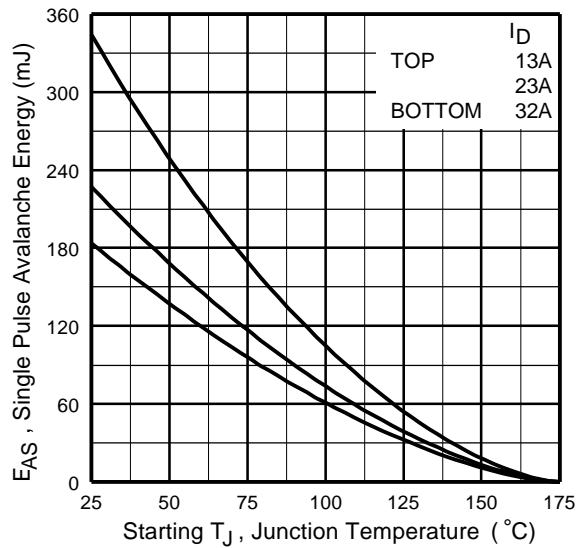


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

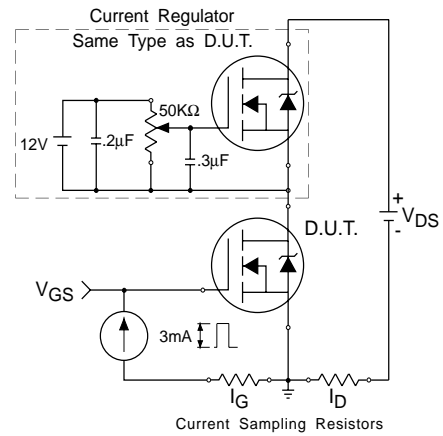
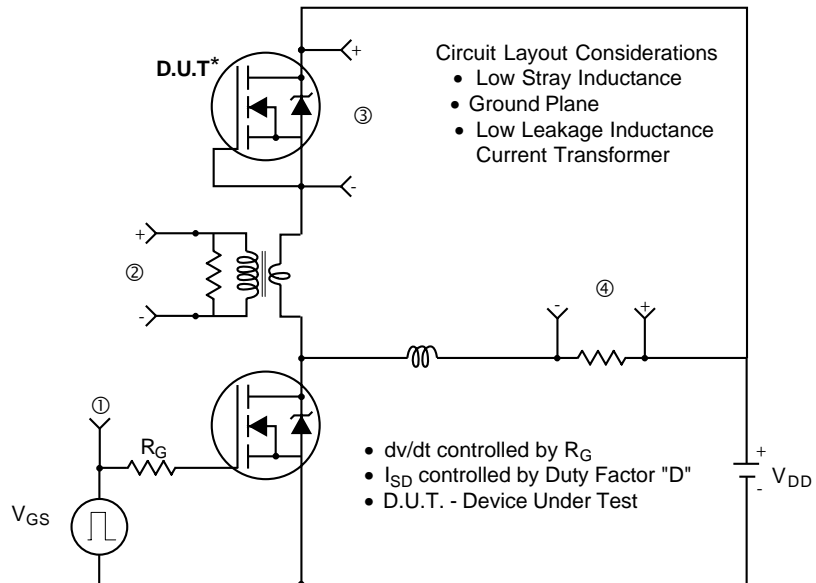
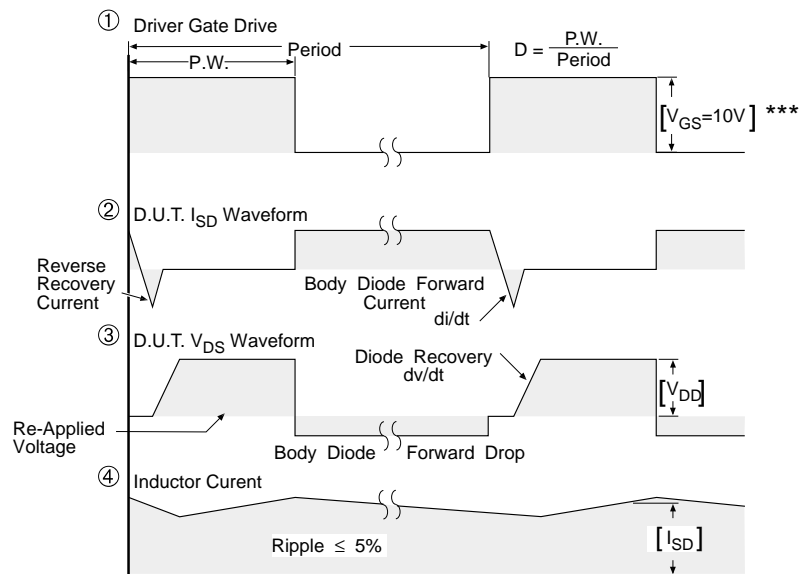


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel



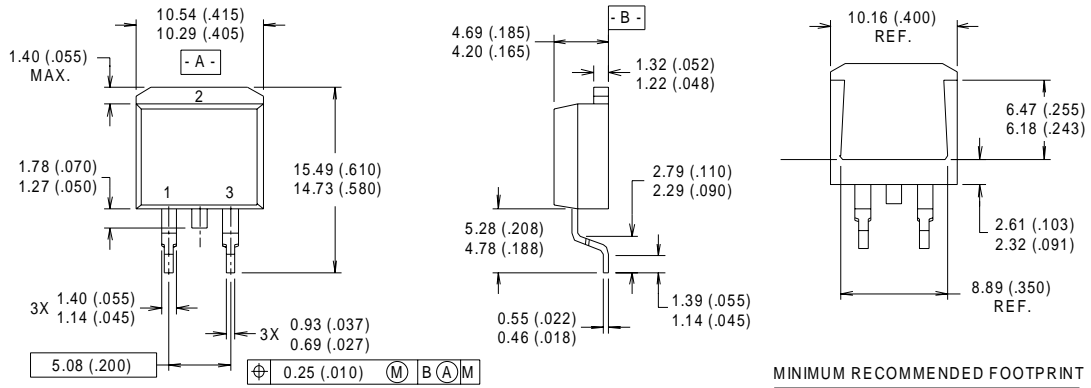
*** $V_{GS} = 5.0V$ for Logic Level and $3V$ Drive Devices

Fig 14. For N-channel HEXFET® power MOSFETs

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D²Pak Package Outline



NOTES:

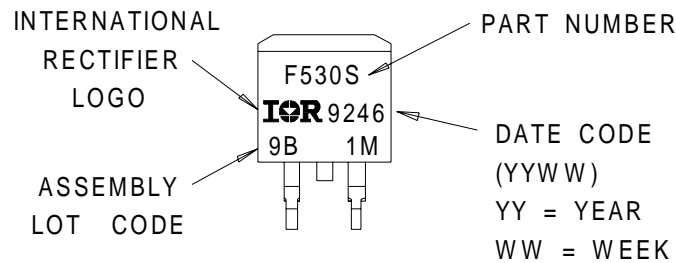
- 1 DIMENSIONS AFTER SOLDER DIP.
- 2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 3 CONTROLLING DIMENSION : INCH.
- 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

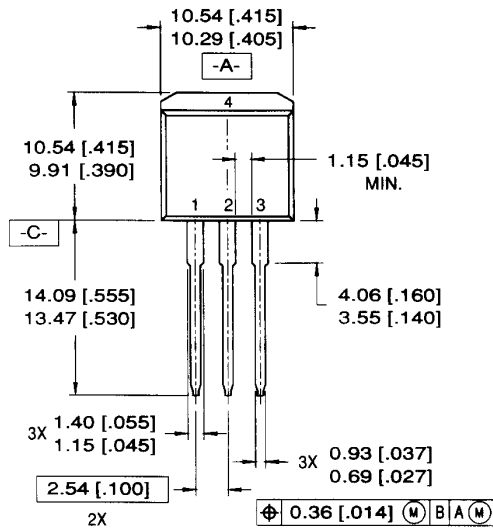
Part Marking Information

D²Pak



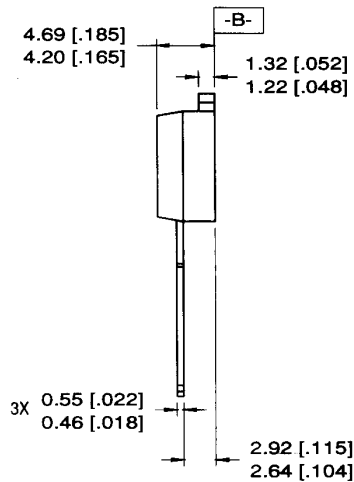
Package Outline

TO-262 Outline



LEAD ASSIGNMENTS

- | | |
|-----------|------------|
| 1 = GATE | 3 = SOURCE |
| 2 = DRAIN | 4 = DRAIN |



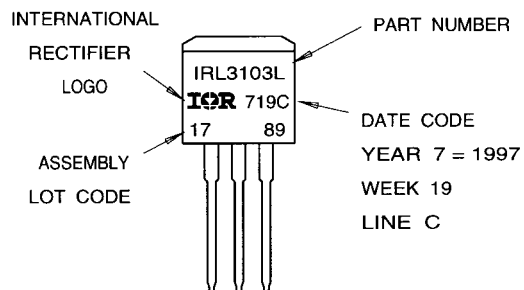
NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

Part Marking Information

TO-262

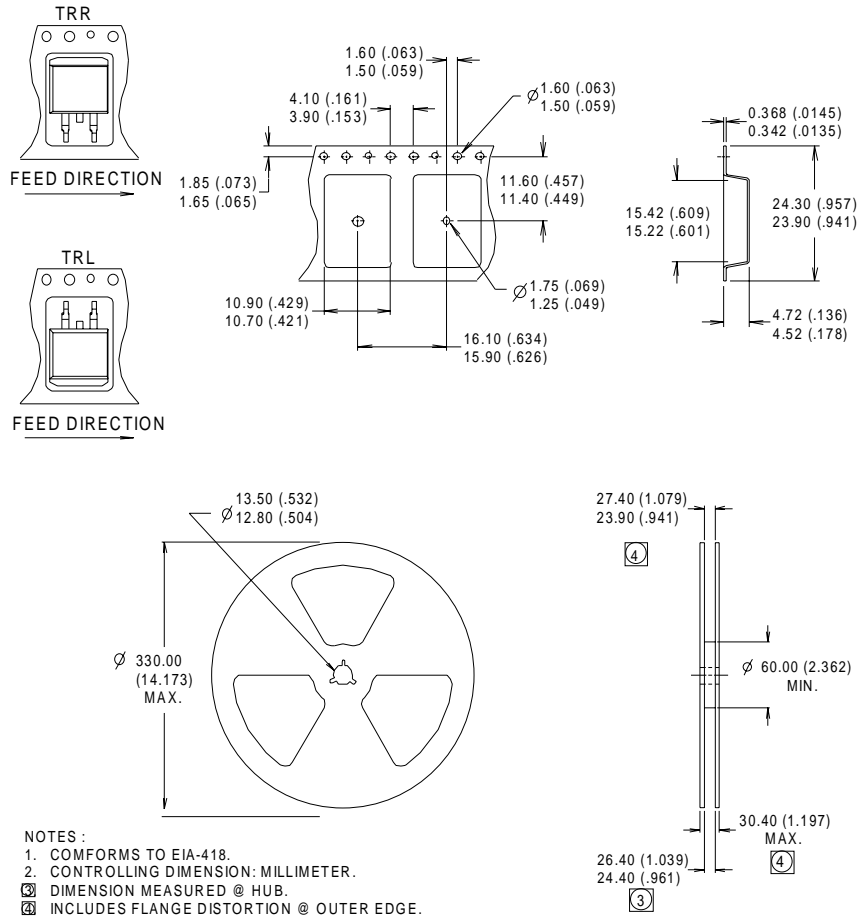
EXAMPLE: THIS IS AN IRL3103L
 LOT CODE 1789
 ASSEMBLED ON WW 19, 1997
 IN THE ASSEMBLY LINE "C"



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Tape & Reel Information D²Pak



Data and specifications subject to change without notice.
This product has been designed and qualified for the industrial market.
Qualification Standards can be found on IR's Web site.

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IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903

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