M50752-XXXSP, M50757-XXXSP M50758-XXXSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M50752-XXXSP, M50757-XXXSP and the M50758-XXXSP are single-chip microcomputers designed with CMOS silicon gate technology. These are housed in a 52-pin shrink plastic molded DIP.

These single-chip microcomputers are useful for business equipment and other consumer applications.

In addition to their simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The differences among M50752-XXXSP, M50757-XXXSP and M50758-XXXSP are noted below. The difference between M50757-XXXSP and M50758-XXXSP is the clock oscillating circuit only.

Type name	ROM size	RAM size	51 pin name
M50752-XXXSP	4096bytes	128bytes	V_{CC}
M50757-XXXSP	3072bytes	96bytes	NC
M50758-XXXSP	3072bytes	96bytes	NC

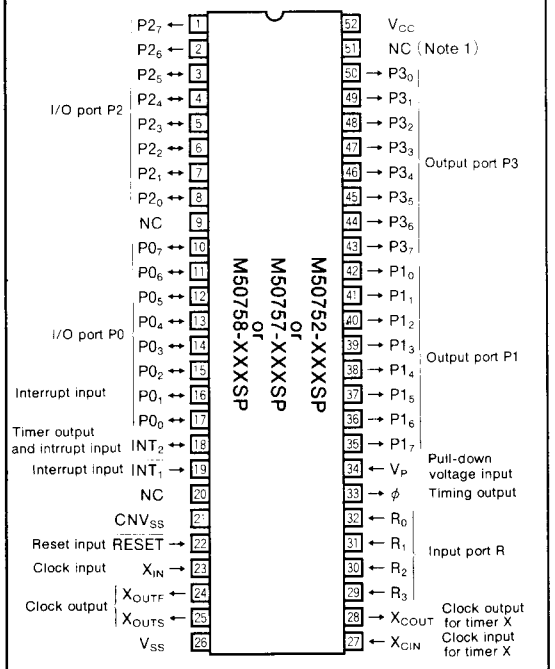
DISTINCTIVE FEATURES

- Number of basic instructions 69
- Memory size
  ROM ..... 3072 bytes (M50757-XXXSP, M50758-XXXSP)
  4096 bytes (M50752-XXXSP)
  RAM ..... 96 bytes (M50757-XXXSP, M50758-XXXSP)
  128 bytes (M50752-XXXSP)
- Instruction execution time
  ..... 2μs (minimum instructions at 4MHz frequency)
- Single power supply f(X_{IN})=4MHz ..... 5V$\pm$10%
- Power dissipation
  normal operation mode, at 4MHz frequency 15mW
- Subroutine nesting ..... 48 levels (Max.)
- Interrupt ..... 6 types, 5 vecters
- 8-bit timer 3
- Programmable I/O ports (Ports P0, $P2_0$~$P2_5$) 14
- Input port (Port R) 4
- High-voltage output ports (Ports P1, P3, $P2_6$, $P2_7$) 18

APPLICATION

VCR, Tuner, Audio-visual equipment

PIN CONFIGURATION (TOP VIEW)

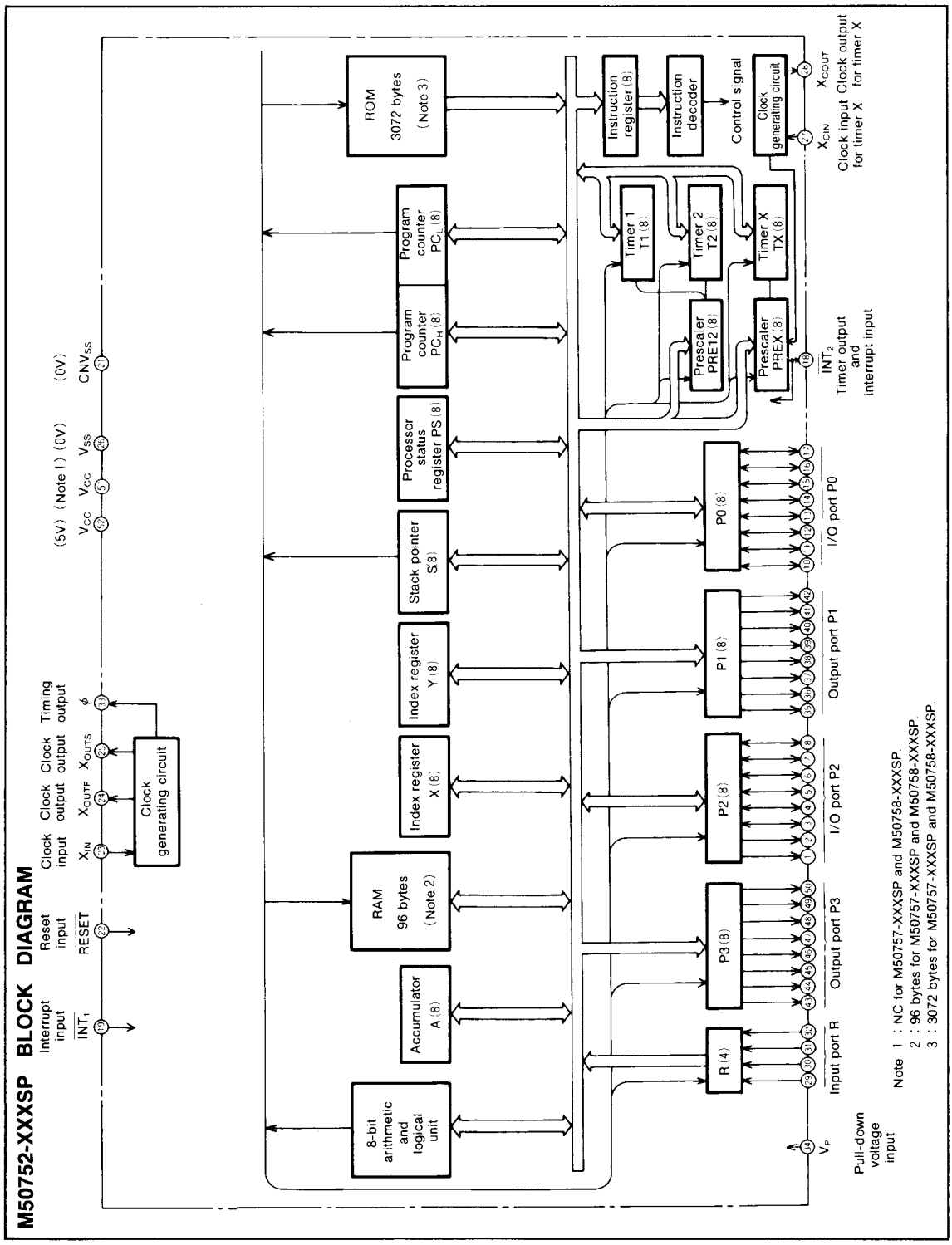


Outline 52P4B

NC : No connection

Note 1 : Pin number 51 is V_{CC} for M50752-XXXSP

M50752-XXXSP BLOCK DIAGRAM



Note 1 : NC for M50757-XXXSP and M50758-XXXSP.
2 : 96 bytes for M50757-XXXSP and M50758-XXXSP.
3 : 3072 bytes for M50757-XXXSP and M50758-XXXSP.

M50752-XXXSP, M50757-XXXSP M50758-XXXSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

FUNCTIONS OF M50752-XXXSP

Parameter			Functions
Number of basic instructions			69
Instruction execution time			2μs (minimum instructions, at 4MHz frequency)
Clock frequency			4MHz
Memory size	ROM		4096bytes (3072bytes for M50757-XXXSP and M50758-XXXSP)
	RAM		128bytes (96bytes for M50757-XXXSP and M50758-XXXSP)
Input/Output ports	R	Input	4-bit×1
	$\overline{INT_1}$	Input	1-bit×1
	P1, P3, $P2_5$, $P2_7$	Output	8-bit×2+2bit
	$\overline{INT_2}$	I/O	1-bit×1
	P0, $P2_0$~$P2_5$	I/O	8-bit×1+6-bit
Timers			8-bit prescaler×2+8-bit timer×3
Subroutine nesting			64 levels (max) (48levels for M50757-XXXSP and M50758-XXXSP)
Interrupts			Two external interrupts, Three internal timer interrupts
Clock generating circuit	for system clock		Built-in (RC oscillation, ceramic oscillator for M50758-XXXSP)
	for timer X		Built-in (quartz crystal oscillator)
Supply voltage	at normal operating		5V±10%
Power dissipation	at high-speed operation		15mW (at 4MHz frequency)
	at low-speed operation		4mW (at 20kH frequency)
Input/Output characteristics	Input/Output voltage		V_{CC}−33V (Ports P1, P3, $P2_6$~$P2_7$)
	Output current		10mA (Ports P0, $P2_0$~$P2_5$), −12mA (Ports P1, P3, $P2_6$~$P2_7$)
Memory expansion			Possible
Operating temperature range			−10~70°C
Device structure			CMOS silicon gate process
Package			52-pin shrink plastic molded DIP

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC} V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS}.
V_P	Pull-down voltage	Input	This is the input voltage pin for the pull-down transistor of ports P1, P3, $P2_6$ and $P2_7$.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, a resistor is connected between the X_{IN} and X_{OUTS} or the X_{OUTF} pins. If an external clock is used, the clock source should be connected to the X_{IN} pin and the X_{OUTS} and X_{OUTF} pins should be left open.
X_{OUTS}	Clock output	Output	This is output pin from internal clock generating circuit. The generating frequency can be controlled by connecting a resistor between this pin and X_{IN} pin.
X_{OUTF}	Clock output	Output	This is output pin from internal clock generating circuit. The generating frequency can be controlled by connecting a resistor between this pin and X_{IN} pin.
ϕ	Timing output	Output	This is the timing output pin.
X_{CIN}	Clock I/O for timer X	Input	These are I/O pins of the clock oscillating circuit for the timer X. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{CIN}pin and X_{COUT} pin.
X_{COUT}		Output	
$\overline{INT_1}$	Interrupt input	Input	This is the lowest order interrupt input pin.
$\overline{INT_2}$	Time output or interrupt input	I/O	This is in common with an output for the time X and an interrupt input pin.
R_0~R_3	Input port R	Input	Port R is a 4-bit input port.
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is N-channel open drain.
$P1_0$~$P1_7$	Output port P1	Output	Port P1 is an 8-bit output port. The output structure is P-channel open drain.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0. For $P2_6$ and $P2_7$ pins, output structure is P-channel open drain, and a pull-down transistor is built in between the V_P pin.
$P3_0$~$P3_7$	Output port P3	Output	Port P3 is an 8-bit output port and has basically the same functions as port P1.

BASIC FUNCTION BLOCKS

MEMORY

A memory map for the M50752-XXXSP is shown in Figure 1. Addresses 1000_{16} to $1FFF_{16}$ are assigned to the built-in ROM area which consists of 4096 bytes.

Addresses 1400_{16} to $1FFF_{16}$ are the ROM address area assigned to the M50757-XXXSP and M50758-XXXSP.

Addresses $1F00_{16}$ to $1FFF_{16}$ are a special address area (special page). By using the special page addressing mode of the JSR instruction, subroutines addressed on this page can be called with only 2 bytes. Addreeses $1FF4_{16}$ to $1FFF_{16}$ are vector addresses used for the reset and interrupts (see interrupt chapter). Addresses 0000_{16} to $00FF_{16}$ are the zero page address area. By using the zero page addressing mode, this area can also be accessed with 2 bytes. The use of these addressing methods will greatly reduce the object size required. The RAM, I/O port, timer, etc., are assigned to this area.

Addresses 0000_{16} to $007F_{16}$ are assigned to the built-in RAM and consist of 128 bytes of static RAM. Address 0000_{16} to $005F_{16}$, an area of 96 bytes, assigned to M50757-XXXSP and M50758-XXXSP. In addition to data storage, this RAM is used for the stack during subroutine calls and interrupts.

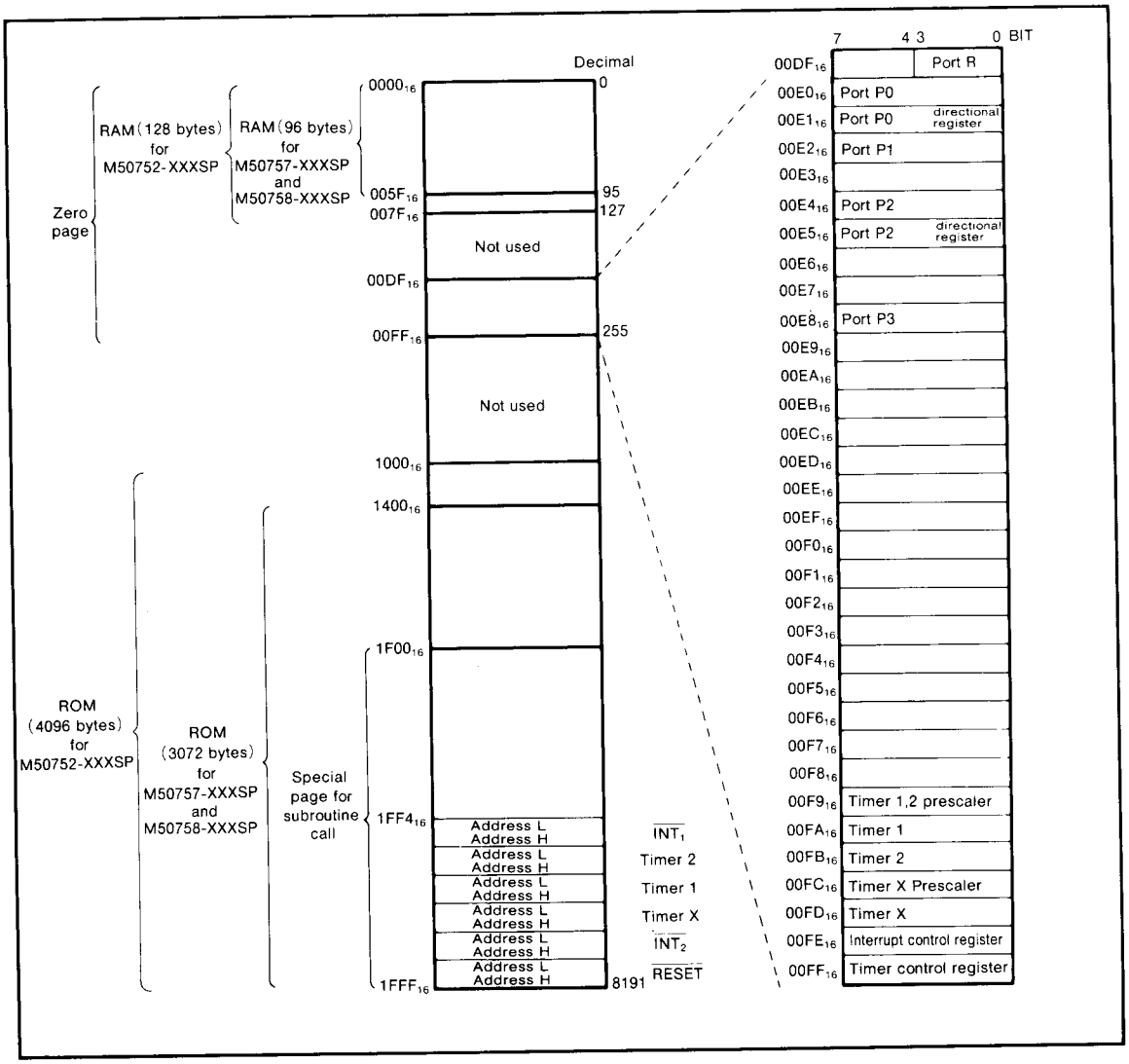


Fig.1 Memory map

CENTRAL PROCESSING UNIT (CPU)

The CPU consists of 6 registers and is shown in Figure 2.

ACCUMULATOR (A)

The 8-bit accumulator (A) is the main register of the microcomputer. Data operations such as data transfer, input/output, etc., are executed mainly through accumulator.

INDEX REGISTER X (X)

The index register X is an 8-bit register.
In the index addressing mode, the value of the OPERAND added to the contents of the register X, specifies the real address. When the T flag in the processor status register is set to "1", the index register X itself becomes the address for the second OPERAND.

INDEX REGISTER Y (Y)

The index register Y is an 8-bit register.
In the index addressing mode, the value of the OPERAND added to the contents of the register Y specifies the real address.

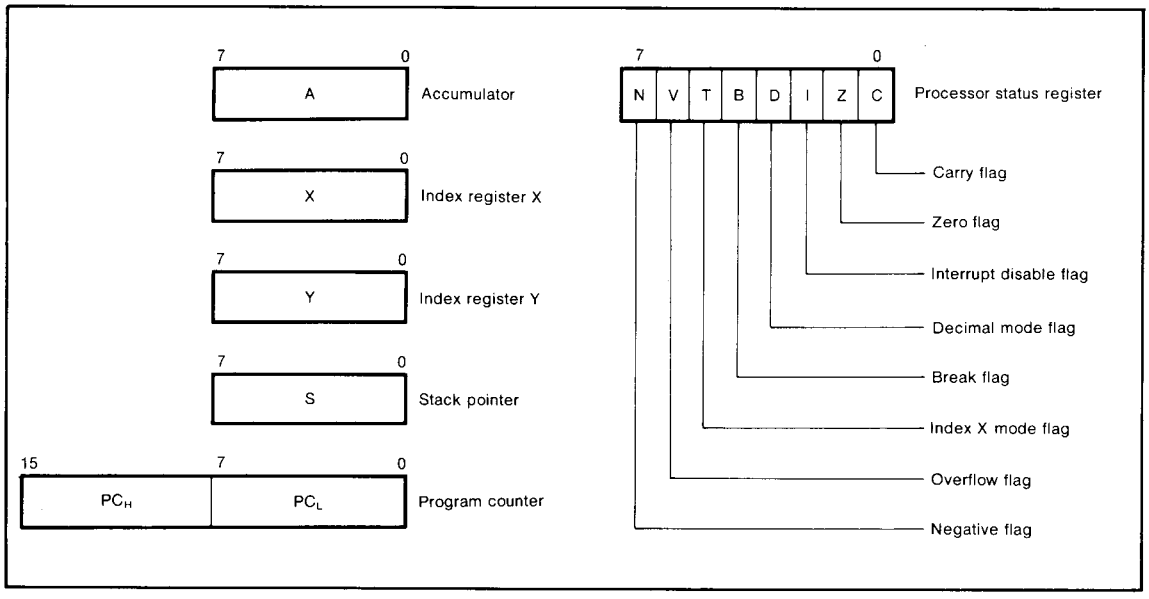


Fig.2 Register structure

STACK POINTER (S)

The stack pointer (S) is an 8-bit register that contains the address of the next location in the stack. It is mainly used during interrupts and subroutine calls. The stack pointer is not automatically initialized after reset and should be initialized by the program using the TXS instruction.

The contents of the stack pointer is XX_{16}, the stack address is set to $00XX_{16}$. When using this microcomputer in the single-chip mode, the stack pointer should be set at the bottom address of the internal RAM.

When an interrupt occurs, the higher 8 bits of the program counter are pushed into the stack first, and then the lower 8 bits of the program counter are pushed into the stack. After each byte is pushed into the stack, the stack pointer is decremented by one. Next, the contents of the processor status register are pushed into the stack. When the return from interrupt instruction (RTI) is executed, the program counter are processor status register data is pulled off the stack in reverse order from above.

The Accumulator is never pushed into the stack automatically. A Push Accumulator instruction (PHA) is provided to execute this function. Restoring the Accumulator to its previous value is accomplished by the Pull Accumulator instruction (PLA). It is executed in reverse order of the PHA instruction.

The contents of the Processor Status Register (PS) are pushed (pulled) to (from) the stack with the PHP and PLP instructions, respectively. Only the program counter is pushed into the stack during a subroutine call. Therefore, any registers that should not be destroyed should be pushed into the stack manually. The RTS instruction is used to return from a subroutine.

PROGRAM COUNTER (PC)

The 16-bit program counter consists of two 8-bit registers PC_H and PC_L. The program counter is used to indicate the address of the next instruction to be executed.

PROCESSOR STATUS REGISTER (PS)

The processor status register is composed entirely of flags used to indicate the condition of the processor immediately after an operation. Branch operations can be performed by testing the Carry flag (C), Zero flag (Z), Overflow flag (V) or the Negative flag (N). Each bit of the register is explained below.

1. Carry flag (C)

The carry flag contains the carry or borrow generated by the Arithmetic and Logical operation Unit (ALU) immediately after an operation. It also changed by the shift and rotate instructions. The set carry (SEC) and clear carry (CLC) instructions allow direct access for setting and clearing this flag.

2. Zero flag (Z)

This flag is used to indicate if the immediate operation generated a zero result or not. If the result is zero, the zero flag will be set to "1". If the result is not zero, the zero flag will be set to "0".

3. Interrupt disable flag (I)

This flag is used to disable all interrupts. This is accomplished by setting the flag to "1". When an interrupt, this flag is automatically set to "1" to prevent other interrupts from interfering until the current interrupt is completed. The SEI and CLI instructions are used to set and clear this flag, respectively.

4. Decimal mode flag (D)

The decimal mode flag is used to define whether addition and subtraction are executed in binary or decimal. If the decimal mode flag is set to "1", the operations are executed in decimal, if the flag is set to "0", the operations are executed in binary. Decimal correction is automatically executed. The SED and CLD instructions are used to set and clear this flag, respectively.

5. Break flag (B)

When the BRK instruction is executed, the same operations are performed as in an interrupt. The address of the interrupt vector of the BRK instruction is the same as that of the lowest priority interrupt. The contents of the B flag can be checked to determine which condition caused the interrupt. If the BRK instruction caused the interrupt, the break flag will be "1", otherwise it will be "0".

6. Index X mode flag (T)

When the T flag is "1", operations between memories are executed directly without passing through the accumulator. Operations between memories involving the accumulator are executed when the T flag is "0" (i.e., operation results between memories 1 and 2 are stored in the accumulator). The address of memory 1 is specified by the contents of the index register X, and that of memory 2 is specified by the normal addressing mode. The SET and CLT instructions are used to set and clear the index X mode flag, respectively.

7. Overflow flag (V)

The overflow flag functions when one byte is added or subtracted as a signed binary number. When the result exceeds +127 or −128, the overflow flag is set to "1". When the BIT instruction is executed, bit 6 of the memory location is input to the overflow flag. The overflow flag is reset by the CLV instruction and there is no set instruction.

8. Negative flag (N)

The negative flag is set whenever the result of a data transfer or operation is negative (bit 7 is set to "1"). Whenever the BIT instruction is executed, bit 7 of the memory location is input to the negative flag. There are no instructions for directly setting or resetting the negative flag.

Table 1 Interrupt vector address and priority

Interrupt	Priority	Vector address
$\overline{\text{RESET}}$	1	$1FFF_{16}$, $1FFE_{16}$
$\overline{\text{INT}_2}$	2	$1FFD_{16}$, $1FFC_{16}$
Timer X	3	$1FFB_{16}$, $1FFA_{16}$
Timer 1	4	$1FF9_{16}$, $1FF8_{16}$
Timer 2	5	$1FF7_{16}$, $1FF6_{16}$
$\overline{\text{INT}_1}$ (BRK)	6	$1FF5_{16}$, $1FF4_{16}$

INTERRUPT

The M50752-XXXSP can be interrupted from seven souces; $\overline{\text{INT}_2}$, timer X, timer 1, timer 2 or $\overline{\text{INT}_1}$/BRK instruction.

These interrupts are vectored and their priorities are shown in Table 1. Reset is included in this table since it has the same functions as the interrupts.

When an interrupt is accepted, the contents of certain registers are pushed into specified locations, (as discussed in the stack pointer section) the interrupt disable flag I is set, the program jumps to the address specified by the interrupt vector, and the interrupt request bit is cleared automatically. The reset interrupt is the highest priority interrupt and can never be inhibited. Except for the reset interrupt, all interrupt are inhibited when the interrupt disable flag is set to "1". All of the other interrupts can further be controlled individually via the interrupt control register shown in Figure 3.

An interrupt is accepted when the interrupt enable bit and the interrupt request bit are both "1" and the interrupt disable flag is "0".

The interrupt request bits are set when the following conditions occur:

(1) When the $\overline{\text{INT}_1}$ or $\overline{\text{INT}_2}$ pins go from "H" to "L"

(2) When the contents of timer X, timer 1, timer 2 go to "0"

These request bits can be reset by the program but can not be set by the progream. However, the interrupt enable bit can be set and reset by the program.

Since the BRK instruction and the $\overline{\text{INT}_1}$ interrupt have the same vectored address, the contents of the B flag must be checked to determine if the BRK instruction caused the interrupt or if $\overline{\text{INT}_1}$ generated the interrupt.

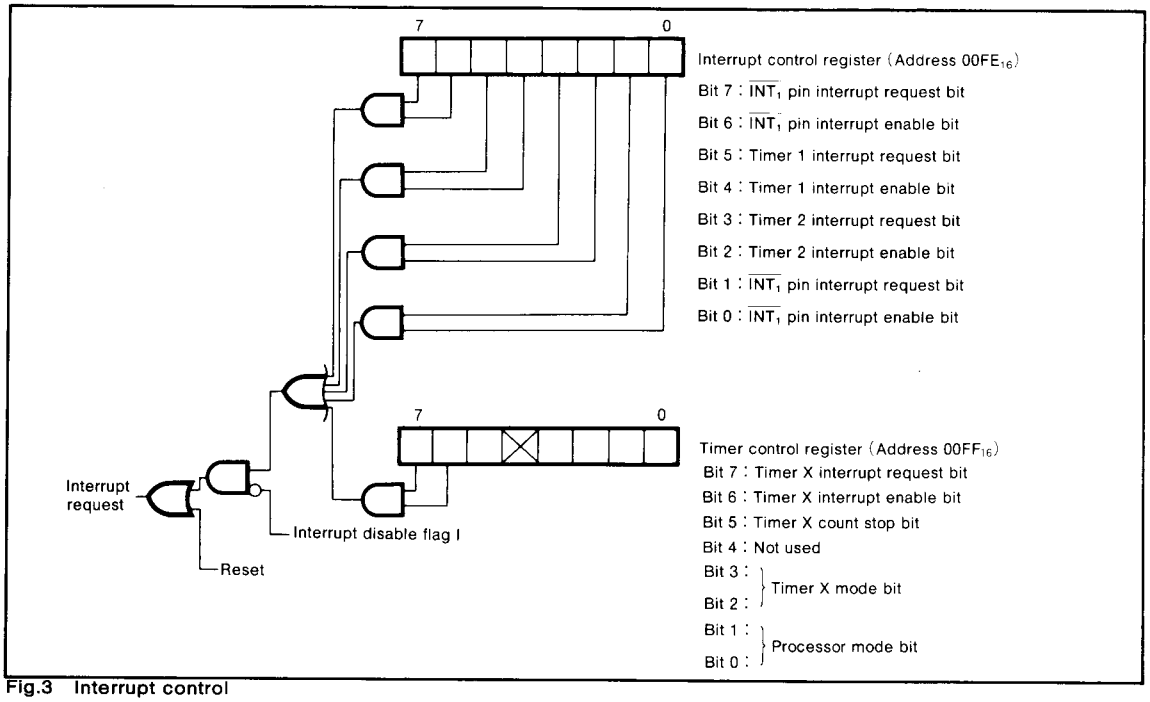


Fig.3 Interrupt control

TIMER

The M50752-XXXSP has three timers; timer X, timer 1, and timer 2. Timer X has four modes which can be selected by bit 2 and 3 of the timer control register. When the timer X count stop bit (bit 5) is set to "1", the timer X will stop regardless of which mode it is in. A block diagram of timer X, timer 1 and timer 2 is shown in Figure 4.

Timer 1 and timer 2 share with a prescaler. This prescaler has an 8-bit programmable latch used as a frequency divider. The division ratio is defined as $1/(n+2)$, where n is the decimal contents of the prescaler latch. All three timers are down-count timers which are reloaded from the timer latch following the zero cycle of the timer (i.e. the cycle after the timer counts to zero).

The timer interrupt request bit is set to "1" during the next clock pulse after the timer reaches zero. The interrupt and timer control registers are located at addresses $00FE_{16}$ and $00FF_{16}$, respectively (see Interrupt section). The prescaler latch and timer latch can be loaded with any number except zero.

The four modes of timer X as follows:

(1) Timer mode [00]
In this mode the clock is driven by the oscillator frequency divided by 16. When the timer down-counts to zero, the timer interrupt request bit is set to "1" and the contents of the timer's latch is reloaded into the timer and the counting begins again.

(2) Pulse output mode [01]
In this mode, the polarity of the $\overline{INT_2}$ signal is reversed each time the timer down-counts to zero.

(3) Event counter mode [10]
This mode operates in the same manner as the timer mode except, the clock source is input to the X_{CIN} pin. This mode will allow an interrupt to be generated whenever a specified number of external events have been generated. The timer down-counts every rising edge of the clock sourse.

(4) Pulse width measurement mode [11]
This mode measures the pulse width (between lows) input to the X_{CIN} pin. The timer, driven by the oscillator frequency divided by 16, continues counting during the low cycle of the X_{CIN} pin. When the timer contents reaches "0", the interrupt request bit is set to "1", the timer's reload latch is reloaded and the counting resumes.

The structure of the timer control register is shown in Figure 5.

When after reset, the prescaler and timer latch are set to FF_{16} and 01_{16}, respectively.

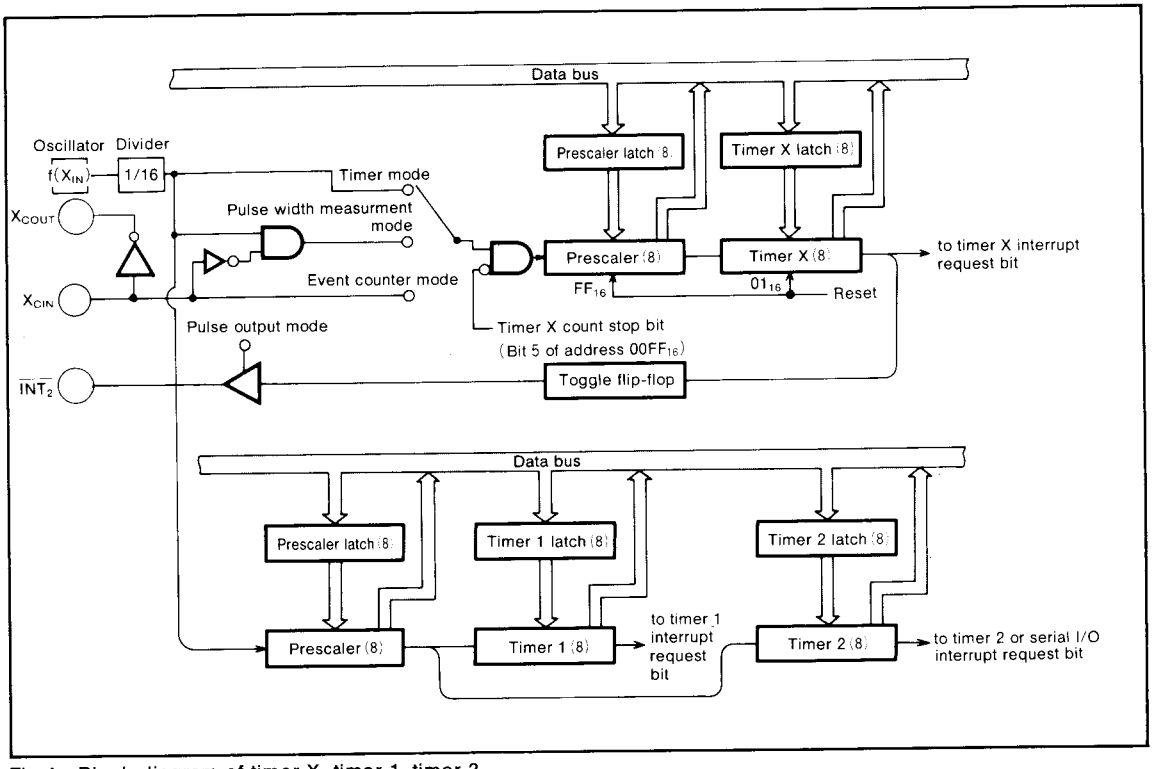


Fig.4 Block diagram of timer X, timer 1, timer 2

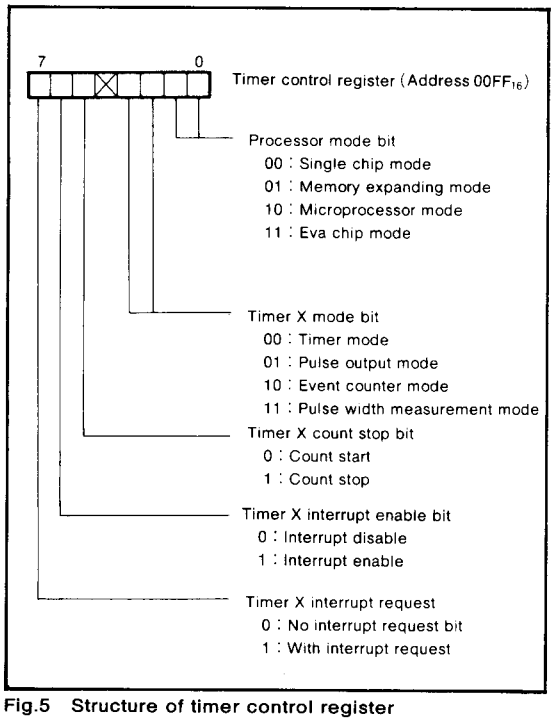


Fig.5 Structure of timer control register

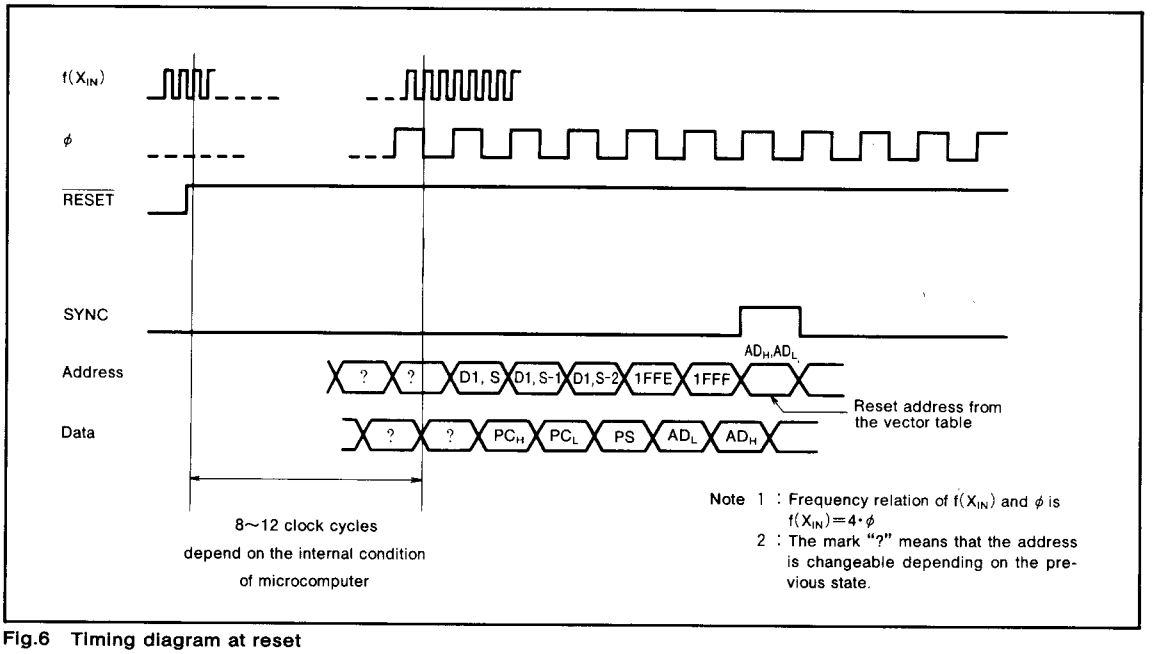


Fig.6 Timing diagram at reset

RESET CIRCUIT

The M50752-XXXSP is reset according to the sequence shown in Figure 6. It starts the program from the address formed by using the content of address $1FFF_{16}$ as the high order address and the content of the address $1FFF_{16}$ as the low order address, when the $\overline{RESET}$ pin is held at "L" level for more than $2\mu s$ while the power voltage is in the recommended operating condition and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 7.

An example of the reset circuit is shown in Figure 8.

When the power on reset is used, the $\overline{RESET}$ pin must be held "L" until the oscillation of X_{IN}-X_{OUT} becomes stable.

	Address	
(1) Port P0 directional register	($E1_{16}$) ···	00_{16}
(2) Port P1	($E2_{16}$) ···	00_{16}
(3) Port P2 directional register	($E5_{16}$) ···	00_{16}
(4) Port P3	($E8_{16}$) ···	00_{16}
(5) Prescaler X	(FC_{16}) ···	FF_{16}
(6) Timer X	(FD_{16}) ···	01_{16}
(7) Interrupt control register	(FE_{16}) ···	00_{16}
(8) Timer control register	(FF_{16}) ···	00_{16}
(9) Interrupt disable flag on the processor status register	(PS) ···	1
(10) Program counter	(PC_H) ···	Contents of address $FFFF_{16}$
	(PC_L) ···	Contents of address $FFFE_{16}$
(11) Internal oscillator output is connected to X_{OUT} (same condition after FST instruction is excuted)		

Fig.7 Internal state of microcomputer at reset

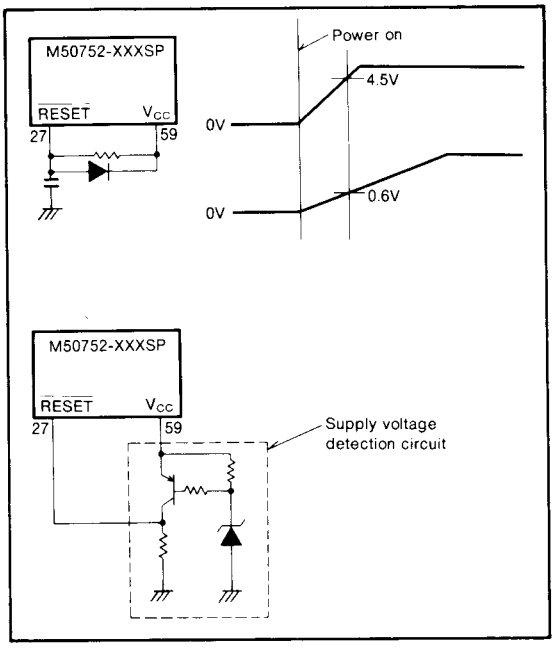


Fig.8 Example of reset circuit

I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with N-channel open drain output.

As shown in the memory map (Figure 1), port P0 can be accessed at zero page memory address $00E0_{16}$. Port P0 has a directional register (address $00E1_{16}$) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously output value to be read correctly even though the output voltage level is shifted up or down. Pins set as input are in the floating state and the signal levels can thus be read. When data is written into the input port, the data is latched only to the port latch and the pin still remains in the floating state.

Depending on the contents of the processor status register (bit 0 and bit 1 at address $00FF_{16}$), four different modes can be selected; single-chip mode, memory expanding mode, microprocessor mode and eva-chip mode. These modes (excluding single-chip mode) have a multiplexed address output function in addition to the I/O function. For more details, see the processor mode information.

(2) Port P1

Port P1 is an 8-bit output port with high-breakdown voltage p-channel open-drain outputs featuring a breakdown voltage of V_{CC}-33V. Each pin contains a pull-down resistor making V_P a negative power source. As shown in the memory map in Figure 1, port P0 is used on the zero page at address $00E2_{16}$ in memory.

Except in the single-chip mode, P1's functions are slightly different from P0's. For more details, see the processor mode information.

(3) Port P2

In the single chip mode, port $P2_6$, $P2_7$ has the same function as P1. And $P2_0 \sim P2_5$ has the same function as P0. In the other modes, P2's functions are slightly different from P0's.

For more details, see the processor mode information.

(4) Port P3

In the single-chip mode, port P3 has the same function as P0. This function does not change even though the processor mode changes. See Figure 9 for more details.

(5) Port R

Port R is an 4-bit input port. As shown in the memory map (Figure 1), port R can be accessed at the lower order 4 bits of zero page memory address $00DF_{16}$.

(6) Clock ϕ output pin

In normal conditions, the oscillator frequency divided by four is output as ϕ.

(7) $\overline{INT_1}$ pin

The $\overline{INT_1}$ pin is an interrupt input pin. The $\overline{INT_1}$ interrupt request bit (bit 1 at address $00FE_{16}$) is set to "1" when the input level of this pin changes from "H" to "L".

(8) $\overline{INT_2}$ pin

The $\overline{INT_2}$ pin is an interrupt input pin. When this signal level changes from "H" to "L", the interrupt request bit (bit 7 at address $00FE_{16}$) is set to "1". In the pulse output mode, the $\overline{INT_2}$ output changes polarity each time the contents of timer X goes to "0".

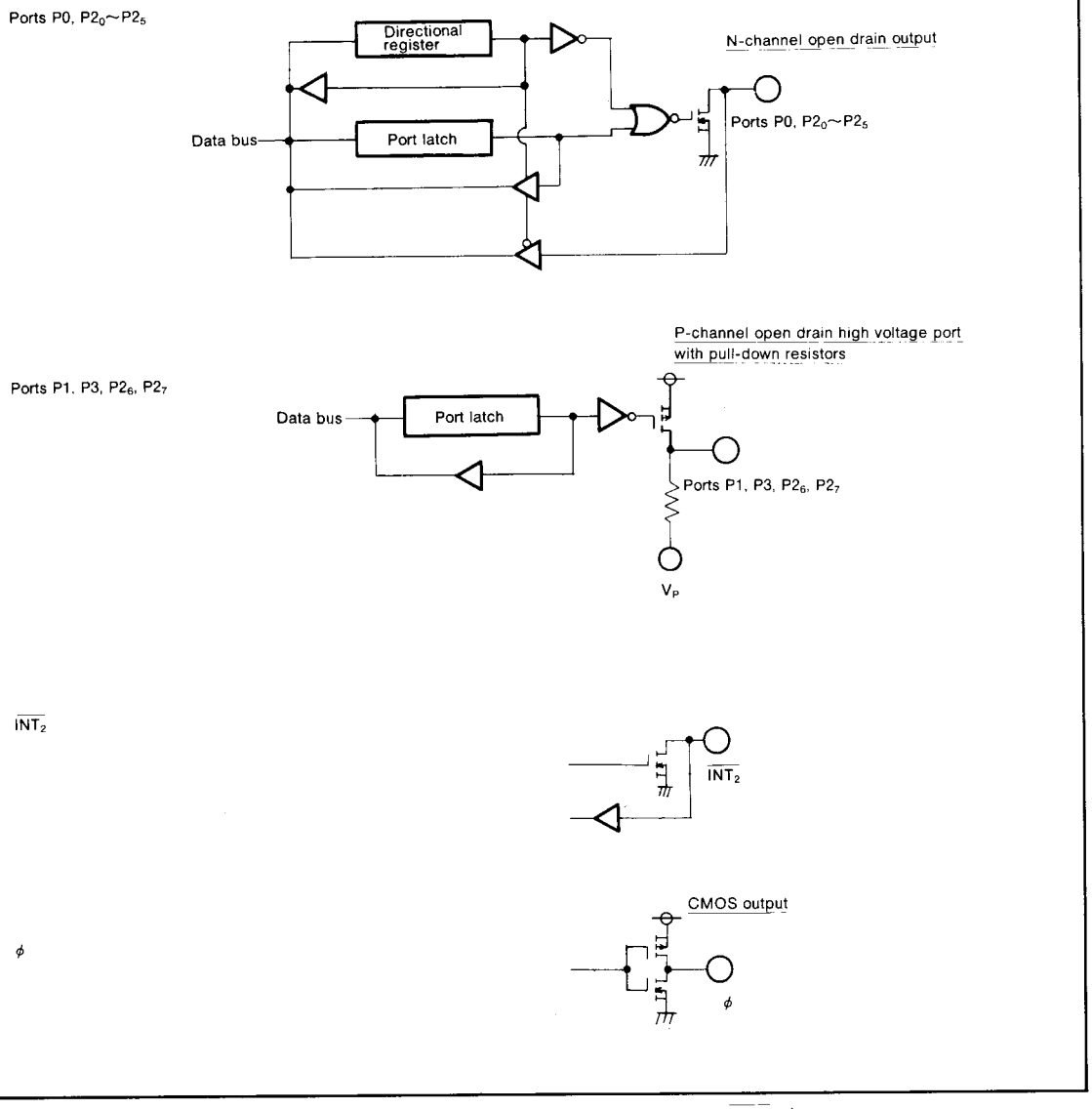


Fig.9 Block diagram of port P0~P3 (single-chip mode) and output formats of $\overline{INT_2}$, ϕ

PROCESSOR MODE

By changing the contents of the processor mode bit (bit 0 and 1 at address $00FF_{16}$), four different operation modes can be selected; single-chip mode, memory expanding mode, microprocessor mode and evaluation chip (eva-chip) mode. In the memory expanding mode, microprocessor mode and eva-chip mode, ports P0~P2 can be used as multiplexed I/O for address, data and control signals, as well as the normal functions of the I/O ports.

Figure 11 shows the functions of ports P0~P2.

The memory map for the single-chip mode is illustrated in Figure 1 and for other modes, in Figure 10.

By connecting CNV_{SS} to V_{SS}, all four modes can be selected through software by changing the processor mode bits.

Supplying "H" level to CNV_{SS} places the microcomputer in the eva-chip mode. The four different modes are explained as follows:

(1) Single-chip mode [00]

The microcomputer will automatically be in the single-chip mode when started from reset, if CNV_{SS} is connected to V_{SS}. Ports P0~P2 will work as original I/O ports.

(2) Memory expanding mode [01]

The microcomputer will be placed in the memory expansion mode when CNV_{SS} is connected to V_{SS} and the processor mode bits are set to "01". This mode is used to add external memory when the internal memory is not sufficient.

The lower 8 bits of address data for port P0 is output when ϕ goes to "H" state. When ϕ goes to the "L" state, P0 retains its original I/O functions.

Port P1's higher 5 bits of address data are output when ϕ goes to "H" state and as it changes back to the "L" state it retains its original I/O functions.

Pins $P1_6$ and $P1_5$ output the SYNC and R/$\overline{W}$ control signals, respectively while ϕ is in the "H" state. When in the "L" state, $P1_5$, $P1_6$ and $P1_7$ retain their original I/O function.

The R/$\overline{W}$ output is used to read/write from/to the outside. When this pin is in the "H" state, the CPU reads data, and when in the "L" state, the CPU writes data.

The SYNC is a synchronous signal which goes to the "H" state when it fetches the OP CODE.

Port P2 retains its original output functions while ϕ is at the "H" state, and works as a data bus of $D_7 \sim D_0$ (including instruction code) while at the "L" state.

(3) Microprocessor mode [10]

In this mode, port P0 and P1 are used as the system address bus and the original function of the I/O pins is lost. Port $P1_5$ and $P1_6$ become the SYNC and R/$\overline{W}$ pins, respectively and the normal I/O functions are lost. Port P2 becomes the databus ($D_7 \sim D_0$) and loses its normal I/O functions. Insternal memory ($E1_{16}$ to $E0_{16}$) cannot be used, and an external memory is needed if the address where normal I/O function have lost.

(4) Eva-chip mode [11]

When "H" level is supplied to CNV_{SS} pin, the microcomputer is forced into the eva-chip mode. The main purpose of this mode is to evaluate ROM programs prior to masking them into the microcomputer's internal ROM.

With the exceptions that the internal ROM is disabled and that external memory must be attached in this mode is the same as the memory expanding mode.

The relationship between the input level of CNV_{SS} and the processor mode is shown in Table 2.

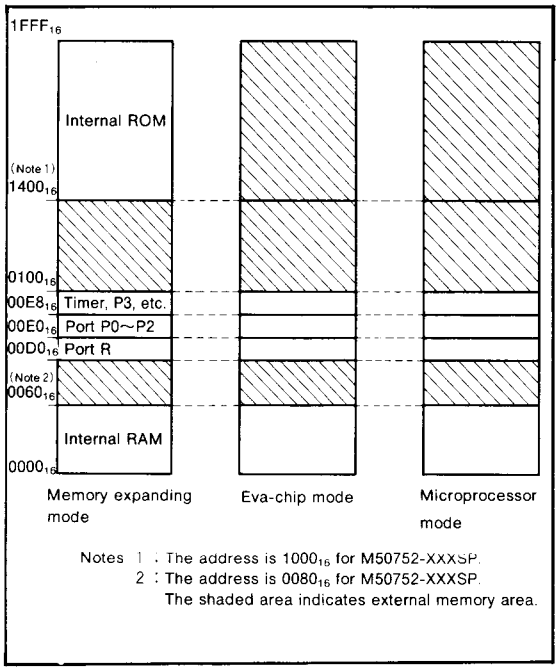


Fig.10 External memory area in processor mode

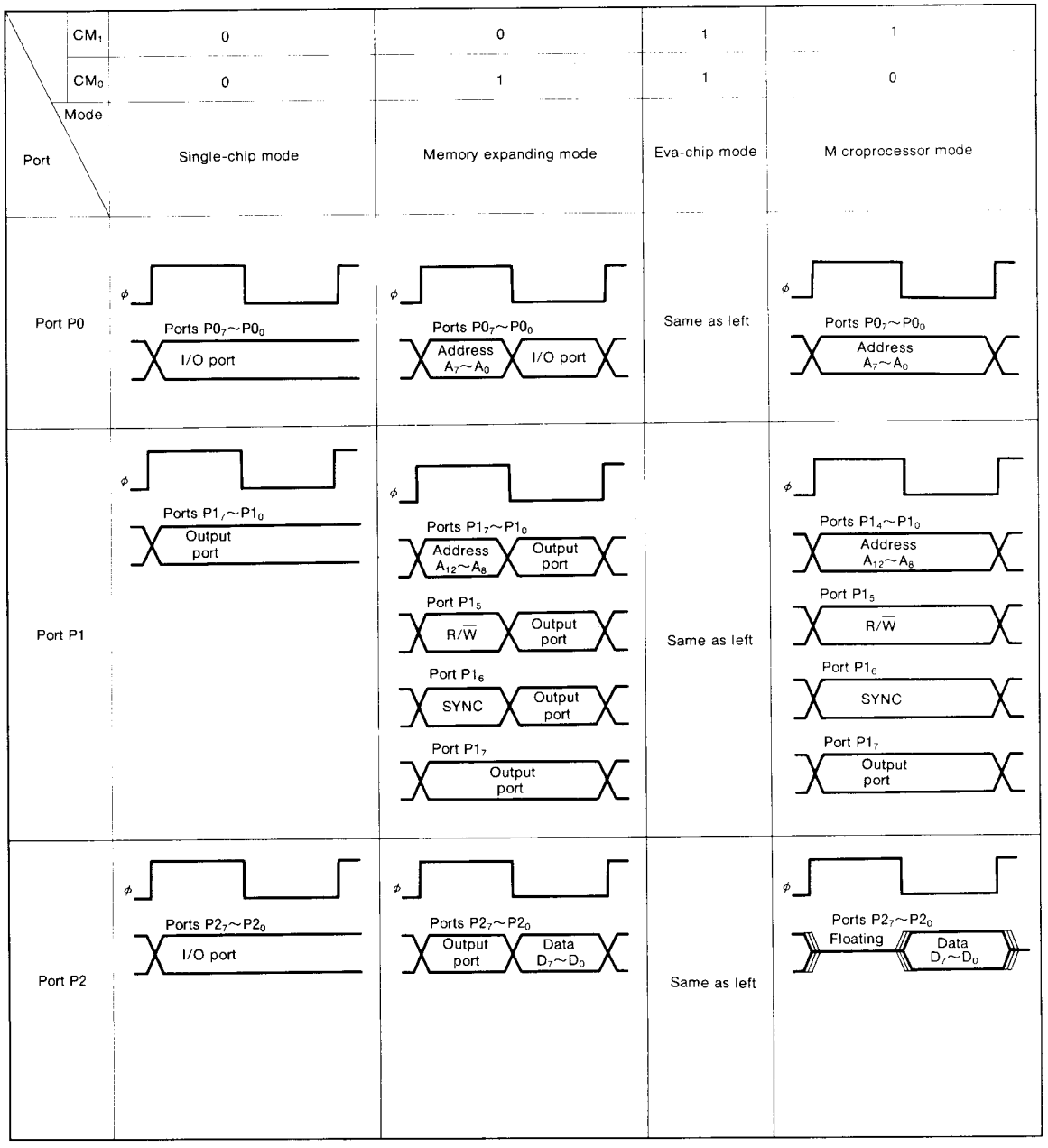


Fig.11 Processor mode and functions of ports P0~P2

Table 2 Relationship between CNV_{SS} pin input level and processor mode

CNV_{SS}	Mode	Explanation
V_{SS}	• Single-chip mode • Memory expanding mode • Eva-chip mode • Microprocessor mode	The single-chip mode is set by the reset. All modes can be selected by changing the processor mode bit with the program.
"H" level	• Eva-chip mode	Eva-chip mode can be also selected by changing the processor mode bit with the program.

CLOCK GENERATING CIRCUIT

The built-in clock generating circuits are shown in Figure 12. When FST instruction is executed, SW_{OSC} is closed and when SLW instruction is executed, SW_{OSC} is open. These instructions are used, when CR oscillation is required, to change the oscillation frequency.

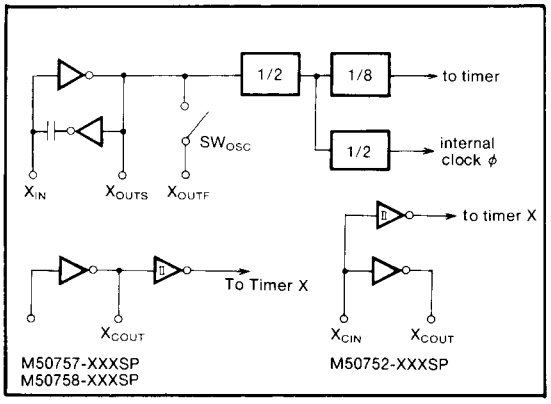


Fig.12 Block diagram of clock generating circuit

The circuit examples of clock generator are shown in Figures 13 ~ 17. The example when system clock signal is supplied from outside is shown in Figures 13 and 14. When clock signal is supplied from outside, let X_{IN} be the input, and open X_{OUTS} and X_{OUTF} (Figure 15).

The clock signal for Timer X can be supplied by planing the ceramic oscillation (or a quartz crystal oscillation) in outside. The constant of capacitance differs depending on oscillators. Therefore, try to adjust the recommended value of each oscillator manufactuer (Figure 16). In order to supply the clock signal from outside, let X_{CIN} be the input, and open X_{COUT} (Figure 17).

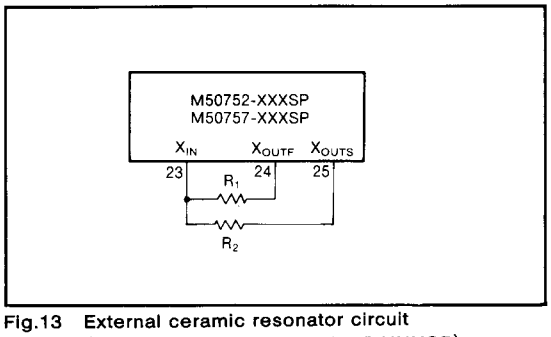


Fig.13 External ceramic resonator circuit (M50752-XXXSP and M50757-XXXSP)

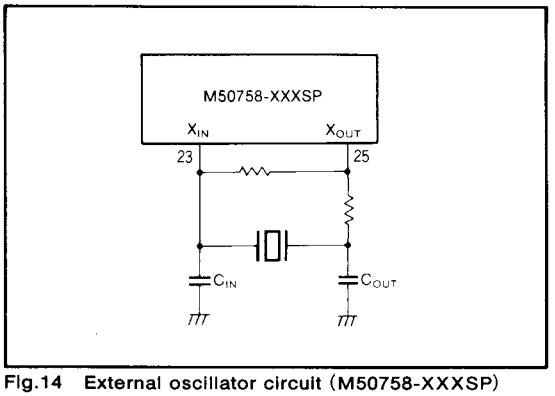


Fig.14 External oscillator circuit (M50758-XXXSP)

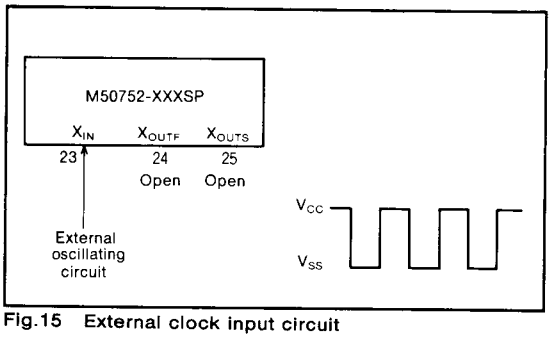


Fig.15 External clock input circuit

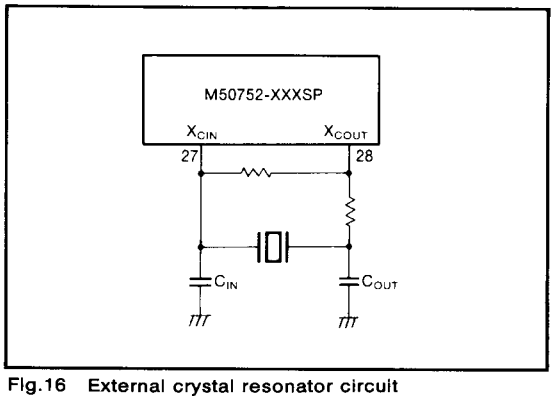


Fig.16 External crystal resonator circuit

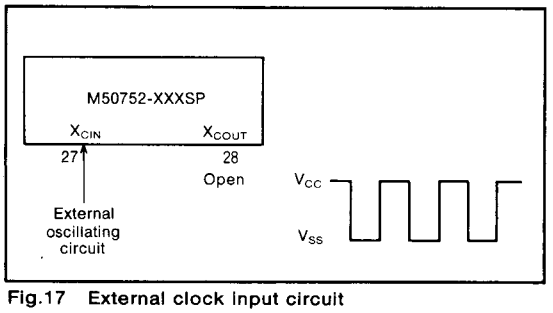


Fig.17 External clock input circuit

PROGRAMMING NOTES

(1) The frequency ratio of the timer and the prescaler is 1/(n+2).
(2) Set a value other than "0" for the timer and the prescaler.
(3) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
(4) Reading the timer and prescaler must be avoided while the input to the prescaler is changing.
(5) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.
(6) A NOP instruction must be used after the execution of a PLP instruction.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.
(1) mask ROM confirmation form
(2) mark specification form
(3) ROM data ..... EPROM 3sets

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power voltage	With respect to V_{SS}. Output transistors cut-off.	−0.3~7	V
V_P	Power voltage		V_{CC}−35~V_{CC}+0.3	V
V_I	Input voltage, R_3~R_0, CNV_{SS}, $\overline{RESET}$, X_{IN}, X_{CIN}		−0.3~7	V
V_I	Input voltage, $\overline{INT_1}$, $\overline{INT_2}$, $P0_0$~$P0_7$, $P2_5$~$P2_0$		−0.3~13	V
V_O	Output voltage, X_{OUTF}, X_{COUT}, X_{OUTS}, ϕ,		−0.3~V_{CC}+0.3	V
V_O	Output voltage, $\overline{INT_2}$, $P0_7$~$P0_0$, $P2_5$~$P2_0$		−0.3~13	V
V_O	Output voltage, $P1_7$~$P1_0$, $P3_7$~$P3_0$, $P2_7$, $P2_6$		V_{CC}−35~V_{CC}+0.3	V
P_d	Power dissipation	T_a = 25℃	1000	mW
T_{opr}	Operating temperture		−10~70	℃
Tstg	Storage temperature		−40~125	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −10~70℃, V_{CC} = 5V±10%, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Nom.	Max.	
V_{CC}	Power voltage	4.5	5.0	5.5	V
V_P	Power voltage	V_{CC}−33		V_{CC}	V
V_{SS}	Power voltage		0		V
V_{IH}	"H" input voltage, $P0_0$~$P0_7$, $P2_0$~$P2_5$, $\overline{INT_1}$, $\overline{INT_2}$	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage, CNV_{SS}, X_{CIN}, $\overline{RESET}$	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage, X_{IN}	0.9V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage, R_0~R_3	0.4V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage, $P0_0$~$P0_7$, $P2_0$~$P2_5$, CNV_{SS}, $\overline{INT_1}$, $\overline{INT_2}$, X_{CIN}	0		0.2V_{CC}	V
V_{IL}	"L" input voltage, $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage, R_0~R_3, X_{IN}	0		0.12V_{CC}	V
$f(X_{IN})$	Internal clock oscillating frequency			4	MHz

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, V_{SS} = 0V, $f(X_{IN})$ = 4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage, ϕ	V_{CC} = 5V, T_a = 25℃, I_{OH} = −2.5mA	3			V
V_{OH}	"H" output voltage, $P1_0$~$P1_7$, $P3_0$~$P3_7$, $P2_6$, $P2_7$	V_{CC} = 5V, T_a = 25℃, I_{OH} = −12mA	3			V
V_{OL}	"L" output voltage, ϕ	V_{CC} = 5V, T_a = 25℃, I_{OL} = 5mA			2	V
V_{OL}	"L" output voltage, $P0_0$~$P0_7$, $P2_0$~$P2_5$, $\overline{INT_2}$	V_{CC} = 5V, T_a = 25℃, I_{OL} = 10mA			2	V
V_{T+}−V_{T-}	Hysterisis, $\overline{INT_1}$, $\overline{INT_2}$	V_{CC} = 5V, T_a = 25℃	0.3		1	V
V_{T+}−V_{T-}	Hysterisis, $\overline{RESET}$	V_{CC} = 5V, T_a = 25℃		0.4	0.7	V
I_{OL}	"L" output current (Pull-down resistance) $P1_0$~$P1_7$, $P3_0$~$P3_7$, $P2_6$, $P2_7$	V_P = V_{CC}−33V, V_{OL} = V_{CC}, T_a = 25℃	150		900	μA
I_{IL}	input leakage current, $\overline{INT_1}$, $\overline{INT_2}$, $P0_0$~$P0_7$ $P2_0$~$P2_5$	V_{CC} = 5V, T_a = 25℃ 0≦ V_I ≦ 5V	−5		5	μA
I_{IL}	input leakage current, CNV_{SS}, $\overline{RESET}$, X_{IN} X_{CIN}, R_0~R_3	V_{CC} = 5V, T_a = 25℃ 0 ≦ V_I ≦ 5V	−5		5	μA
I_{IL}	input leakage current, $P1_0$~$P1_7$, $P3_0$~$P3_7$, $P2_6$, $P2_7$	V_{CC} = 5V, T_a = 25℃ V_{CC}−33 ≦ V_I ≦ V_{CC}, V_I = V_P	−33		33	μA
I_{CC}	Supply current	V_{CC}=5V, T_a=25℃ $P2_6$, $P2_7$: V_{CC}, Output pins open Input and I/O pins other than $P2_6$, $P2_7$: V_{SS}		3	6	mA

TIMING REQUIREMENTS

Single-chip mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time	270			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time	270			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time	270			ns
$t_{su(P3D-\phi)}$	Port P3 input setup time	270			ns
$t_{su(RD-\phi)}$	Port R input setup time	330			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time	0			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time	0			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	0			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time	0			ns
$t_{h(\phi-RD)}$	Port R input hold time	0			ns
t_C	External clock input cycle time	250			ns
t_W	External clock input puise width	75			ns
t_r	External clock rising edge			25	ns
t_f	External clock falling edge			25	ns

Memory expanding mode and eva-chip mode

(V_{CC}=5V±10%, V_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time	270			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time	270			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time	270			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time	0			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time	0			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	0			ns

Microprocessor mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P2D-\phi)}$	Port P2 input setup time	270			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	0			ns

SWITCHING CHARACTERISTICS

Single-chip mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=25°C, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
$t_{d(\phi-P0Q)}$	Port P0 data output delay time	Fig.18			230	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time	Fig.19			230	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time	Fig.18, Fig.19			230	ns
$t_{d(\phi-P3Q)}$	Port P3 data output delay time	Fig.19			200	ns

Memory expanding mode and eva-chip mode

(V_{CC}=5V±10%, V_{SS}=0V, T_a=25°C, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig.18			250	ns
$t_{d(\phi-P0AF)}$	Port P0 address output delay time				250	ns
$t_{d(\phi-P0Q)}$	Port P0 data output delay time				200	ns
$t_{d(\phi-P0QF)}$	Port P0 data output delay time				200	ns
$t_{d(\phi-P1A)}$	Port P1 address and control signal delay time	Fig.19			250	ns
$t_{d(\phi-P1AF)}$	Port P1 address and control signal delay time				250	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P1QF)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time	Fig.18, Fig.19			200	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				200	ns

Microprocessor mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=25°C, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig.18			250	ns
$t_{d(\phi-P1A)}$	Port P1 address and control signal delay time	Fig.19			250	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time	Fig.18, Fig.19			200	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				200	ns

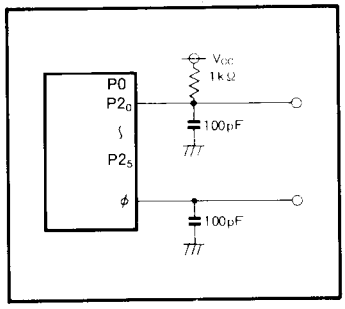


Fig.18 Port P0, $P2_0$~$P2_5$ test circuit

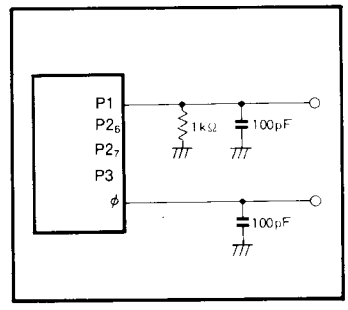
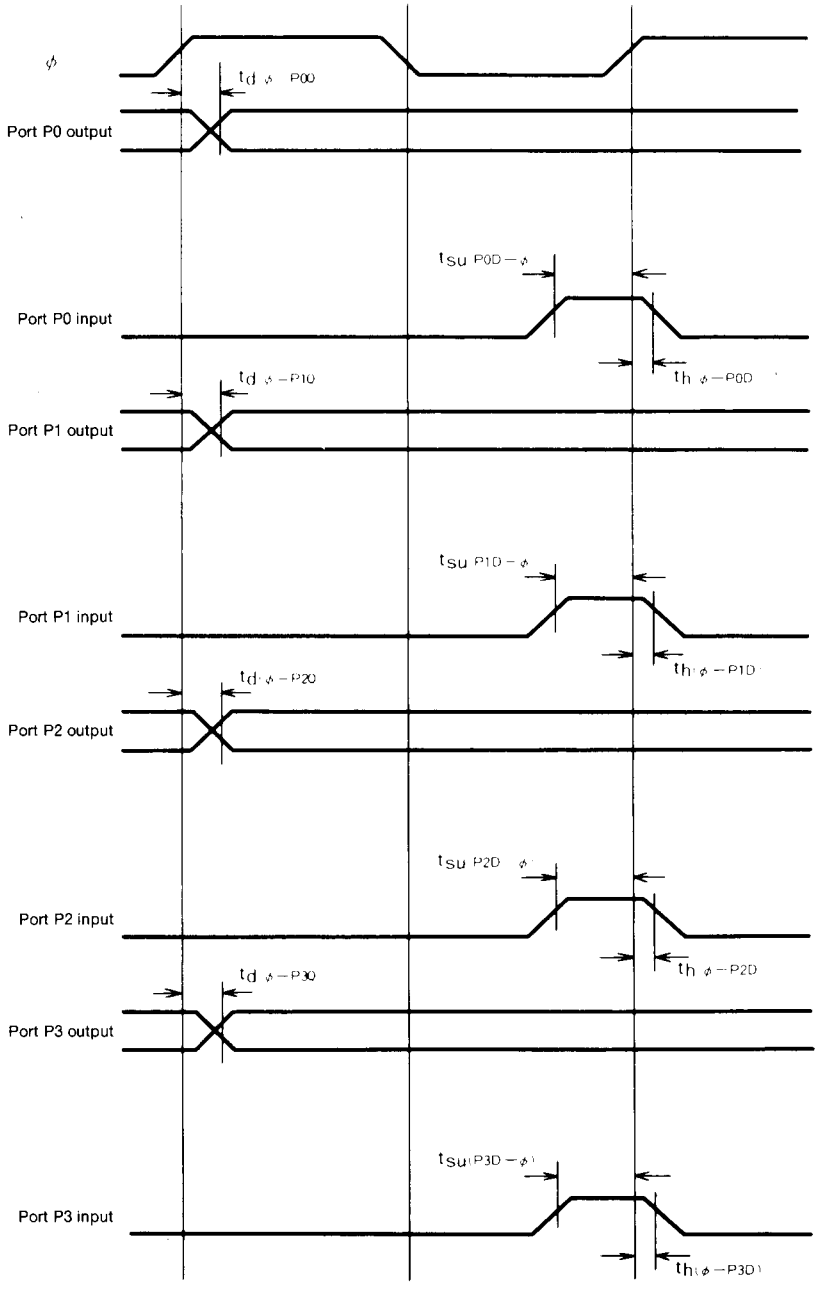


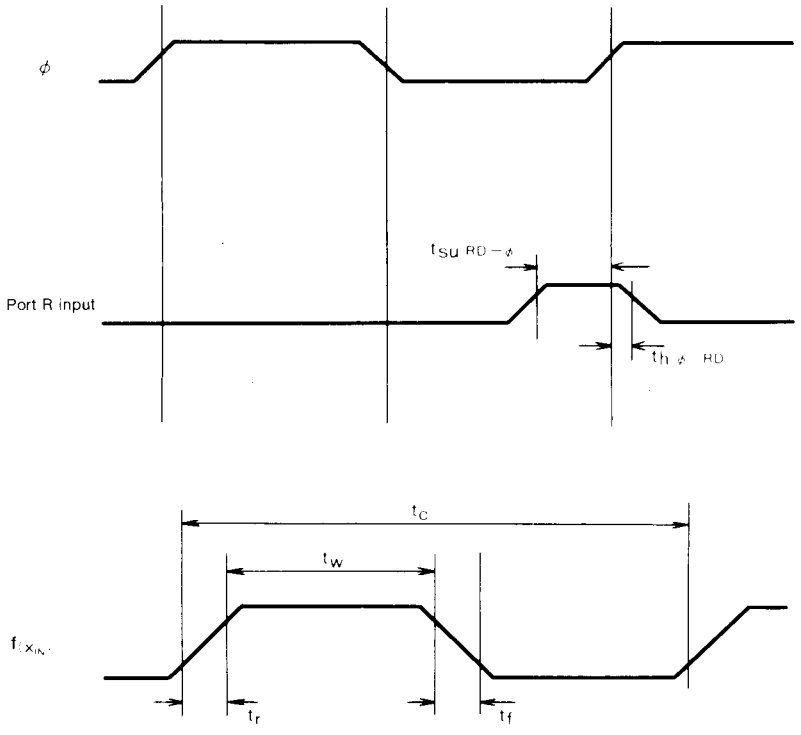
Fig.19 Port P1, $P2_6$, $P2_7$, P3 test circuit

TIMING DIAGRAMS

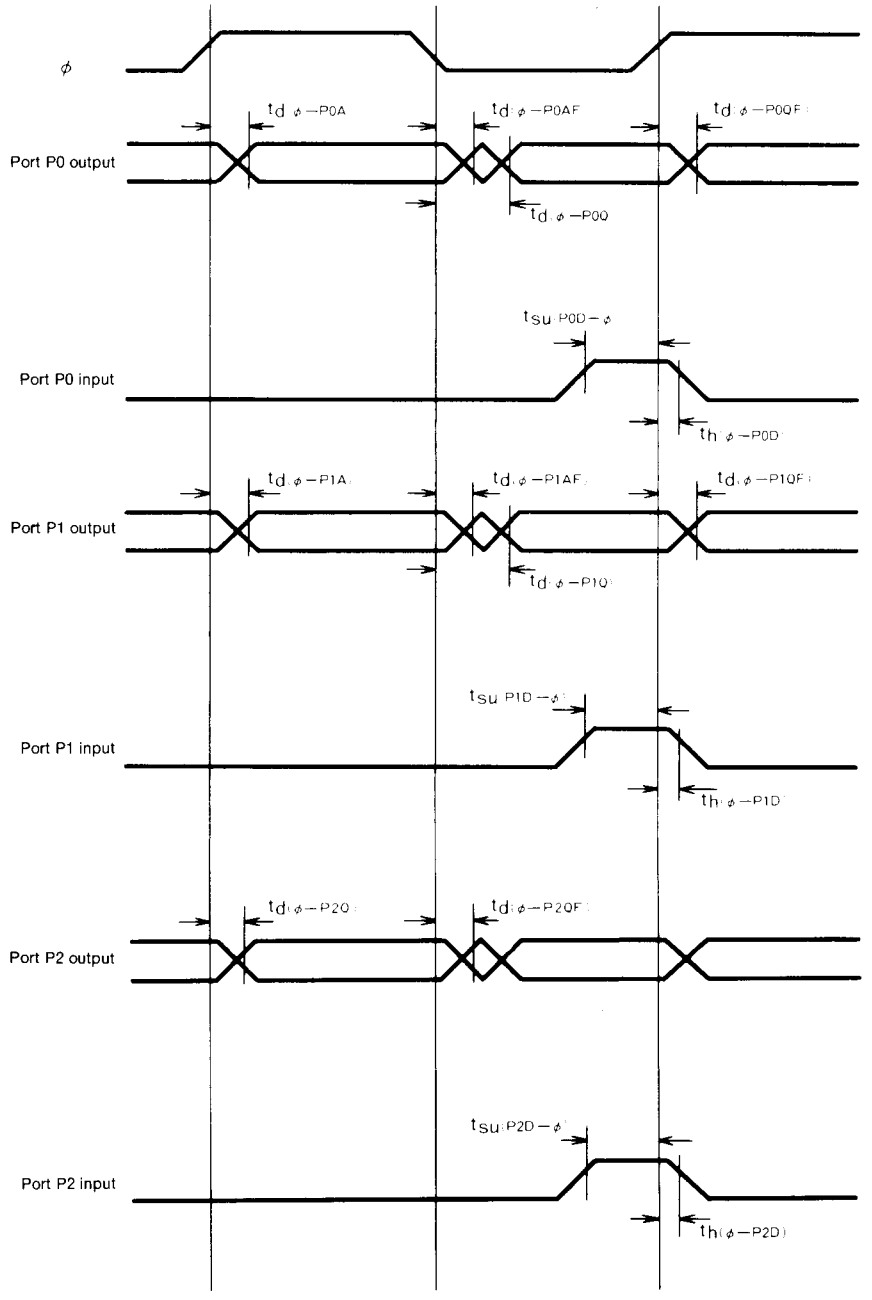
In single-chip mode



In single-chip mode (continued from the preceding page)



In memory expanding mode and eva-chip mode



In microprocessor mode