



# STP8NK85Z STF8NK85Z

## N-CHANNEL 850V -1.1Ω - 6.7A TO-220/TO-220FP Zener-Protected SuperMESH™ MOSFET

**Table 1: General Features**

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>	P <sub>w</sub>
STP8NK85Z	850 V	<1.4 Ω	6.7A	150 W
STF8NK85Z	850 V	<1.4 Ω	6.7A	35 W

- TYPICAL R<sub>DS(on)</sub> = 1.1Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- IMPROVED ESD CAPABILITY
- 100% AVALANCHE RATED
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEATIBILITY

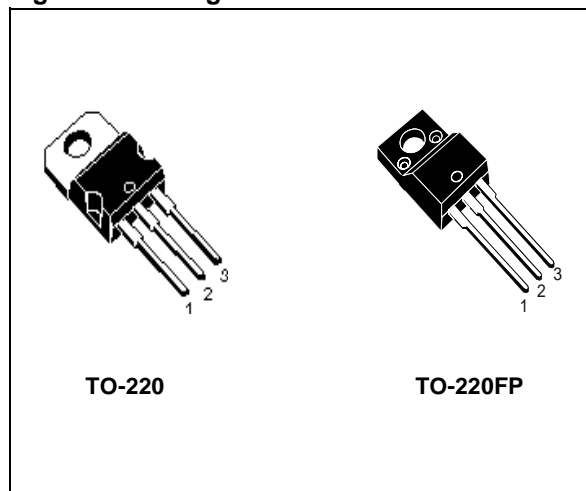
### DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

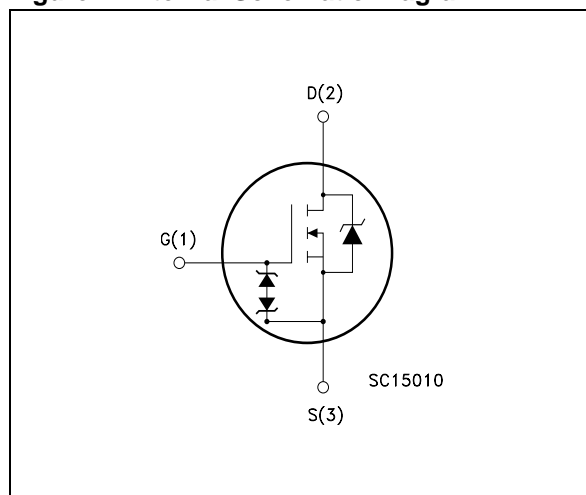
### APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- IDEAL FOR OFF-LINE POWER SUPPLIES
- SMPS

**Figure 1: Package**



**Figure 2: Internal Schematic Diagram**



**Table 2: Order Codes**

SALES TYPE	MARKING	PACKAGE	PACKAGING
STP8NK85Z	P8NK85Z	TO-220	TUBE
STF8NK85Z	F8NK85Z	TO-220FP	TUBE

**Table 3: Absolute Maximum ratings**

Symbol	Parameter	Value		Unit
		TO-220	TO-220FP	
$V_{DS}$	Drain-source Voltage ( $V_{GS} = 0$ )	850		V
$V_{DGR}$	Drain-gate Voltage ( $R_{GS} = 20\text{ k}\Omega$ )	850		V
$V_{GS}$	Gate- source Voltage	$\pm 30$		V
$I_D$	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	6.7	6.7 (*)	A
$I_D$	Drain Current (continuous) at $T_C = 100^\circ\text{C}$	4.3	4.3 (*)	A
$I_{DM}(\bullet)$	Drain Current (pulsed)	26.7	26.7 (*)	A
$P_{TOT}$	Total Dissipation at $T_C = 25^\circ\text{C}$	150	35	W
	Derating Factor	1.20	0.28	W/ $^\circ\text{C}$
$V_{ESD(G-S)}$	Gate source ESD(HBM-C=100pF, R=1.5K $\Omega$ )	4000		KV
dv/dt (1)	Peak Diode Recovery voltage slope	4.5		V/ns
$V_{ISO}$	Insulation Withstand Voltage (DC)	-	2500	V
$T_j$ $T_{stg}$	Operating Junction Temperature Storage Temperature	-55 to 150 -55 to 150		$^\circ\text{C}$ $^\circ\text{C}$

( $\bullet$ ) Pulse width limited by safe operating area

(1)  $I_{SD} \leq 6.7\text{A}$ ,  $di/dt \leq 200\text{A}/\mu\text{s}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$

(\*) Limited only by maximum temperature allowed

**Table 4: Thermal Data**

		TO-220	TO-220FP	
Rthj-case	Thermal Resistance Junction-case Max	0.83	3.6	$^\circ\text{C}/\text{W}$
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5		$^\circ\text{C}/\text{W}$
$T_l$	Maximum Lead Temperature For Soldering Purpose	300		$^\circ\text{C}$

**Table 5: Avalanche Characteristics**

Symbol	Parameter	Max Value	Unit
$I_{AR}$	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by $T_j$ max)	6.7	A
$E_{AS}$	Single Pulse Avalanche Energy (starting $T_j = 25^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{V}$ )	350	mJ

**Table 6: Gate-Source Zener Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$BV_{GSO}$	Gate-Source Breakdown Voltage	$I_{gs} = \pm 1\text{mA}$ (Open Drain)	30			V

## PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

**ELECTRICAL CHARACTERISTICS** ( $T_{CASE} = 25^{\circ}C$  UNLESS OTHERWISE SPECIFIED)**Table 7: On/Off**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 1 \text{ mA}, V_{GS} = 0$	850			V
$I_{DSS}$	Zero Gate Voltage Drain Current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}, T_C = 125^{\circ}C$			1 50	$\mu A$ $\mu A$
$I_{GSS}$	Gate-body Leakage Current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20V$			$\pm 10$	$\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 100\mu A$	3	3.75	4.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10V, I_D = 3.35 \text{ A}$		1.1	1.4	$\Omega$

**Table 8: DYNAMIC**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs}$ (1)	Forward Transconductance	$V_{DS} = 15 \text{ V}, I_D = 3.35 \text{ A}$		6		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25V, f = 1 \text{ MHz}, V_{GS} = 0$		1870 190 44		pF pF pF
$C_{oss \text{ eq.}}$ (3)	Equivalent Output Capacitance	$V_{GS} = 0V, V_{DS} = 0V \text{ to } 680V$		75		pF
$t_{d(on)}$ $t_r$ $t_{d(off)}$ $t_f$	Turn-on Delay Time Rise Time Turn-off Delay Time Fall Time	$V_{DD} = 425 \text{ V}, I_D = 3.35 \text{ A}$ $R_G = 4.7\Omega, V_{GS} = 10 \text{ V}$ (see Figure 19)		26 19 58 18		ns ns ns ns
$t_{r(Voff)}$ $t_f$ $t_c$	Off-voltage Rise Time Fall Time Cross-over Time	$V_{DD} = 680 \text{ V}, I_D = 6.7 \text{ A},$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see Figure 20)		12 10 24		ns ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 680V, I_D = 6.7 \text{ A},$ $V_{GS} = 10V$ (see Figure 22)		60 12 35	84	nC nC nC

**Table 9: Source Drain Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM}$ (2)	Source-drain Current Source-drain Current (pulsed)				6.7 26.7	A A
$V_{SD}$ (1)	Forward On Voltage	$I_{SD} = 6.7 \text{ A}, V_{GS} = 0$			1.6	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 6.7 \text{ A}, di/dt = 100A/\mu s$ $V_{DD} = 35V, T_j = 25^{\circ}C$ (see Figure 20)		530 4.5 17		ns $\mu C$ A
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 6.7 \text{ A}, di/dt = 100A/\mu s$ $V_{DD} = 35V, T_j = 150^{\circ}C$ (see Figure 20)		690 6.4 17		ns $\mu C$ A

Note: 1. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5 %.

2. Pulse width limited by safe operating area.

3.  $C_{oss \text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

Figure 3: Safe Operating Area for TO-220

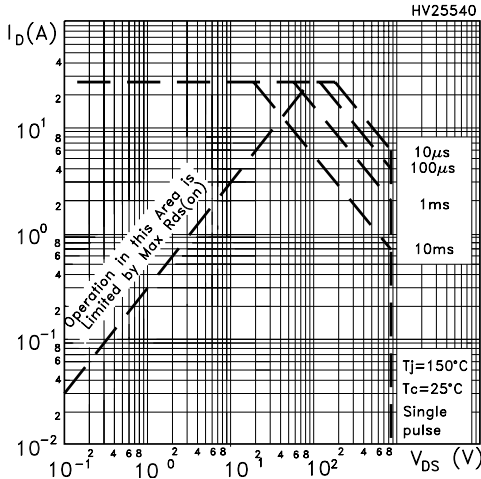


Figure 4: Safe Operating Area for TO-220FP

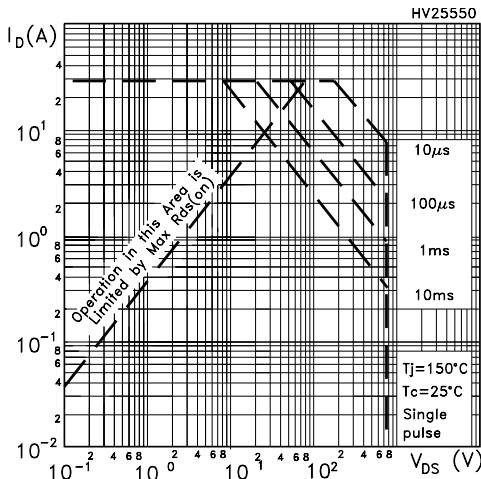


Figure 5: Output Characteristics

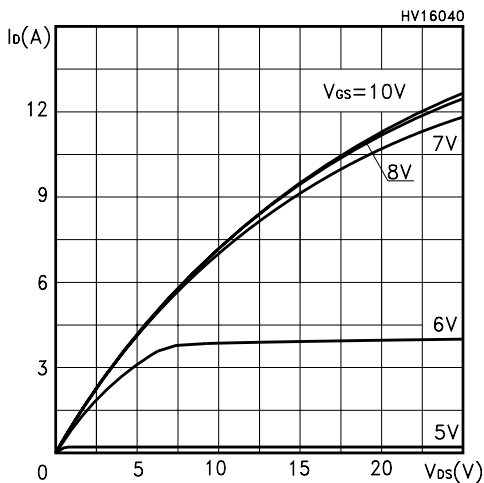


Figure 6: Thermal Impedance for TO-220

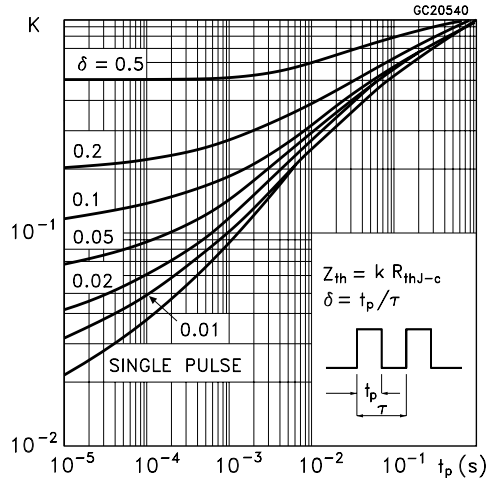


Figure 7: Thermal Impedance for TO-220FP

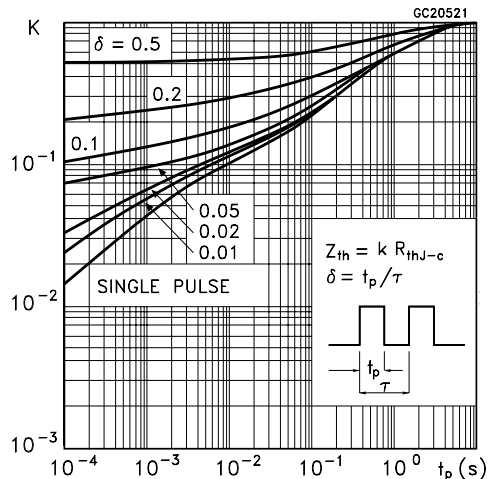


Figure 8: Transfer Characteristics

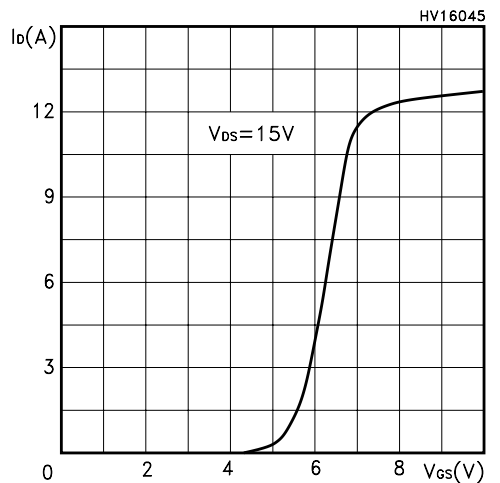


Figure 9: Transconductance

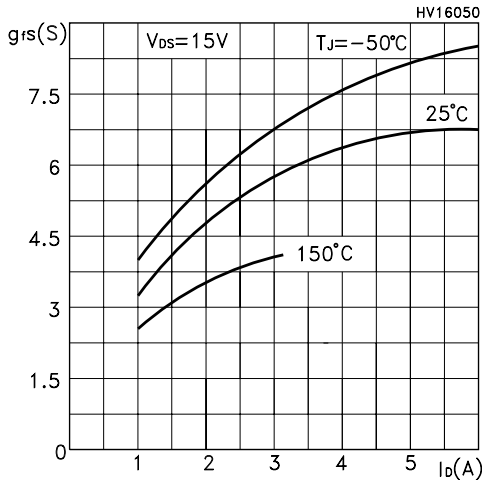


Figure 10: Gate Charge vs Gate-source Voltage

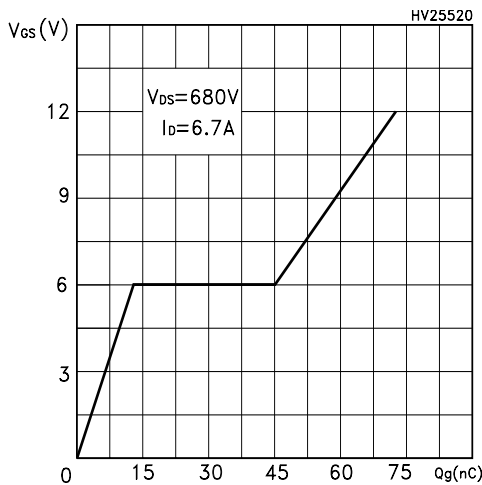


Figure 11: Normalized Gate Threshold Voltage vs Temperature

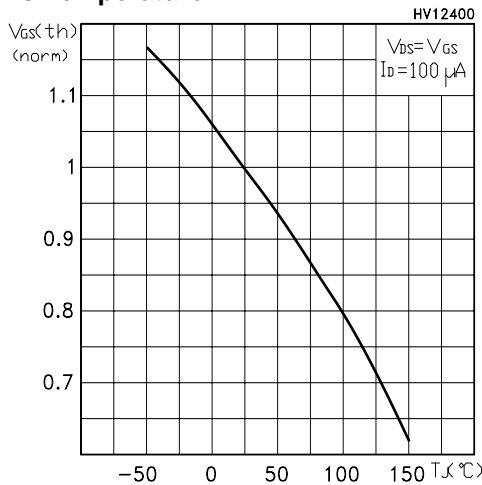


Figure 12: Static Drain-source On Resistance

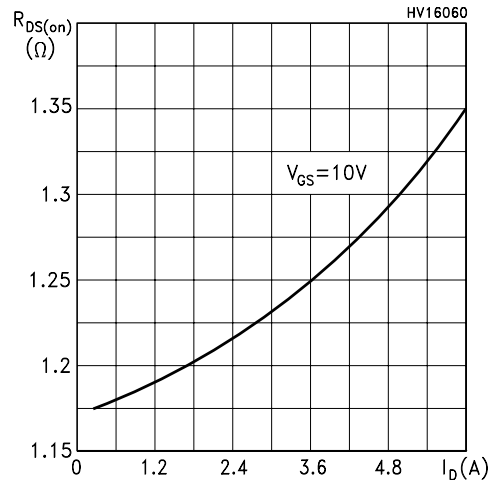


Figure 13: Capacitance Variations

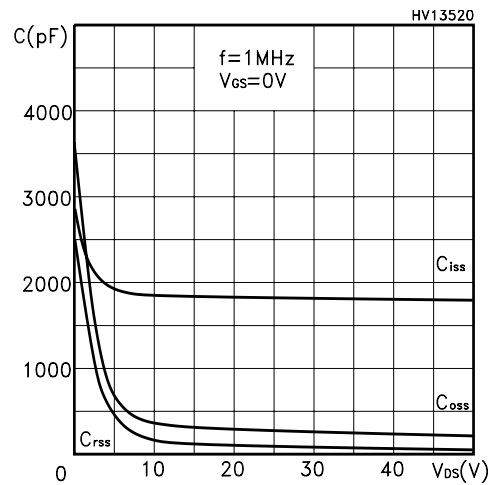


Figure 14: Normalized BV\_DS vs Temperature

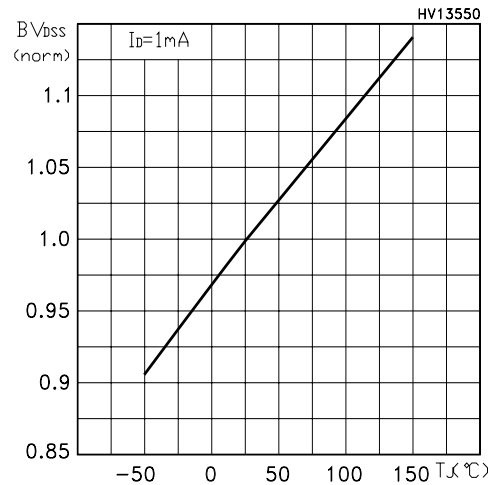


Figure 15: Normalized On Resistance vs TemperatureS

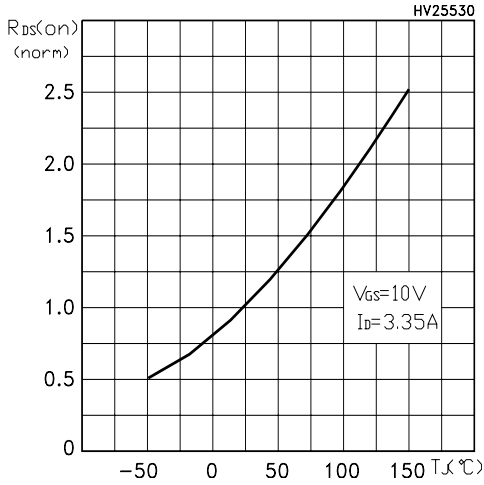


Figure 16: Avalanche Energy vs Temperature

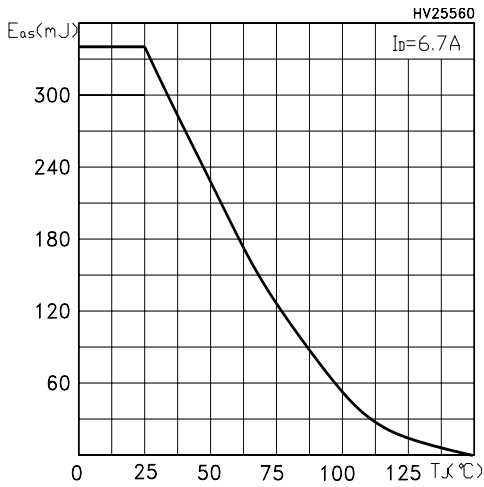


Figure 17: Source-Drain Diode Forward Characteristics

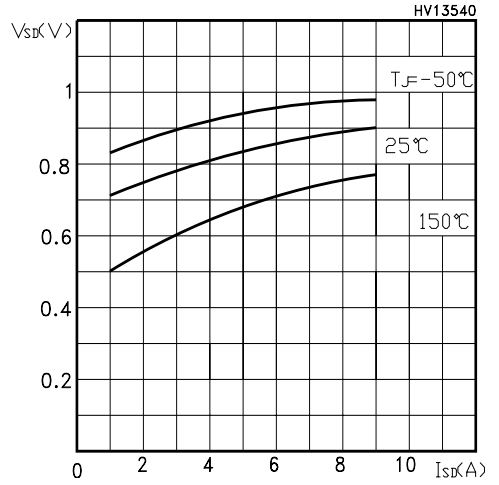


Figure 18: Unclamped Inductive Load Test Circuit

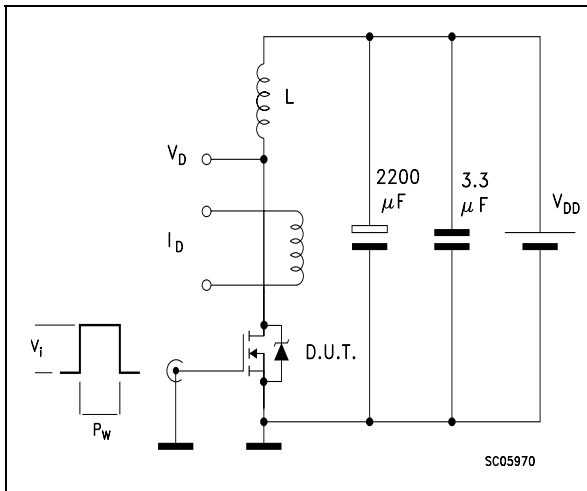


Figure 19: Switching Times Test Circuit For Resistive Load

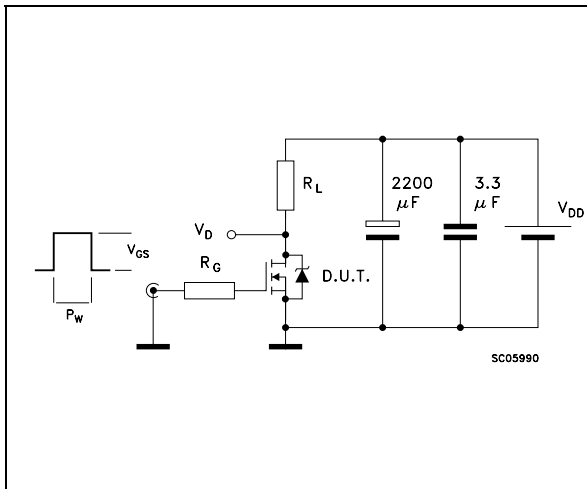


Figure 20: Test Circuit For Inductive Load Switching and Diode Recovery Times

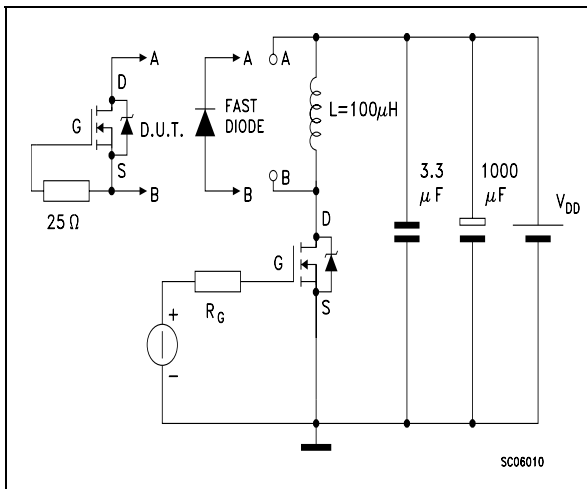


Figure 21: Unclamped Inductive Waferform

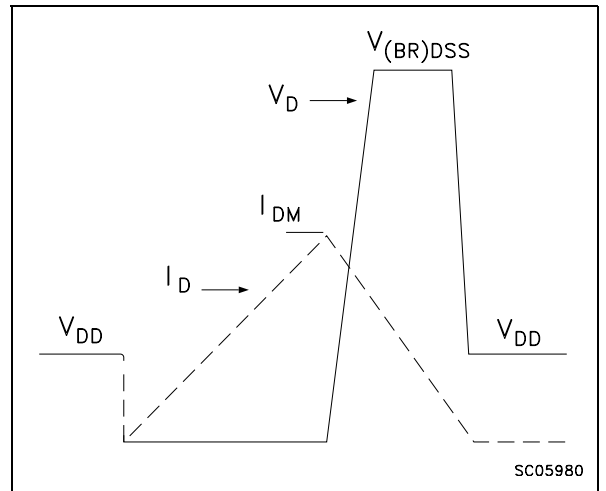


Figure 22: Gate Charge Test Circuit

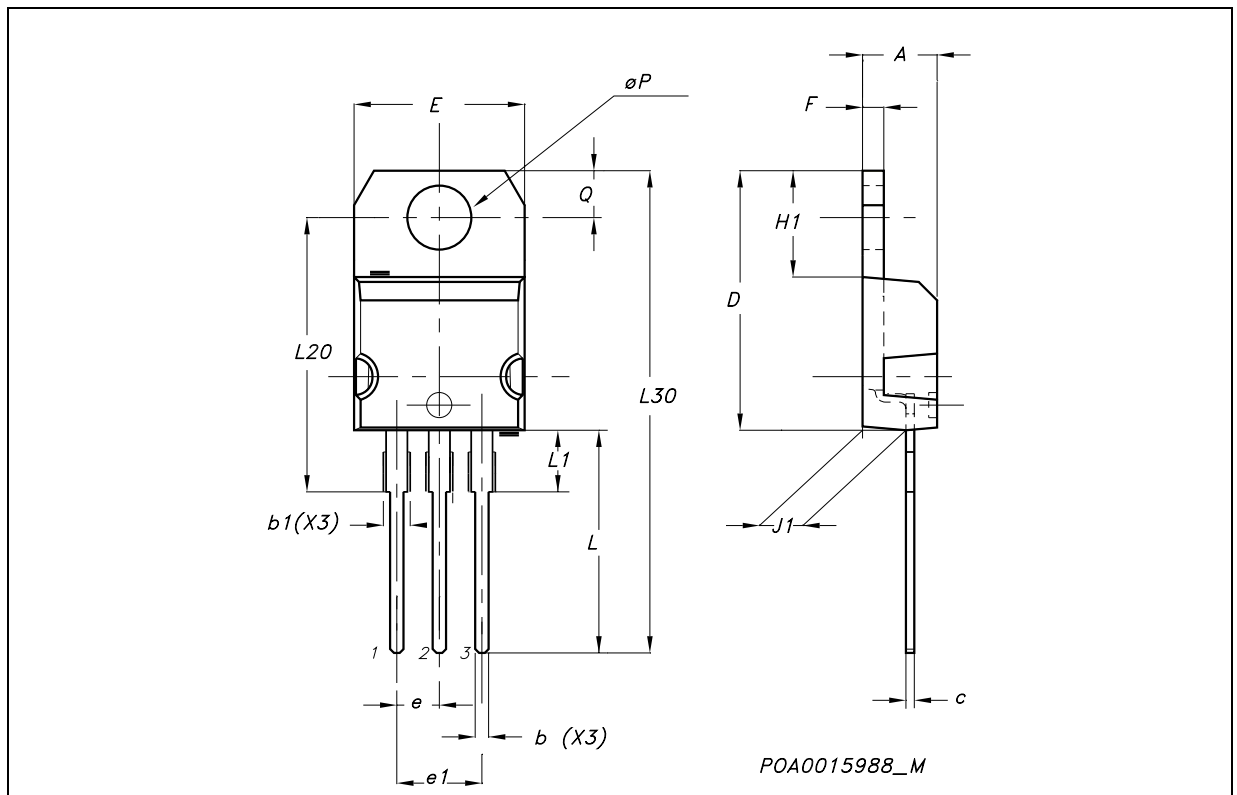


In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)



## TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
$\varnothing P$	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116





**Table 10: Revision History**

<b>Date</b>	<b>Revision</b>	<b>Description of Changes</b>
02-Mar-2005	1	First Release.
03-Mar-2005	2	Modified value in table 7
26-Apr-2005	3	Modified values in table 8 and inserted curves. Final datasheet.
09-May-2005	4	Modified note1 and Application Scope
06-Sep-2005	5	Inserted Ecopack indication

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