

MPC565/MPC566

Product Brief

MPC565/MPC566 RISC MCU with Code Compression Option

Features

The MPC565 / MPC566 key features are as follows. The information inside boxes are optional features.

- **40 MHz / 56 MHz operation**

- **56 MHz operation is available as an option.**

- -40° – 125 °C ambient temperature

- 2.6 V ± 0.1 V external bus

- External bus is compatible with external memory devices operating from 2.5 V to 3.4 V.

- Extended voltage range (2.7 – 3.4 V) degrades data drive timing by 1.1 ns on data writes.

- 2.6 ± 0.1 V internal logic

- 5-V I/O (5.0 ± 0.25 V)

- **High performance RISC CPU system**

- High performance core

- Single issue integer core

- Instruction set compatible with PowerPC instruction set architecture

- Precise exception model

- Floating point

- Code compression supported on the MPC566

- Compression reduces usage of internal or external flash memory

- Compression optimized for automotive (non-cached) applications

- New compression scheme increases compression performance to 40% – 50% compression

- 4-Kbyte static DECRAM can be used as memory if Compression is not used.

- General-purpose I/O support

- On address (24) and data (32) pins

- 16 GPIO in MIOS14

- Many peripheral pins can be used as GPIO when not used as primary functions

- 2.6-V outputs on external bus pins

- Extensive system development support

- On-chip watchpoints and breakpoints

- Program flow tracking

- Background debug mode (BDM)

Key Feature Details

MPC500 System Interface (USIU, BBC, L2U)

- Periodic interrupt timer, bus monitor, clocks, decremter and time base

- Clock synthesizer, power management, reset controller

- External bus tolerates 5-V inputs, provides 3.3-V outputs

- Enhanced interrupt controller supports a separate interrupt vector for up to eight external and 40 Internal interrupts

- IEEE 1149.1 JTAG test access port
- Bus supports multiple master designs
- Flexible memory protection units in BBC (IMPU) and L2U (DMPU)
- Flexible chip selects via memory controller
 - 24-bit address and 32-bit data buses
 - Four- to 16-Mbyte (data) or 4-Gbyte (instruction) region size support
 - Four-beat transfer bursts, two-clock minimum bus transactions
 - Use with SRAM, EPROM, flash and other peripherals
 - Byte selects or write enables
 - 32-bit address decodes with bit masks
 - Four instruction regions
 - Four data regions
- Default attributes available in one global entry
- Attribute support for speculative accesses
- Exception vector table relocation features allow exception table to be relocated to following locations:
 - 0x0000 0100 (normal MPC5xx exception table location)
 - 0x0001 0000 (0 + 64 Kbytes; second page of internal flash)
 - Second internal flash module
 - Internal SRAM
 - 0x0FFF_0100 (external memory space; normal MPC5xx exception table location)
- USIU supports dual-mapping of flash to move part of internal flash memory to external bus for development

One Mbyte Flash

- Two UC3F modules, 512 Kbytes each
- Page mode read
- Block (64-Kbyte) erasable
- External 4.75- to 5.25-V V_{PP} program, erase, and read power supply

36-Kbyte Static RAM (CALRAM)

- Composed of four- and 32-Kbyte CALRAM modules
- Fast access: one clock
- Keep-alive power
- Soft defect detection (SDD)
- 4-Kbyte calibration (overlay) RAM per module (eight Kbytes total)
- Eight 512-byte overlay regions per module (16 regions total)

IEEE – ISTO Nexus 5001-1999 Debug Port (Class 3)

- Address (24) and data (32) pins can be used as GPIO in single chip mode
- Reduced-port mode (1 MDI, 2 MDo) or full-port mode (2 MDI, 8 MDO)
- Many peripheral pins can be used as GPIO when not used as primary functions
- 5-V outputs with slew rate control

Integrated I/O System

- True 5-V I/O
- Three time processing units (TPU3)
 - 16 channels each
 - Each TPU3 is a microcoded timer subsystem
 - One 6-Kbyte and one 4-Kbyte dual port TPU RAM (DPTRAM), one (6-Kbyte) shared by two TPU3 modules for TPU microcode and the 4-Kbyte dedicated to the third TPU3 for microcode.

22-Channel MIOS timer (MIOS14)

- Six modulus counter sub-module (MCSM)
 - Four additional MCSM submodules compared to MIOS1
- 10 double action sub-module (DASM).
- 12 dedicated PWM sub-modules (PWMSM)
 - Four additional PWM submodules compared to MIOS1 (shared with MIOS GPIO pins)
- Real-time clock sub-module (MRTCSCM) provides low power clock/counter
 - Requires external 32-KHz crystal
 - Uses four pins: two for 32-KHz crystal, two for power/ground.

Two Queued Analog-to-Digital Converter Modules (QADC64E_A, QADC64E_B)

- AMUXes providing a total of 40 analog channels.
- 40 total input channels on the two modules with internal multiplexing (AMUXes)
- Each QADC64E can see all 40 input channels
- 10 bit A/D converter with internal sample/hold
- Typical conversion time is 4 μ s (250-Kbyte samples/sec)
- Two conversion command queues of variable length
- Automated queue modes initiated by:
 - External edge trigger/level gate
 - Software command
 - Periodic/interval timer, assignable to both queue 1 and 2
- 64 result registers in each QADC64E module
- Conversions alternate reference (ALTREF) pin. This pin can be connected to a different reference voltage
- Output data is right or left justified, signed or unsigned

Message Data Link Controller (DLCMD2) Module

- Two pins muxed with QSMCM_B pins. Muxing controlled by QSMCM_B PCS3 pin assignment register
- SAE J1850 Class B data communications network interface compatible and ISO compatible for low-speed (< 125 Kbps) serial data communications in automotive applications
- 10.4 Kbps variable pulse width (VPW) bit format
- Digital noise filter, collision detection
- Hardware cyclical redundancy check (CRC) generation and checking
- Block mode receive and transmit supported
- 4X receive mode supported (41.6 Kbps)
- Digital loopback mode
- In-frame response (IFR) types 0, 1, 2, and 3 supported
- Dedicated register for symbol timing adjustments
- Inter-module bus 3 (IMB3) slave interface
- Power-saving IMB3 stop mode with automatic wakeup on network activity
- Power-saving IMB3 CLOCKDIS mode
- Debug mode available through IMB3 FREEZE signal or user controllable SOFT_FRZ bit
- Polling and IMB3 interrupt generation with vector lookup available

Three TouCAN™ Modules (TOUCAN_A, TOUCAN_B, TOUCAN_C)

- 16 message buffers each, programmable I/O modes
- Maskable interrupts
- Programmable loop-back for self test operation
- Independent of the transmission medium (external transceiver is assumed)
- Open network architecture, multimaster concept
- High immunity to EMI
- Short latency time for high-priority messages
- Low power sleep mode, with programmable wake up on bus activity

- TOUCAN_C pins shared with MIOS14 GPIO pins

Two Queued Serial Modules with One Queued-SPI and two SCI Each (QSMCM_A, QSMCM_B)

- QSMCM_A matches full MPC555/MPC556 QSMCM functionality
- QSMCM_B has pins muxed with DLCMD2 module
 - Two pins are muxed with DLCMD2 (J1850) transmit and receive pins (B_PCS3_J1850_TX and B_RXD2_J1850_RX)
 - QSMCM_B vs J1850 mux control provided by QPAPCS3 bit in QSMCM pin assignment register (PQSPAR)
- Queued-SPI
 - Provides full-duplex communication port for peripheral expansion or interprocessor communication
 - Up to 32 preprogrammed transfers, reducing overhead
 - Synchronous serial interface with baud rate of up to system clock / 4
 - Four programmable peripheral-selects pins support up to 16 devices
 - Special wrap-around mode allows continuous sampling of a serial peripheral for efficient interfacing to serial analog-to-digital (A/D) converters
- SCI
 - UART mode provides NRZ format and half- or full-duplex interface
 - 16 register receive buffer and 16 register transmit buffer on one SCI
 - Advanced error detection, and optional parity generation and detection
 - word length programmable as eight or nine bits
 - Separate transmitter and receiver enable bits, and double buffering of data
 - Wake-up functions allow the CPU to run uninterrupted until either a true idle line is detected, or a new address byte is received
 - External source clock for baud generation
- **Available in package**
 - **Plastic ball grid array (PBGA) packaging**
 - 352/388 ball PBGA
 - 27 mm x 27 mm body size
 - 1.0 mm ball pitch

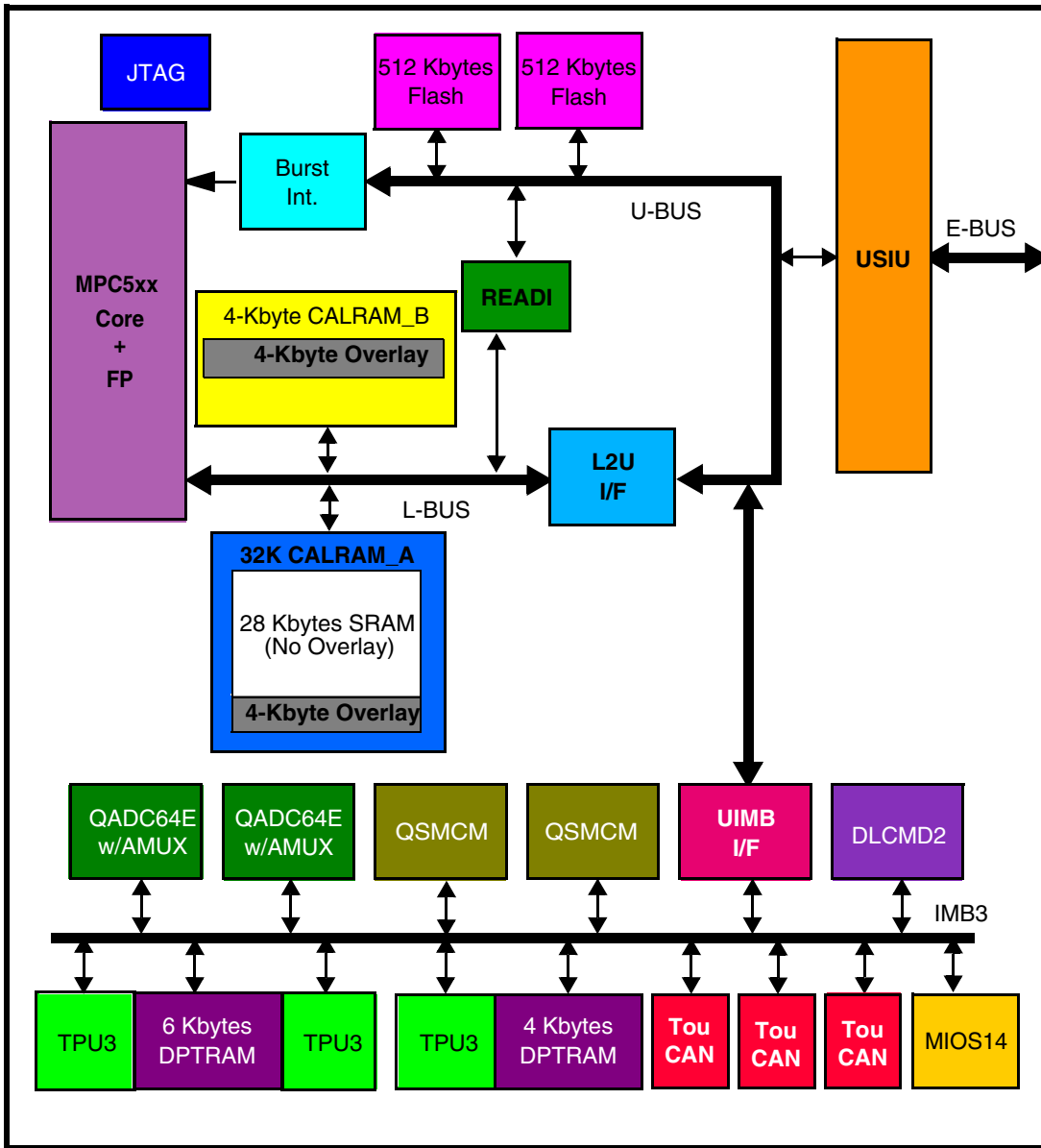


Figure 1 MPC565/MPC566 Block Diagram

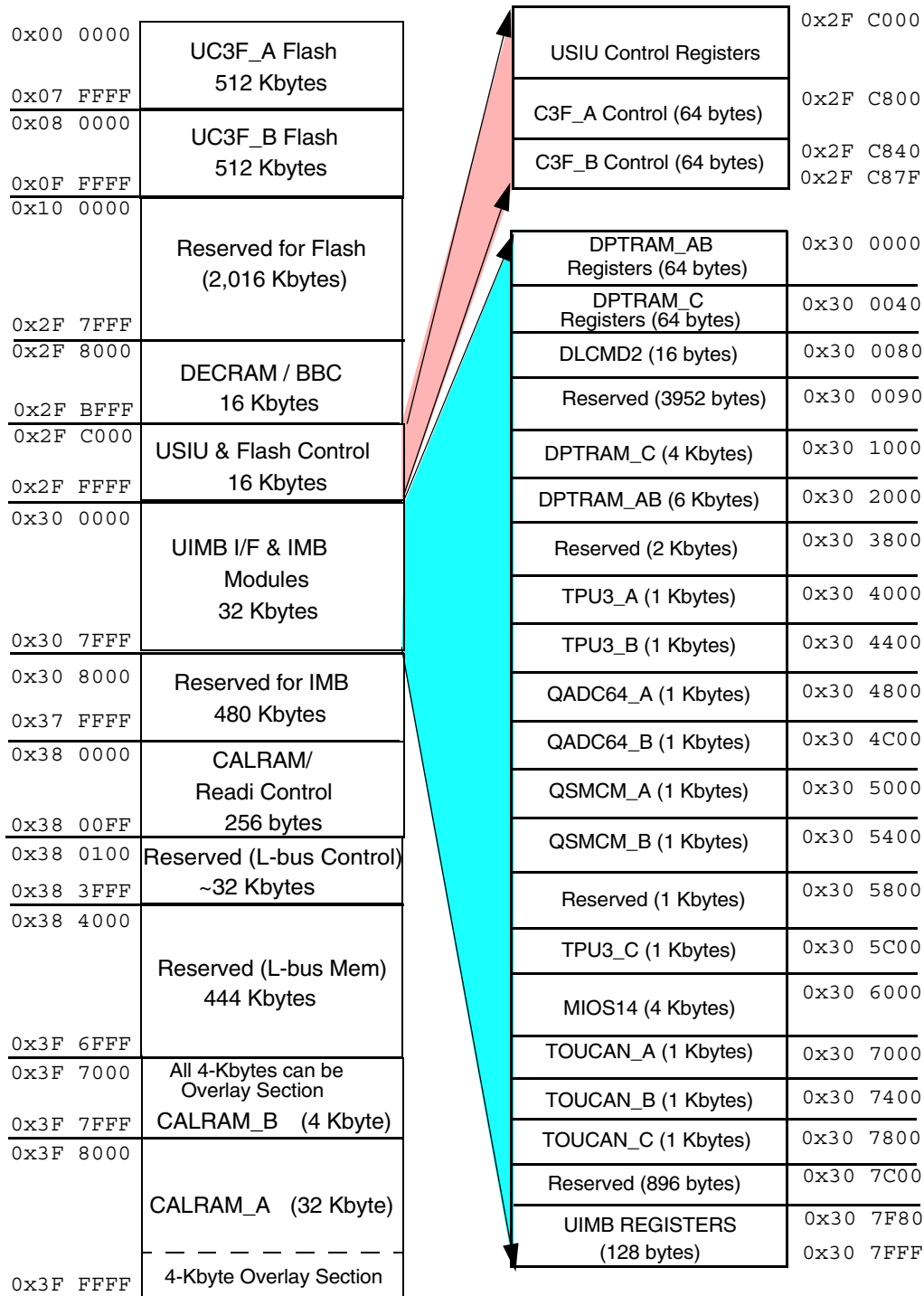


Figure 2 MPC565 / MPC566 Internal Memory Block

Ordering Information

Table 1 MPC565 / MPC566

Device Name	Order Part Number ¹	Package Info	Temperature Range	Maximum Frequency	Code Compression
MPC565	MPC565MZP40	388 PBGA	-40 – 125° C	40 MHz	No
MPC565	MPC565CZP40	388 PBGA	-40 – 85° C	40 MHz	No
MPC565	MPC565MZP56	388 PBGA	-40 – 125° C	56 MHz	No
MPC565	MPC565CZP56	388 PBGA	-40 – 85° C	56 MHz	No
MPC566	MPC566MZP40	388 PBGA	-40 – 125° C	40 MHz	Yes
MPC566	MPC566CZP40	388 PBGA	-40 – 85° C	40 MHz	Yes
MPC566	MPC566MZP56	388 PBGA	-40 – 125° C	56 MHz	Yes
MPC566	MPC566CZP56	388 PBGA	-40 – 85° C	56 MHz	Yes

NOTES:


1. Add R2 suffix for parts shipped in tape and reel media.

Table 2 lists the documents that provide a complete description of the MPC565/566 and are required to design properly with the part. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, a Motorola Literature Distribution Center, or through the Motorola Semiconductor documentation page on the Internet (the source for the latest information).

Table 2 Available Documentation

Document Number	Title
MPC565RM/D	MPC565/MPC566 Reference Manual
AN1821/D	Exception Table Relocation and Multi-Processor Address Mapping in the Embedded MPC5XX Family
AN2002/D	MPC565/566 Nexus Interface Connector Options
AN2109/D	MPC555 Interrupts
AN2127/D	EMC Guidelines for MPC500-Based Automotive Powertrain Systems

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