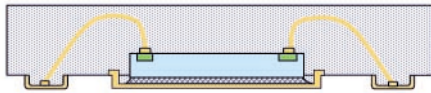


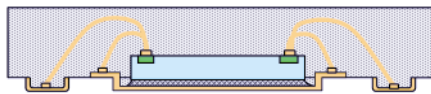
BCC

Bump Chip Carrier

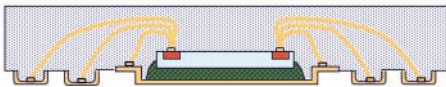
BCC+ (exposed paddle without ground ring)



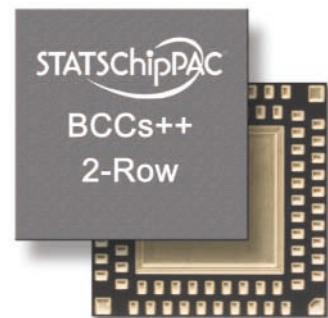
BCC++ (exposed paddle with ground ring)



BCCs++ (staggered dual row design)



- Saw singulated format
- Package height 0.8mm max.
- Square body size (rectangular body designable)
- Staggered dual row or single row bump design



FEATURES

- Body sizes: 4 x 4mm to 9 x 9mm
- Lead pitch: 0.50mm and 0.80mm
- Custom body / lead / pitch configurations available
- Package profile heights (overall): maximum 0.80mm
- Both single row & dual row design
- Ni / Pd / Au plated bumps
- Excellent thermal and electrical performance
- Full in-house package and leadframe design capability
- Full in-house electrical, thermal and mechanical simulation and measurement capability
- JEDEC standard compliant

APPLICATIONS

- RF
- Power Management
- Analog/Linear
- Logic
- Applications requiring enhanced electrical and thermal performance and reduced package size and weight

DESCRIPTION

STATS ChipPAC's Bump Chip Carrier (BCC) technology produces a chip scale leadframe based molded package with bumps which are formed after the leadframe is etched away. An exposed die pad coupled with extremely low RLC provides excellent electrical and thermal performance enhancements which are ideal for high frequency and high power applications especially for handheld portable applications such as cell phones. The BCC is manufactured in a molded array format that maximizes product throughput and material utilization. The BCC is available with single row and dual row bumps in BCC++ and BCC+. Overall package profile height is 0.80mm maximum.

Bump Chip Carrier

SPECIFICATIONS

Die Thickness	279µm nominal, 355µm max.
Gold Wire	25µm (1.0mils) diameter
Lead Finish	Preplated Ni/Pd/Au bumps
Marking	Laser
Packing Options	Tape & reel / JEDEC tray

RELIABILITY

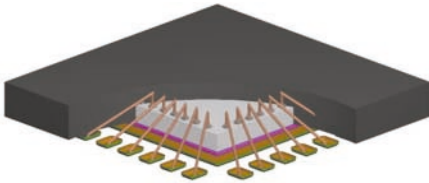
Moisture Sensitivity Level	JEDEC Level 2a/2/1@260°C (depending upon package)
Temperature Cycling	-65°C/150°C, 1000 cycles
High Temp Storage	150°C, 1000 hrs
Temp / Humidity Test	85°C/85% RH, 1000 cycles
Pressure Cooker Test	121°C, 100% RH, 2 atm, 168 hrs

PACKAGE CONFIGURATIONS

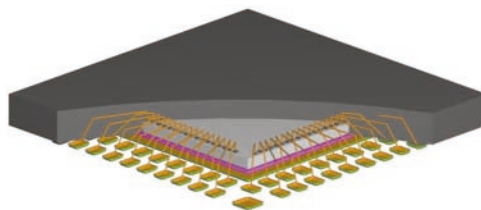
Package Size (mm)	Lead Pitch (mm)	Lead Count
4 x 4	0.80	16
5 x 5	0.50	32
6 x 6	0.50	40
7 x 7	0.50	48 / 84
8 x 8	0.50	56
9 x 9	0.50	116

CROSS-SECTIONS

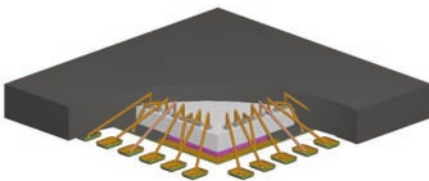
BCC+



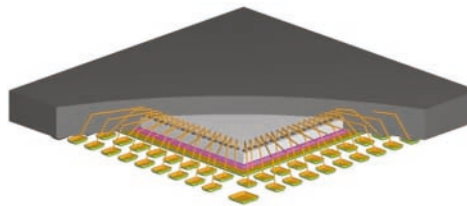
BCCs+



BCC++



BCCs++



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