

BGA
Commercial Temp
Industrial Temp

256K x 32 8Mb Asynchronous SRAM

10, 12, 15ns
3.3V V_{DD}

Features

- Fast access time: 10, 12, 15ns.
- CMOS low power operation: 340/290/260/220mA at min. cycle time.
- Single 3.3V ± 0.3V power supply.
- All inputs and outputs are TTL compatible.
- Byte control.
- Fully static operation.
- Industrial Temperature Option: -40° to 85°C.
- 14mm x 22mm, 119 Bump, 1.27mm Pitch Ball Grid Array package.

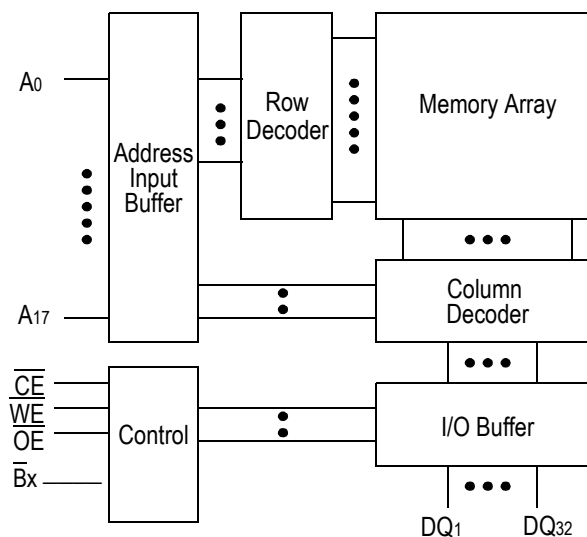
Description

The GS78132 is a high speed CMOS static RAM organized as 262,144-words by 32-bits. Static design eliminates the need for external clocks or timing strobes. Operating on a single 3.3V power supply and all inputs and outputs are TTL compatible. The GS78132 is available in 14mm x 22mm BGA package.

Pin Descriptions

| Symbol | Description |
|--------------------------------------|--------------------------|
| A ₀ to A ₁₇ | Address input |
| $\overline{\text{CE}}$ | Chip enable input |
| DQA ₁ TO DQA ₈ | Byte A Data input/output |
| DQB ₁ TO DQB ₈ | Byte B Data input/output |
| DQC ₁ TO DQC ₈ | Byte C Data input/output |
| DQD ₁ TO DQD ₈ | Byte D Data input/output |
| $\overline{\text{BA}}$ | Byte A Byte enable input |
| $\overline{\text{BB}}$ | Byte B Byte enable input |
| $\overline{\text{BC}}$ | Byte C Byte enable input |
| $\overline{\text{BD}}$ | Byte D Byte enable input |
| $\overline{\text{WE}}$ | Write enable input |
| $\overline{\text{OE}}$ | Output enable input |
| V _{DD} | +3.3V power supply |
| V _{SS} | Ground |
| NC | No connect |

Block Diagram



256K x 32 Async SRAM in 119 Bump, 14x22mmBGA

Top View

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|------------------|------|------------|------------------|------------|------|------------------|
| A | NC | A15 | A14 | A16 | A13 | A12 | NC |
| B | $\overline{B_C}$ | A11 | A10 | $\overline{C_E}$ | A9 | A8 | $\overline{B_B}$ |
| C | DQC6 | NC | VDD, NC | A17 | VSS, NC | NC | DQB6 |
| D | DQC5 | VDD | VSS | VSS | VSS | VDD | DQB5 |
| E | DQC4 | DQC8 | VDD | VSS | VDD | DQB8 | DQB4 |
| F | DQC3 | VDD | VSS | VSS | VSS | VDD | DQB3 |
| G | DQC2 | DQC7 | VDD | VSS | VDD | DQB7 | DQB2 |
| H | DQC1 | VDD | VSS | VSS | VSS | VDD | DQB1 |
| J | VDD | VSS | VDD | VSS | VDD | VSS | VDD |
| K | DQD1 | VDD | VSS | VSS | VSS | VDD | DQA1 |
| L | DQD2 | DQD7 | VDD | VSS | VDD | DQA7 | DQA2 |
| M | DQD3 | VDD | VSS | VSS | VSS | VDD | DQA3 |
| N | DQD4 | DQD8 | VDD | VSS | VDD | DQA8 | DQA4 |
| P | DQD5 | VDD | VSS | VSS | VSS | VDD | DQA5 |
| R | DQD6 | NC | NC | NC | NC | NC | DQA6 |
| T | $\overline{B_D}$ | A7 | A6 | $\overline{W_E}$ | A5 | A4 | $\overline{B_A}$ |
| U | NC | A3 | A2 | $\overline{O_E}$ | A1 | A0 | NC |

Note: Bumps 3C and 5C are actually NC's but should be wired 3C = VDD and 5C = VSS to assure compatibility with future versions.

Truth Table

| \overline{CE} | \overline{OE} | \overline{WE} | $\overline{B_A}$ | $\overline{B_B}$ | $\overline{B_C}$ | $\overline{B_D}$ | DQA1-8 | DQB1-8 | DQC1-8 | DQD1-8 | Supply Current |
|-----------------|-----------------|-----------------|------------------|------------------|------------------|------------------|--------------|--------------|--------------|--------------|----------------|
| H | X | X | X | X | X | X | Not Selected | Not Selected | Not Selected | Not Selected | ISB1, ISB2 |
| L | L | H | L | L | L | L | Read | Read | Read | Read | IDD |
| | | | H | L | L | L | High Z | Read | Read | Read | |
| | | | L | H | L | L | Read | High Z | Read | Read | |
| | | | L | L | H | L | Read | Read | High Z | Read | |
| | | | L | L | L | H | Read | Read | Read | High Z | |
| L | X | L | L | L | L | L | Write | Write | Write | Write | |
| | | | H | L | L | L | High Z | Write | Write | Write | |
| | | | L | H | L | L | Write | High Z | Write | Write | |
| | | | L | L | H | L | Write | Write | High Z | Write | |
| | | | L | L | L | H | Write | Write | Write | High | |
| L | H | H | X | X | X | X | High Z | High Z | High Z | High Z | |
| L | X | X | H | H | H | H | High Z | High Z | High Z | High Z | |

Note: X: "H" or "L"

Absolute Maximum Ratings

| Parameter | Symbol | Rating | Unit |
|-----------------------------|-----------|---|------|
| Supply Voltage | V_{DD} | -0.5 to +4.6 | V |
| Input Voltage | V_{IN} | -0.5 to $V_{DD}+0.5$ ($\leq 4.6V$ max.) | V |
| Output Voltage | V_{OUT} | -0.5 to $V_{DD}+0.5$ ($\leq 4.6V$ max.) | V |
| Allowable power dissipation | PD | 1.5 | W |
| Storage temperature | T_{STG} | -55 to 150 | °C |

Note:

Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation shall be restricted to Recommended Operating Conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|-----------------|------|-----|----------------------|------|
| Supply Voltage for -10/12/15 | V _{DD} | 3.0 | 3.3 | 3.6 | V |
| Input High Voltage | V _{IH} | 2.0 | - | V _{DD} +0.3 | V |
| Input Low Voltage | V _{IL} | -0.3 | - | 0.8 | V |
| Ambient Temperature, Commercial Range | T _{Ac} | 0 | - | 70 | °C |
| Ambient Temperature, Industrial Range | T _{Ai} | -40 | - | 85 | °C |

Note:

1. Input overshoot voltage should be less than V_{DD}+2V and not exceed 20ns.
2. Input undershoot voltage should be greater than -2V and not exceed 20ns.

Capacitance

| Parameter | Symbol | Test Condition | Max | Unit |
|--------------------|------------------|----------------------|-----|------|
| Input Capacitance | C _{IN} | V _{IN} =0V | 10 | pF |
| Output Capacitance | C _{OUT} | V _{OUT} =0V | 7 | pF |

Notes:

1. Tested at T_A=25°C, f=1MHz
2. These parameters are sampled and are not 100% tested

DC I/O Pin Characteristics

| Parameter | Symbol | Test Conditions | Min | Max |
|------------------------|-----------------|---|------|------|
| Input Leakage Current | I _{IL} | V _{IN} = 0 to V _{DD} | -2uA | 2uA |
| Output Leakage Current | I _{OL} | Output High Z, V _{OUT} = 0 to V _{DD} | -1uA | 1uA |
| Output High Voltage | V _{OH} | I _{OH} = - 4mA | 2.4 | |
| Output Low Voltage | V _{OL} | I _{OL} = + 4mA | | 0.4V |

Power Supply Currents

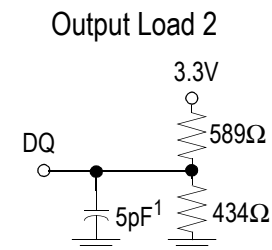
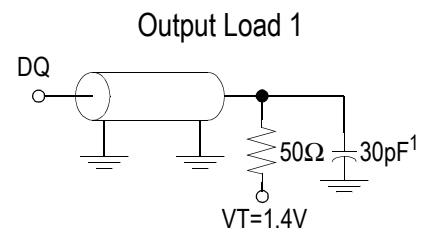
| Parameter | Symbol | Test Conditions | 0 to 70°C | | | -40 to 85°C | | |
|--------------------------|-----------|---|-----------|-------|-------|-------------|-------|-------|
| | | | 10ns | 12ns | 15ns | 10ns | 12ns | 15ns |
| Operating Supply Current | I_{DD} | $\bar{E} \leq V_{IL}$ All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Min. cycle time $I_{OUT} = 0$ mA | 290mA | 260mA | 220mA | 310mA | 280mA | 240mA |
| Standby Current | I_{SB1} | $\bar{E} \geq V_{IH}$ All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Min. cycle time | 130mA | 120mA | 110mA | 150mA | 140mA | 130mA |
| Standby Current | I_{SB2} | $E \geq V_{DD} - 0.2V$ All other inputs $\geq V_{DD} - 0.2V$ or $\leq 0.2V$ | 60mA | | | 80mA | | |

AC Test Conditions

| Parameter | Conditions |
|------------------------|---------------|
| Input high level | $V_{IH}=2.4V$ |
| Input low level | $V_{IL}=0.4V$ |
| Input rise time | $t_r=1V/ns$ |
| Input fall time | $t_f=1V/ns$ |
| Input reference level | 1.4V |
| Output reference level | 1.4V |
| Output load | Fig. 1 & 2 |

Note:

1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in Fig. 1 unless otherwise noted
3. Output load 2 for t_{LZ} , t_{HZ} , t_{OLZ} and t_{OHZ} .

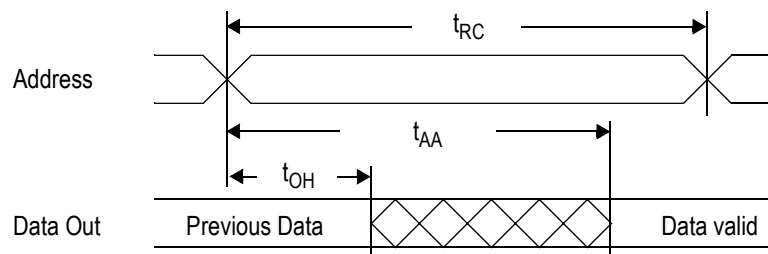


AC Characteristics

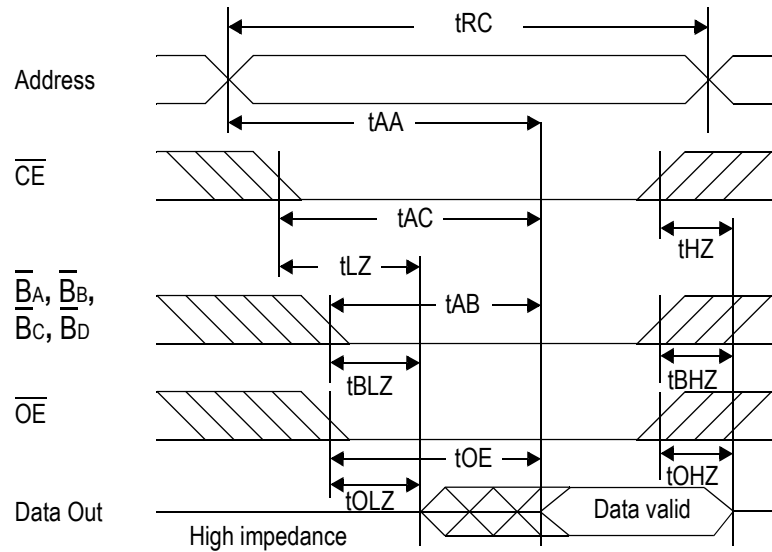
Read Cycle

| Parameter | Symbol | -10 | | -12 | | -15 | | Unit |
|--|-------------|-----|-----|-----|-----|-----|-----|------|
| | | Min | Max | Min | Max | Min | Max | |
| Read cycle time | t_{RC} | 10 | --- | 12 | --- | 15 | --- | ns |
| Address access time | t_{AA} | --- | 10 | --- | 12 | --- | 15 | ns |
| Chip enable access time (\overline{CE}) | t_{AC} | --- | 10 | --- | 12 | --- | 15 | ns |
| Byte enable access time | t_{AB} | --- | 4 | --- | 5 | --- | 6 | ns |
| Output enable to output valid (\overline{OE}) | t_{OE} | --- | 4 | --- | 5 | --- | 6 | ns |
| Output hold from address change | t_{OH} | 3 | --- | 3 | --- | 3 | --- | ns |
| Chip enable to output in low Z (\overline{CE}) | t_{LZ}^* | 3 | --- | 3 | --- | 3 | --- | ns |
| Output enable to output in low Z (\overline{OE}) | t_{OLZ}^* | 0 | --- | 0 | --- | 0 | --- | ns |
| Byte enable to output in low Z | t_{BLZ}^* | 0 | --- | 0 | --- | 0 | --- | ns |
| Chip disable to output in High Z (\overline{CE}) | t_{HZ}^* | --- | 5 | --- | 6 | --- | 7 | ns |
| Output disable to output in High Z (\overline{OE}) | t_{OHZ}^* | --- | 4 | --- | 5 | --- | 6 | ns |
| Byte disable to output in High Z | t_{BHZ}^* | --- | 4 | --- | 5 | --- | 6 | ns |

Read Cycle 1: $\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$, $\overline{BA} = \overline{BB} = \overline{BC} = \overline{BD} = V_{IL}$



Read Cycle 2: $\overline{WE} = V_{IH}$

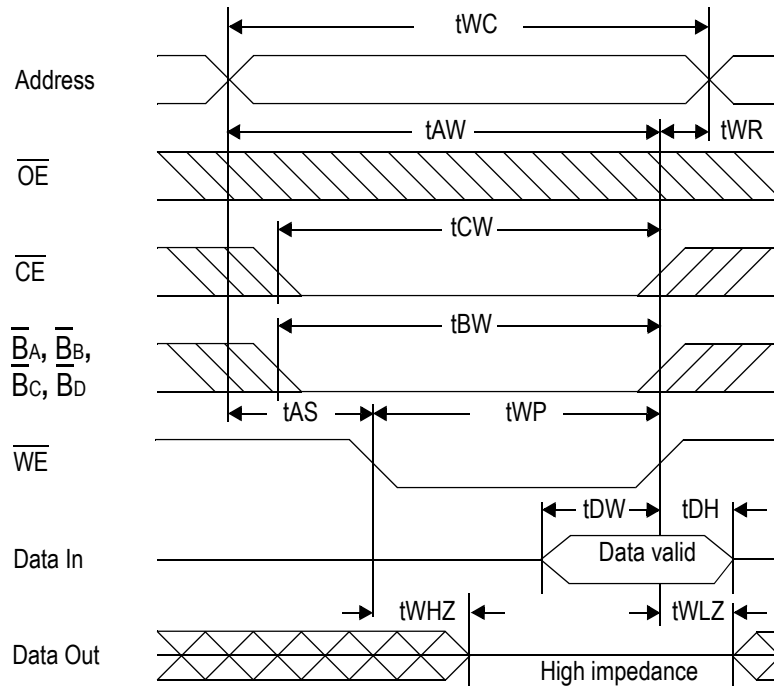


Write Cycle

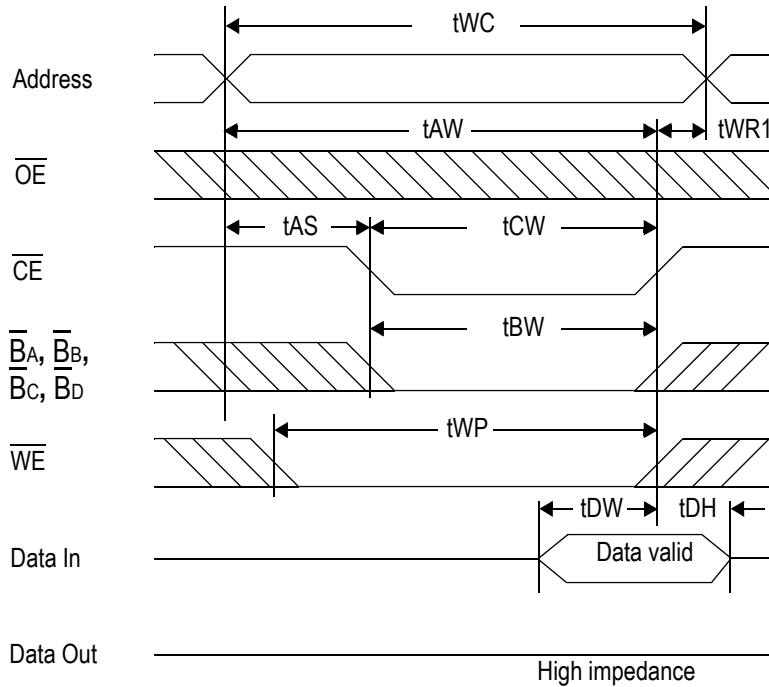
| Parameter | Symbol | -10 | | -12 | | -15 | | Unit |
|---|-------------|-----|-----|-----|-----|-----|-----|------|
| | | Min | Max | Min | Max | Min | Max | |
| Write cycle time | t_{WC} | 10 | --- | 12 | --- | 15 | --- | ns |
| Address valid to end of write | t_{AW} | 7 | --- | 8 | --- | 10 | --- | ns |
| Chip enable to end of write | t_{CW} | 7 | --- | 8 | --- | 10 | --- | ns |
| Byte enable to end of write | t_{BW} | 7 | --- | 8 | --- | 10 | --- | ns |
| Data set up time | t_{DW} | 5 | --- | 6 | --- | 7 | --- | ns |
| Data hold time | t_{DH} | 0 | --- | 0 | --- | 0 | --- | ns |
| Write pulse width | t_{WP} | 7 | --- | 8 | --- | 10 | --- | ns |
| Address set up time | t_{AS} | 0 | --- | 0 | --- | 0 | --- | ns |
| Write recovery time (\overline{WE}) | t_{WR} | 0 | --- | 0 | --- | 0 | --- | ns |
| Write recovery time (\overline{CE}) | t_{WR1} | 0 | --- | 0 | --- | 0 | --- | ns |
| Output Low Z from end of write | t_{WLZ}^* | 3 | --- | 3 | --- | 3 | --- | ns |
| Write to output in High Z | t_{WHZ}^* | --- | 4 | --- | 5 | --- | 6 | ns |

* These parameters are sampled and are not 100% tested

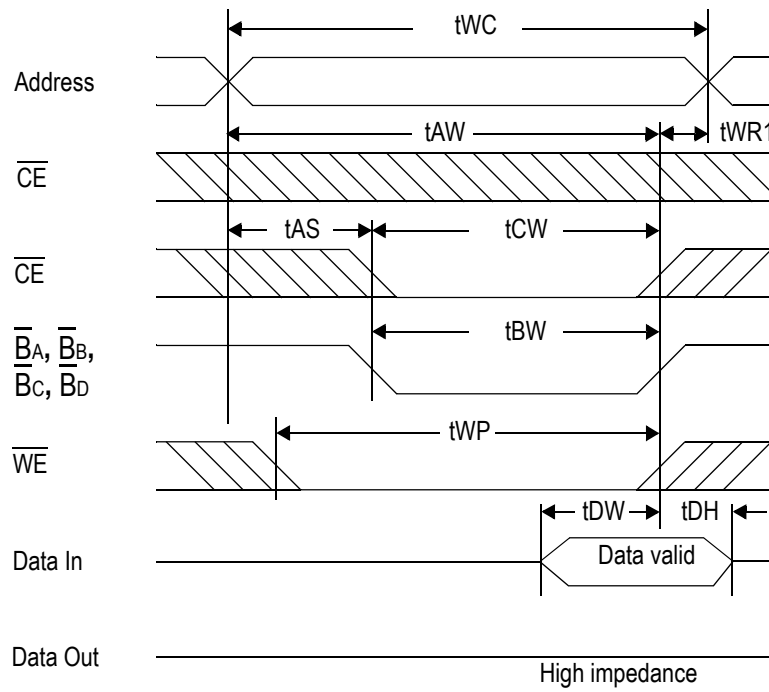
Write Cycle 1: $\overline{\text{WE}}$ Controlled



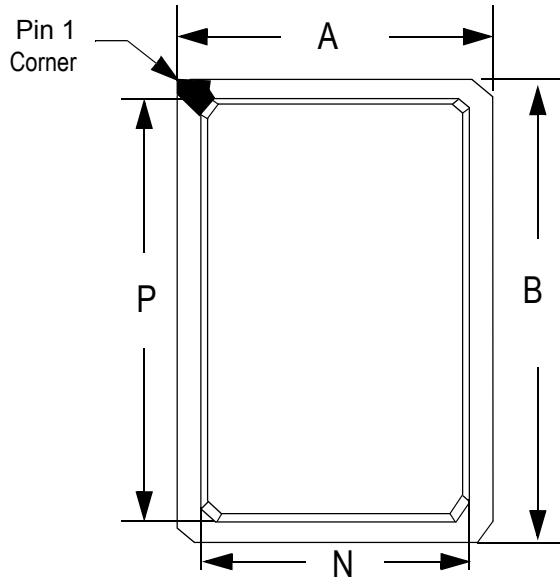
Write Cycle 2: $\overline{\text{CE}}$ Controlled



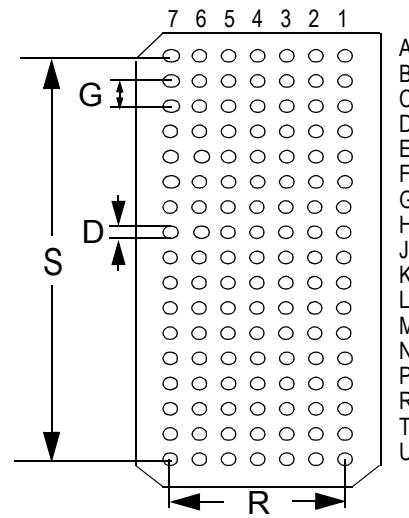
Write Cycle 3: Byte Enable Controlled



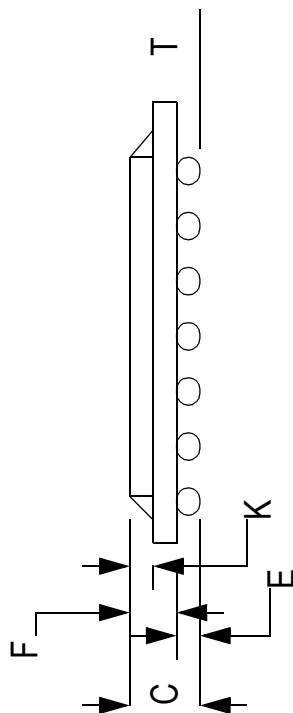
Package Dimensions - 119 Pin PBGA



Top View



Bottom View



Side View

Package Dimensions - 119 Pin PBGA

| Symbol | Description | Min. | Nom. | Max |
|--------|----------------------------------|------|-------|------|
| A | Width | 13.8 | 14.0 | 14.2 |
| B | Length | 21.8 | 22.0 | 22.2 |
| C | Package Height (including ball) | - | | 2.40 |
| D | Ball Size | 0.60 | 0.75 | 0.90 |
| E | Ball Height | 0.50 | 0.60 | 0.70 |
| F | Package Height (excluding balls) | | 1.46 | 1.70 |
| G | Width between Balls | | 1.27 | |
| K | Package Height above board | 0.80 | 0.90 | 1.00 |
| N | Cut-out Package Width | | 12.00 | |
| P | Foot Length | | 19.50 | |
| R | Width of package between balls | | 7.62 | |
| S | Length of package between balls | | 20.32 | |
| T | Variance of Ball Height | | 0.15 | |

Unit: mm

Ordering Information

| Part Number * | Package | Access Time | Temp. Range | Status |
|---------------|---------|-------------|-------------|--------|
| GS78132B-10 | BGA | 10 ns | Commercial | |
| GS78132B-12 | BGA | 12 ns | Commercial | |
| GS78132B-15 | BGA | 15 ns | Commercial | |
| GS78132B-10I | BGA | 10 ns | Industrial | |
| GS78132B-12I | BGA | 12 ns | Industrial | |
| GS78132B-15I | BGA | 15 ns | Industrial | |

* Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. For example: GS78132B-12T

Revision History

| Rev. Code: Old; New | Types of Changes Format or Content | Page #/Revisions/Reason |
|---|---------------------------------------|---|
| GS78132Rev0.01a 5/1999; 1.00 X/1999 | Format/Typos | <ul style="list-style-type: none"> • p.2/Changed 12x22 to 14x22/Typo • p.2/Changed \bar{E} to \bar{CE}/consistency. |
| | Content | <ul style="list-style-type: none"> • p.2/Changed Pin T1 from $\bar{B}A$ to $\bar{B}b$/Correction |
| GS78132Rev 1.0010/1999A;Rev 1.01 2/2000FormatB | | <ul style="list-style-type: none"> • Added GSI Logo |