Non-Volatile SRAM MODULE 32Mbit (4,096K x 8-Bit), 40Pin-DIP, 3.3V

Part No. HMN4M8DV(N)

GENERAL DESCRIPTION

The HMN4M8DV Nonvolatile SRAM is a 33,554,432-bit static RAM organized as 4,194,304 bytes by 8 bits.

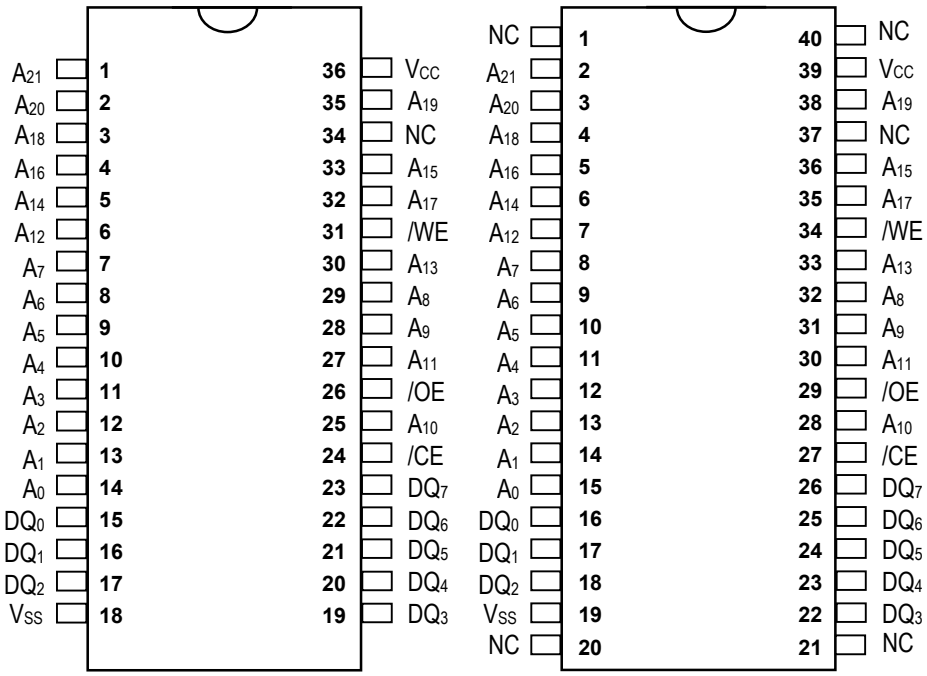
The HMN4M8DV has a self-contained lithium energy source provide reliable non-volatility coupled with the unlimited write cycles of standard SRAM and integral control circuitry which constantly monitors the single 3.3V supply for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on to sustain the memory until after V_{CC} returns valid and write protection is unconditionally enabled to prevent garbled data. In addition the SRAM is unconditionally write-protected to prevent an inadvertent write operation. At this time the integral energy source is switched on to sustain the memory until after V_{CC} returns valid.

The HMN4M8DV uses extremely low standby current CMOS SRAM's, coupled with small lithium coin cells to provide non-volatility without long write-cycle times and the write-cycle limitations associated with EEPROM.

FEATURES

- Access time : 55, 70ns
- High-density design : 32Mbit Design
- Battery internally isolated until power is applied
- Industry-standard 40-pin 4,096K x 8 pinout
- Unlimited write cycles
- Data retention in the absence of V_{CC}
- 5-years minimum data retention in absence of power
- Automatic write-protection during power-up/power-down cycles
- Data is automatically protected during power loss

PIN ASSIGNMENT



36-pin Encapsulated Package **40-pin Encapsulated Package**

- Package Option
  - HMN4M8DV - 36 Pin DIP Package
  - HMN4M8DVN - 40 Pin DIP Package

FUNCTIONAL DESCRIPTION

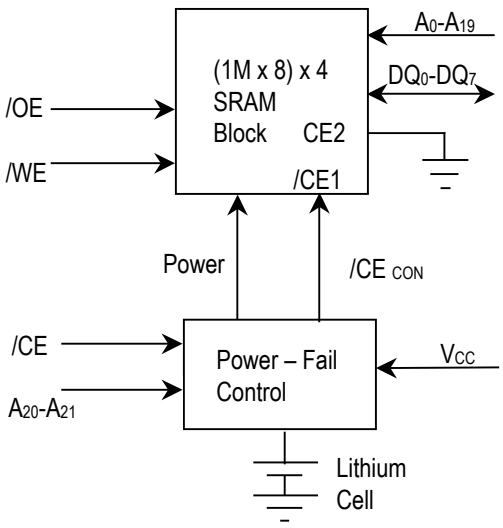
The HMN4M8DV executes a read cycle whenever /WE is inactive(high) and /CE is active(low). The address specified by the address inputs(A_0-A19) defines which of the 4,194,304 bytes of data is accessed. Valid data will be available to the eight data output drivers within t_{ACC} (access time) after the last address input signal is stable.

When power is valid, the HMN4M8DV operates as a standard CMOS SRAM. During power-down and power-up cycles, the HMN4M8DV acts as a nonvolatile memory, automatically protecting and preserving the memory contents.

The HMN4M8DV is in the write mode whenever the /WE and /CE signals are in the active (low) state after address inputs are stable. The later occurring falling edge of /CE or /WE will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of /CE or /WE. All address inputs must be kept valid throughout the write cycle. WE must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The /OE control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus been enabled (/CE and /OE active) then /WE will disable the outputs in t_{ODW} from its falling edge.

The HMN4M8DV provides full functional capability for Vcc greater than 4.5 V and write protects by 4.37 V nominal. Power-down/power-up control circuitry constantly monitors the Vcc supply for a power-fail-detect threshold V_{PFD}. When V_{CC} falls below the V_{PFD} threshold, the SRAM automatically write-protects the data. All inputs to the RAM become "don't care" and all outputs are high impedance. As Vcc falls below approximately 3 V, the power switching circuit connects the lithium energy soure to RAM to retain data. During power-up, when Vcc rises above approximately 3.0 volts, the power switching circuit connects external Vcc to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after Vcc exceeds 4.5 volts.

BLOCK DIAGRAM



PIN DESCRIPTION

A_0-A_{21} : Address Input
/CE : Chip Enable
V_{SS} : Ground
DQ_0-DQ_7 : Data In / Data Out
/WE : Write Enable
/OE : Output Enable
V_{CC}: Power (+5V)
NC : No Connection

TRUTH TABLE

MODE	/OE	/CE	CE2	/WE	I/O OPERATION	POWER
Not selected	X	H	X	X	High Z	Standby
Output disable	H	L	H	H	High Z	Active
Read	L	L	H	H	D_{OUT}	Active
Write	X	L	H	L	D_{IN}	Active

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	CONDITIONS
DC voltage applied on V_{CC} relative to V_{SS}	V_{CC}	-0.5V to V_{CC} +0.2V	
DC Voltage applied on any pin excluding V_{CC} relative to V_{SS}	V_T	-0.2V to 4.6V	
Operating temperature	T_{OPR}	0 to 70°C	Commercial
		-40 to 85°C	Industrial
Storage temperature	T_{STG}	-65°C to 150°C	
Temperature under bias	T_{BIAS}	-40°C to 85°C	
Soldering temperature	T_{SOLDER}	260°C	For 10 second

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded.
Functional operation should be restricted to the Recommended DC Operating Conditions detailed in this data sheet.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS ($T_A = T_{OPR}$)

PARAMETER	SYMBOL	MIN	TYPICAL	MAX
Supply Voltage	V_{CC}	3.0V	3.3V	3.6V
Ground	V_{SS}	0	0	0
Input high voltage	V_{IH}	2.2	-	V_{CC}+0.3V [1]
Input low voltage	V_{IL}	-0.2 [2]	-	0.6V

NOTE: 1. Overshoot: VCC+2.0V in case of pulse width ≤20ns.
2. Undershoot: -2.0V in case of pulse width ≤20ns.
3. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE (T_A=25℃, f=1MHz)

DESCRIPTION	CONDITIONS	SYMBOL	MAX	MIN	UNIT
Input Capacitance	Input voltage = 0V	C_{IN}	8	-	pF
Input/Output Capacitance	Output voltage = 0V	$C_{I/O}$	10	-	pF

NOTE: 1. Capacitance is sampled, not 100% tested.

DC AND OPERATION CHARACTERISTICS (T_A= T_{OPR}, V_{CCmin} ≤ V_{CC} ≤ V_{CCmax})

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Input Leakage Current	V_{IN}=V_{SS} to V_{CC}	I_{LI}	-4	-	+4	μA
Output Leakage Current	/CE=V_{IH} or /OE=V_{IH} or /WE=V_{IL}	I_{LO}	-4	-	+4	μA
Output high voltage	I_{OH}=-1.0 mA	V_{OH}	2.4	-	-	V
Output low voltage	I_{OL}= 2.1 mA	V_{OL}	-	-	0.4	V
Standby supply current	/CE≥V_{CC}-0.2V	I_{SB1}	-	-	80	μA
Average operating current	Cycle time=Min, 100% duty, $I_{I/O}$=0㎃, /CE<V_{cc}-0.2V, V_{IN}<0.2V or V_{IN}>V_{CC}-0.2V	I_{CC1}	-	-	12	㎃
	Cycle time=1us, 100% duty, $I_{I/O}$=0㎃, /CE=V_{IL}, V_{IN}=V_{IL} or V_{IH}	I_{CC2}	-	-	50	㎃
Power-fail-detect voltage		V_{PFD}	2.5	2.6	2.7	V
Supply switch-over voltage		V_{SO}	-	3	-	V

CHARACTERISTICS (Test Conditions)

PARAMETER	VALUE
Input pulse levels	0 to 3V
Input rise and fall times	< 5 ns
Input and output timing reference levels	1.5V (unless otherwise specified)
Output load (including scope and jig)	See Figure 1 and 2

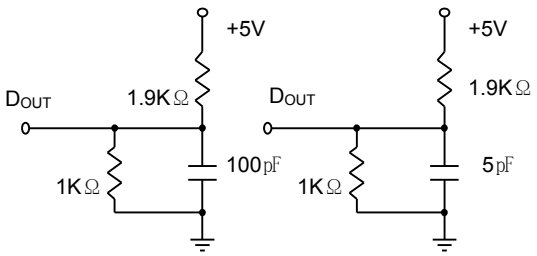


Figure 1. Output Load A

Figure 2. Output Load B

READ CYCLE (T_A= T_{OPR}, V_{CCmin} ≤ V_{CC}≤ V_{CCmax})

PARAMETER	SYMBOL	CONDITIONS	-70		-85		-120		-150		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Read Cycle Time	t_{RC}		70	-	85	-	120	-	150	-	ns
Address Access Time	t_{ACC}	Output load A	-	70	-	85	-	120	-	150	ns
Chip enable access time	t_{ACE}	Output load A	-	70	-	85	-	120	-	150	ns
Output enable to Output valid	t_{OE}	Output load A	-	35	-	45	-	60	-	70	ns
Chip enable to output in low Z	t_{CLZ}	Output load B	5	-	5	-	5	-	10	-	ns
Output enable to output in low Z	t_{OLZ}	Output load B	5	-	0	-	0	-	5	-	ns
Chip disable to output in high Z	t_{CHZ}	Output load B	0	25	0	35	0	45	0	60	ns
Output disable to output high Z	t_{OHZ}	Output load B	0	25	0	25	0	35	0	50	ns
Output hold from address change	t_{OH}	Output load A	10	-	10	-	10	-	10	-	ns

WRITE CYCLE (T_A= T_{OPR}, V_{ccmin} ≤ V_{cc} ≤ V_{ccmax})

PARAMETER	SYMBOL	CONDITIONS	-70		-85		-120		-150		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	Min	Max	
Write Cycle Time	t_{WC}		70	-	85	-	120	-	150	-	ns
Chip enable to end of write	t_{CW}	Note 1	65	-	75	-	100	-	100	-	ns
Address setup time	t_{AS}	Note 2	0	-	0	-	0	-	0	-	ns
Address valid to end of write	t_{AW}	Note 1	65	-	75	-	100	-	90	-	ns
Write pulse width	t_{WP}	Note 1	55	-	65	-	85	-	90	-	ns
Write recovery time (write cycle 1)	t_{WR1}	Note 3	5	-	5	-	5	-	5	-	ns
Write recovery time (write cycle 2)	t_{WR2}	Note 3	15	-	15	-	15	-	15	-	ns
Data valid to end of write	t_{DW}		30	-	35	-	45	-	50	-	ns
Data hold time (write cycle 1)	t_{DH1}	Note 4	0	-	0	-	0	-	0	-	ns
Data hold time (write cycle 2)	t_{DH2}	Note 4	10	-	10	-	10	-	0	-	ns
Write enabled to output in high Z	t_{WZ}	Note 5	0	25	0	30	0	40	0	50	ns
Output active from end of write	t_{OW}	Note 5	5	-	0	-	0	-	5	-	ns

NOTE: 1. A write ends at the earlier transition of /CE going high and /WE going high.

2. A write occurs during the overlap of allow /CE and a low /WE. A write begins at t he later transition of /CE going low and /WE going low.

3. Either t_{WR1} or t_{WR2} must be met.

4. Either t_{DH1} or t_{DH2} must be met.

5. If /CE goes low simultaneously with /WE going low or after /WE going low, the outpu ts remain in high-impedance state.

DATA RETENTION CHARACTERISTICS (T_A= T_{OPR}, V_{CC}=5V)

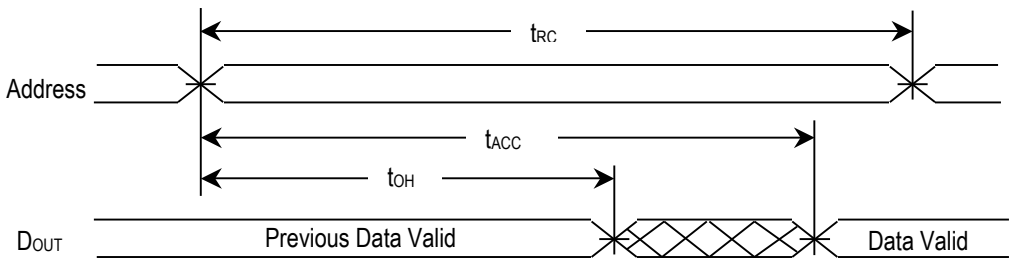
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP.	MAX	UNIT
Vcc for data retention	V_{DR}	CE≥Vcc-0.2V	1.5	-	3.6	V
Data retention current	I_{DR}	Vcc=3.0V, CE≥Vcc		2	24	uA
Data retention set-up time	t_{SDR}	See data retention waveform	0	-	-	ms
Recovery time	t_{RDR}		t_{RC}	-	-	

POWER-DOWN/POWER-UP CYCLE (T_A= T_{OPR}, V_{CC}=3.3V)

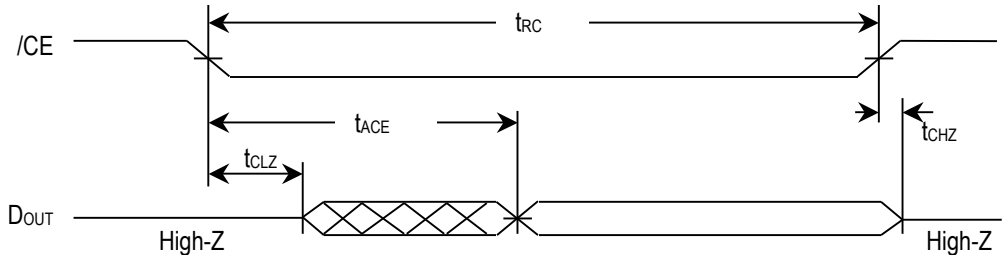
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{PFD}(max) to V_{PFD}(min) V_{CC} Fail Time	t_F		300	-	-	μs
V_{PFD}(max) to V_{SS} V_{CC} Fail Time	t_{FB}		150	-	-	μs
V_{PFD}(max) to V_{PFD}(min) V_{CC} Rise Time	t_R		10	-	-	μs
Write Protect Time	t_{WPT}	Delay after Vcc slews down past V_{PFD} before SRAM is Write-protected.	40		250	μs
Chip Enable Recovery	t_{CER}		40	-	120	ms
V_{SS} to V_{PFD} (min) V_{CC} Rise Time	t_{RB}		1	-	-	μs

TIMING WAVEFORM

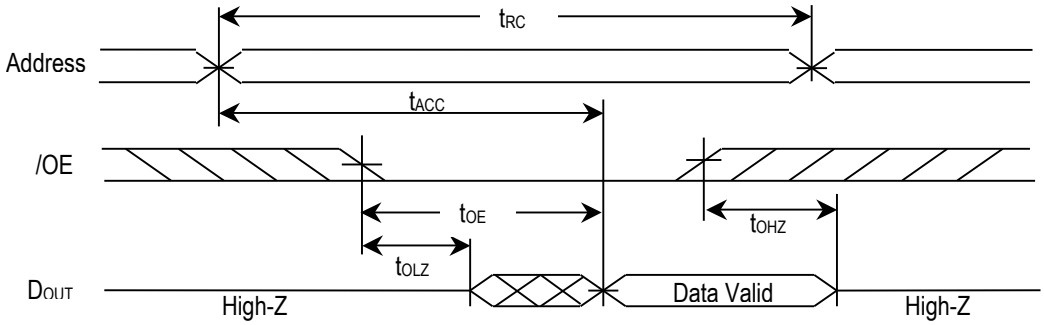
- READ CYCLE NO.1 (Address Access)*[1,2]



- READ CYCLE NO.2 (/CE Access)[*1,3,4]



- READ CYCLE NO.3 (/OE Access)[*1,5]



NOTES: 1. /WE is held high for a read cycle.

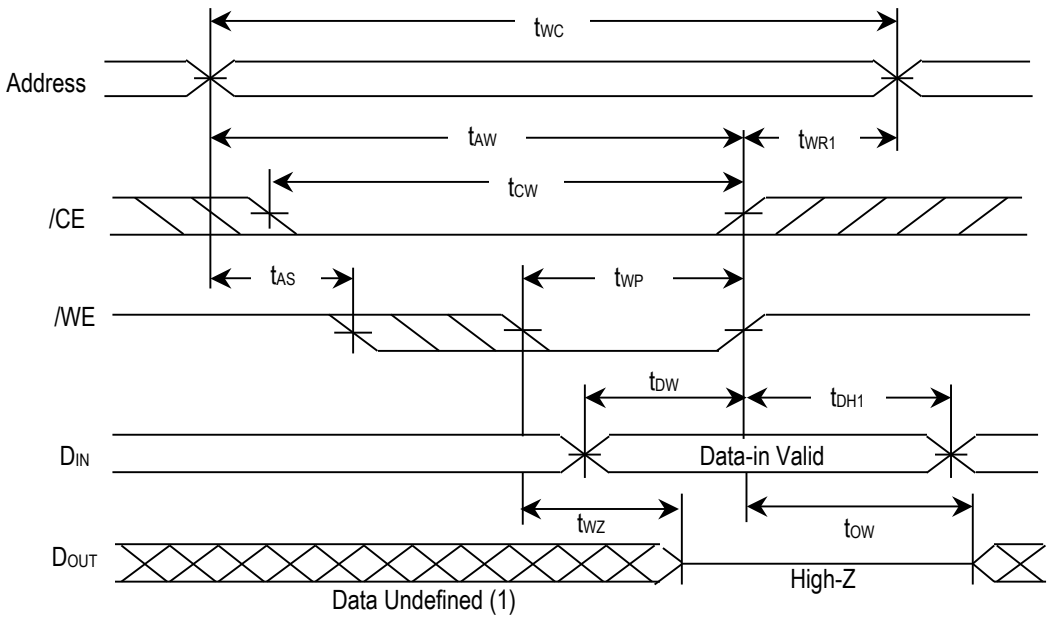
2. Device is continuously selected: /CE = /OE =V_{IL}.

3. Address is valid prior to or coincident with /CE transition low.

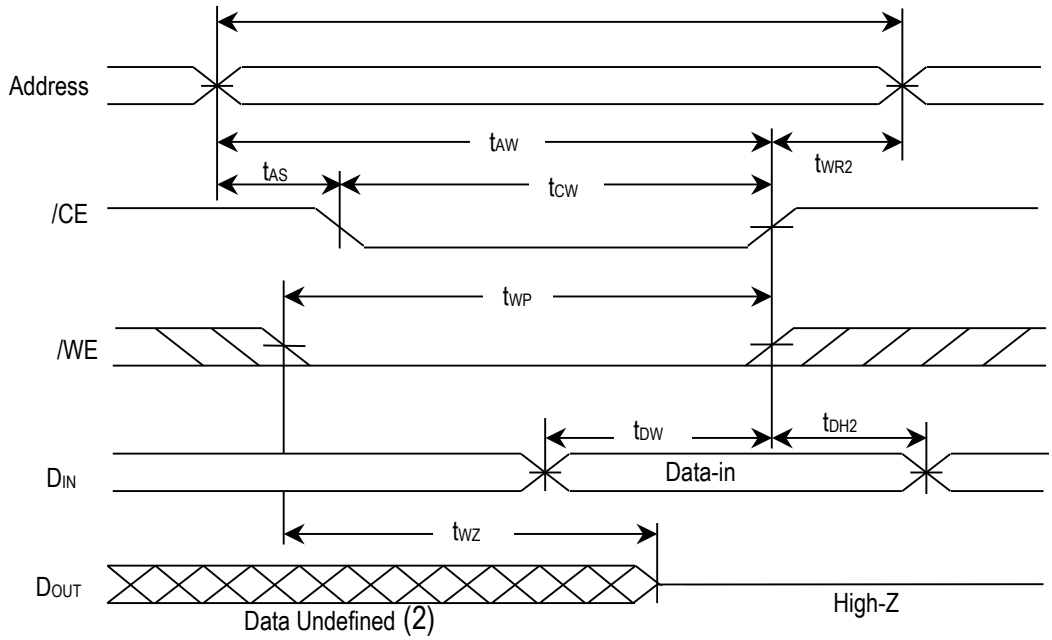
4. /OE = V_{IL}.

5. Device is continuously selected: /CE = V_{IL}

- WRITE CYCLE NO.1 (/WE-Controlled)[*1,2,3]



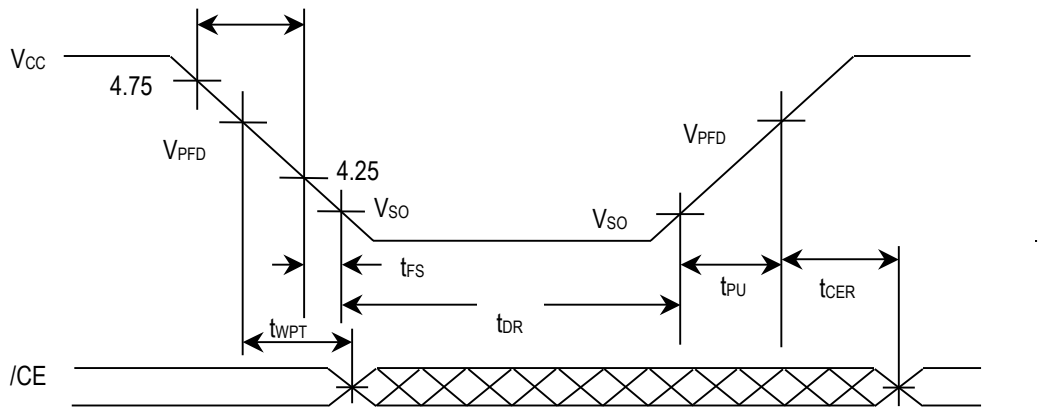
- WRITE CYCLE NO.2 (/CE-Controlled)*1,2,3,4,5



NOTE: 1. /CE or /WE must be high during address transition.

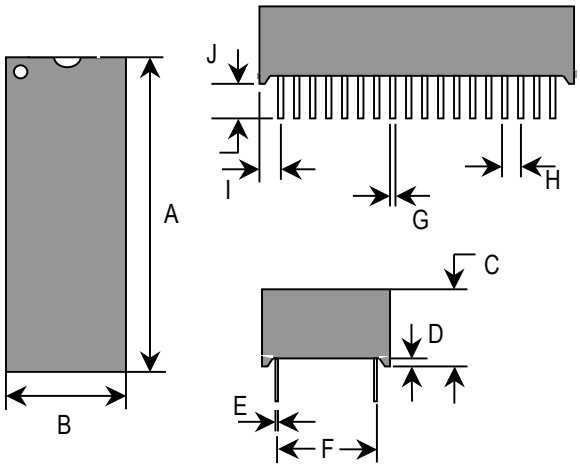
2. Because I/O may be active (/OE low) during this period, data input signals of opp osite polarity to the outputs must not be applied.
3. If /$\overline{OE}$ is high, the I/O pins remain in a state of high impedance.
4. Either t_{WR1} or t_{WR2} must be met.
5. Either t_{DH1} or t_{DH2} must be met.

POWER-DOWN/POWER-UP TIMING



PACKAGE DIMENSION

Dimension	Min	Max
A	2.070	2.100
B	0.710	0.740
C	0.365	0.375
D	0.015	-
E	0.008	0.013
F	0.590	0.630
G	0.017	0.023
H	0.090	0.110
I	0.080	0.110
J	0.120	0.150



All dimensions are in inches.

ORDERING INFORMATION

H M N 4 M 8 D V N – 70 I

- **Temperature Option :** Blank : Commercial(0 to 70°C)
  I : Industrial : -40 to 85°C
- **Speed Option :** 70 = 70ns
  85 = 85ns
  120 = 120ns
  150 = 150ns
- **Package Option :** **Blank** : 36 Pin Dip Package
  N : 40 Pin Dip Package
- **Operation Voltage : 3.3V**
- **Dip type package**
- **Device :** 4,096K x 8 bit
- **Nonvolatile SRAM**
- **HANBit Memory Module**