



2x128Kx72, 3.3V Sync/Sync Burst SRAM SO-DIMM

FEATURES

- 2x128Kx72 Synchronous, Synchronous Burst
- Flow-Through Architecture
- Linear and Sequential Burst Support via MODE pin
- Access Speed(s): T_{KHQV} = 8.5, 9, 12, 15ns
- Clock Controlled Registered Bank Enables (E1#, E2#)
- Clock Controlled Registered Address
- Clock Controlled Registered Global Write (GW#)
- Asynchronous Output Enable (G#)
- Internally Self-timed Write
- Individual Bank Sleep Mode enables (ZZ1, ZZ2)
- Gold Lead Finish
- 3.3V \pm 10% Operation
- Common Data I/O
- High Capacitance (30pf) drive, at rated Access Speed
- Single Total Array Clock
- Multiple Vcc and Gnd

DESCRIPTION

The EDI2CG272128VxxD1 is a Synchronous/Synchronous Burst SRAM, 72 position DIMM (144 contacts) Module, small outline. The Module contains four (4) Synchronous Burst Ram Devices, packaged in the industry standard JEDEC 14mmx20mm TQFP placed on a Multilayer FR4 Substrate. The module architecture is defined as a Sync/Sync Burst, Flow-Through, with support for linear burst. This module provides High Performance, 2-1-1-1 accesses when used in Burst Mode, and used as a Synchronous Only Mode, provides a high performance cost advantage over BiCMOS asynchronous device architectures.

Synchronous Only operations are performed via strapping ADSC# Low, and ADSP# / ADV# High, which provides for Ultra Fast Accesses in Read Mode while providing for internally self-timed Early Writes.

Synchronous/Synchronous Burst operations are in relation to an externally supplied clock, Registered Address, Registered Global Write, Registered Enables as well as an Asynchronous Output enable. This Module has been defined for Quad Words in both Read and Write Operations.

*This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.



PIN CONFIGURATION

PIN SYMBOLS

PIN	FUNCTION	PIN	FUNCTION
1	V _{SS}	37	DQ0
2	V _{SS}	38	DQ7
3	A0	39	DQ1
4	RFU	40	DQ6
5	A16	41	DQ2
6	A1	42	DQ5
7	A2	43	DQ3
8	A15	44	DQ4
9	A14	45	V _{SS}
10	A3	46	V _{SS}
11	A4	47	ZZ ₁
12	A13	48	DQP ₁
13	A12	49	V _{CC}
14	A5	50	V _{CC}
15	A6	51	DQ8
16	A11	52	DQ15
17	A10	53	DQ9
18	A7	54	DQ14
19	A8	55	DQ10
20	A9	56	DQ13
21	V _{CC}	57	DQ11
22	V _{CC}	58	DQ12
23	G#	59	V _{SS}
24	RFU	60	V _{SS}
25	GW#	61	E ₂
26	ADV#	62	DQP ₂
27	ADSP#	63	V _{CC}
28	ADSC#	64	V _{CC}
29	MODE	65	DQ16
30	CK	66	DQ23
31	V _{SS}	67	DQ17
32	V _{SS}	68	DQ22
33	E1#	69	DQ18
34	DQP0	70	DQ21
35	V _{CC}	71	DQ19
36	V _{CC}	72	DQ20

PIN	FUNCTION	PIN	FUNCTION
73	V _{SS}	109	DQ41
74	V _{SS}	110	DQ46
75	ZZ ₂	111	DQ42
76	DQP ₃	112	DQ45
77	V _{CC}	113	DQ43
78	V _{CC}	114	DQ44
79	DQ24	115	V _{SS}
80	DQ31	116	V _{SS}
81	DQ25	117	RFU
82	DQ30	118	DQP ₆
83	DQ26	119	V _{CC}
84	DQ29	120	V _{CC}
85	DQ27	121	DQ48
86	DQ28	122	DQ55
87	V _{SS}	123	DQ49
88	V _{SS}	124	DQ54
89	RFU	125	DQ50
90	DQP ₄	126	DQ53
91	V _{CC}	127	DQ51
92	V _{CC}	128	DQ52
93	DQ32	129	V _{SS}
94	DQ39	130	V _{SS}
95	DQ33	131	RFU
96	DQ38	132	DQP ₇
97	DQ34	133	V _{CC}
98	DQ37	134	V _{CC}
99	DQ35	135	DQ56
100	DQ36	136	DQ63
101	V _{SS}	137	DQ57
102	V _{SS}	138	DQ62
103	RFU	139	DQ58
104	DQP ₅	140	DQ61
105	V _{CC}	141	DQ59
106	V _{CC}	142	DQ60
107	DQ40	143	V _{SS}
108	DQ47	144	V _{SS}

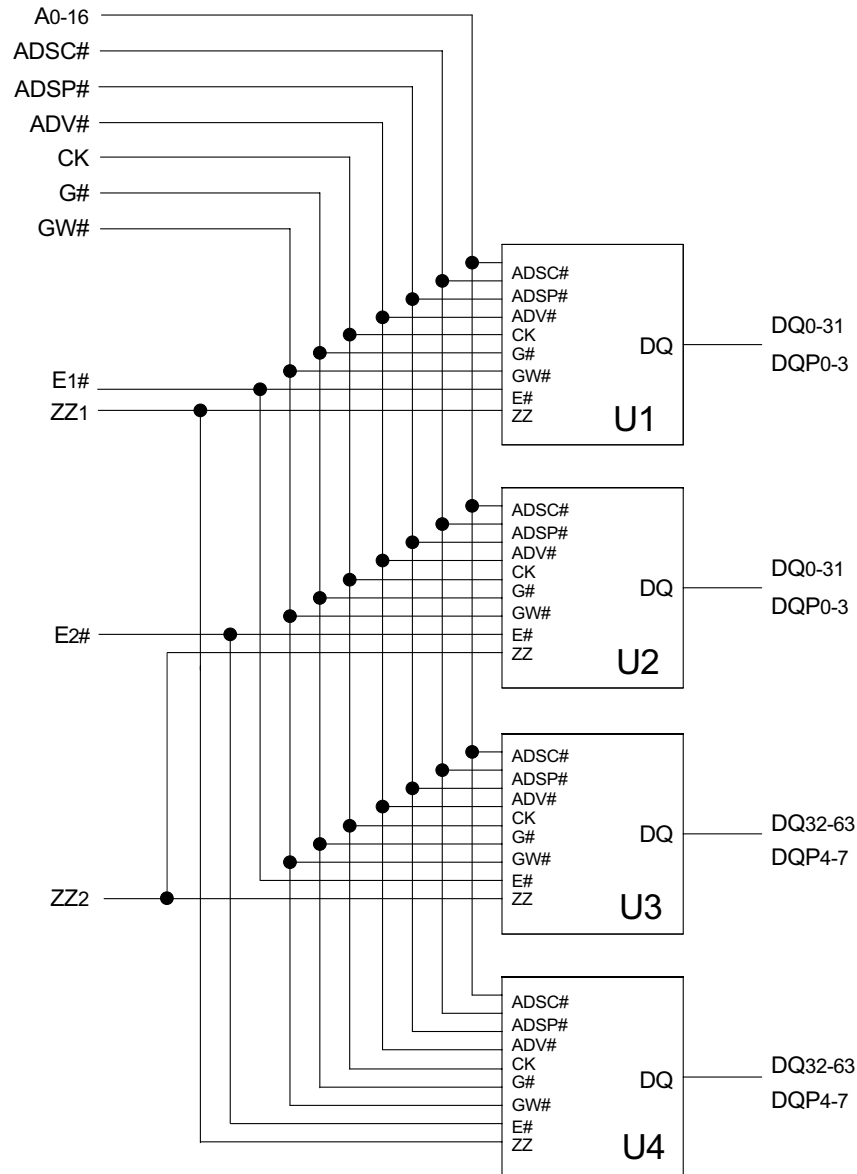
PIN NAMES

DQ0-DQ63	Input/Output Bus
DQP0-DQP7	Parity Bits
A0-A16	Address Bus
E1#, E2#	Synchronous Bank Enables
CK	Array Clock
GW#	Synchronous Global Write Enable
G#	Asynchronous Output Enable
ZZ ₁ , ZZ ₂	Blank Sleep Mode Enables
V _{CC}	3.3V Power Supply
V _{SS}	Ground
NC	No Connect



FIG. 1

FUNCTIONAL BLOCK DIAGRAM





PIN DESCRIPTIONS

DIMM Pins	Symbol	Type	Description
3, 6, 10, 11, 14, 15, 18, 19, 20, 17, 16, 13, 12, 9, 8, 3, 5	A0-16	Input Synchronous	Addresses: These inputs are registered and must meet the setup and hold times around the rising edge of CK. The burst counter generates internal addresses associated with A0 and A1, during burst and wait cycle.
25	GW#	Input Synchronous	Global Write: This active LOW input allows a full 72-bit WRITE to occur independent of the BWE# and BWx# lines and must meet the setup and hold times around the rising edge of CK.
30	CK	Input Synchronous	Clock: This signal registers the addresses, data, chip enables, write control and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
33, 61	E1#, E2#	Input Synchronous	Bank Enables: These active LOW inputs are used to enable each individual bank and to gate ADSP#.
23	G#	Input Synchronous	Output Enable: This active LOW asynchronous input enables the data output drivers.
26	ADV#	Input Synchronous	Address Status Processor: This active LOW input is used to control the internal burst counter. A HIGH on this pin generates wait cycle (no address advance)
27	ADSP#	Input Synchronous	Address Status Processor: This active LOW input, along with EL# and EH# being LOW, causes a new external address to be registered and a READ cycle is initiated using the new address.
28	ADSC#	Input Synchronous	Address Status Controller: This active LOW input causes device to be de-selected or selected along with new external address to be registered. A READ or WRITE cycle is initiated depending upon write control inputs.
29	MODE	Input Static	Mode: This input selects the burst sequence. A LOW on this pin selects LINEAR BURST. A NC or HIGH on this pin selects INTERLEAVED BURST.
47, 75	ZZ1, ZZ2	Input Asynchronous	Snooze: These active HIGH inputs put the individual banks in low power consumption standby mode. For normal operation, this input has to be either LOW or NC (no connect).
Various	DQ0-63	Input/Output	Data Inputs/Outputs: First byte is DQ0-7, second byte is DQ8-15, third byte is DQ16-23, fourth byte is DQ24-31, fifth byte is DQ32-39, sixth byte is DQ40-47, seventh byte is DQ48-55 and the eighth byte is DQ56-64.
34, 48, 62, 76, 90, 104, 118, 132	DQP0-7	Input/Output	Parity Inputs/Outputs: DQP0 is parity bit for DQ0-7. DQP1 is parity bit for DQ8-15. DQP2 is parity bit for DQ16-23. DQP3 is parity bit for DQ24-31. DQP4# is parity bit for DQ32-39. DQP5 is parity bit for DQ40-47. DQP6# is parity bit for DQ48-55. DQP7 is parity bit for DQ56-64 and DQP7. In order to use the device configured as a 128K x 64, the parity bits need to be tied to Vss through a 10K ohm resistor.
Various	Vcc	Supply	Core power supply: +3.3V -5%/+10%
Various	Vss	Ground	Ground



SYNCHRONOUS BURST - TRUTH TABLE

Operation	E1#	E2#	ADSP#	ADSC#	ADV#	GW#	G#	CK	DQ	Addr. Used
Deselected Cycle, Power Down; Bank 1	H	X	X	L	X	X	X	L-H	High-Z	None
Deselected Cycle, Power Down; Bank 2	X	H	X	L	X	X	X	L-H	High-Z	None
Read Cycle, Begin Burst; Bank 1	L	H	L	X	X	X	L	L-H	Q	External
Read Cycle, Begin Burst; Bank 1	L	H	L	X	X	X	H	L-H	High-Z	External
Read Cycle, Begin Burst; Bank 2	H	L	L	X	X	X	L	L-H	Q	External
Read Cycle, Begin Burst; Bank 2	H	L	L	X	X	X	H	L-H	High-Z	External
Write Cycle, Begin Burst; Bank 1	L	H	H	L	X	L	X	L-H	D	External
Write Cycle, Begin Burst; Bank 2	H	L	H	L	X	L	X	L-H	D	External
Read Cycle, Begin Burst; Bank 1	L	H	H	L	X	H	L	L-H	Q	External
Read Cycle, Begin Burst; Bank 1	L	H	H	L	X	H	H	L-H	High-Z	External
Read Cycle, Begin Burst; Bank 2	H	L	H	L	X	H	L	L-H	Q	External
Read Cycle, Begin Burst; Bank 2	H	L	H	L	X	H	H	L-H	High-Z	External
Read Cycle, Continue Burst; Bank 1	X	H	X	H	L	H	L	L-H	Q	Next
Read Cycle, Continue Burst; Bank 1	X	H	X	H	L	H	H	L-H	High-Z	Next
Read Cycle, Continue Burst; Bank 2	H	X	X	H	L	H	L	L-H	Q	Next
Read Cycle, Continue Burst; Bank 2	H	X	X	H	L	H	H	L-H	High-Z	Next
Read Cycle, Continue Burst; Bank 1	H	H	X	H	L	H	L	L-H	Q	Next
Read Cycle, Continue Burst; Bank 1	H	H	X	H	L	H	H	L-H	High-Z	Next
Read Cycle, Continue Burst; Bank 2	H	H	X	H	L	H	L	L-H	Q	Next
Read Cycle, Continue Burst; Bank 2	H	H	X	H	L	H	H	L-H	High-Z	Next
Write Cycle, Continue Burst; Bank 1	X	H	H	H	L	L	X	L-H	D	Next
Write Cycle, Continue Burst; Bank 1	H	H	X	H	L	L	X	L-H	D	Next
Write Cycle, Continue Burst; Bank 2	H	X	H	H	L	L	X	L-H	D	Next
Write Cycle, Continue Burst; Bank 2	H	H	X	H	L	L	X	L-H	D	Next
Read Cycle, Suspend Burst; Bank 1	X	H	H	H	H	H	L	L-H	Q	Current
Read Cycle, Suspend Burst; Bank 1	X	H	H	H	H	H	H	L-H	High-Z	Current
Read Cycle, Suspend Burst; Bank 2	H	X	H	H	H	H	L	L-H	Q	Current
Read Cycle, Suspend Burst; Bank 2	H	X	H	H	H	H	H	L-H	High-Z	Current
Read Cycle, Suspend Burst; Bank 1	H	H	X	H	H	H	L	L-H	Q	Current
Read Cycle, Suspend Burst; Bank 1	H	H	X	H	H	H	H	L-H	High-Z	Current
Read Cycle, Suspend Burst; Bank 2	H	H	X	H	H	H	L	L-H	Q	Current
Read Cycle, Suspend Burst; Bank 2	H	H	X	H	H	H	H	L-H	High-Z	Current
Write Cycle, Suspend Burst; Bank 1	X	H	H	H	H	L	X	L-H	D	Current
Write Cycle, Suspend Burst; Bank 1	H	H	X	H	H	L	X	L-H	D	Current
Write Cycle, Suspend Burst; Bank 2	H	X	H	H	H	L	X	L-H	D	Current
Write Cycle, Suspend Burst; Bank 2	H	H	X	H	H	L	X	L-H	D	Current



SYNCHRONOUS ONLY - TRUTH TABLE

Operation	E1#	E2#	GW#	G#	ZZ	CK	DQ
Synchronous Write-Bank 1	L	H	L	H	L	↑	High-Z
Synchronous Read-Bank 1	L	H	H	L	L	↑	
Synchronous Write-Bank 2	H	L	L	H	L	↑	High-Z
Synchronous Read-Bank 2	H	L	H	L	L	↑	
Synchronous Write-Bank 3	H	H	L	H	L	↑	High-Z
Synchronous Read-Bank 3	H	H	H	L	L	↑	
Synchronous Write-Bank 4	H	H	L	H	L	↑	High-Z
Synchronous Read-Bank 4	H	H	H	L	L	↑	
Snooze Mode	X	X	X	X	H	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on V _{CC} Relative to V _{SS}	-0.5V to +4.6V
V _{IN}	-0.5V to V _{CC} +0.5V
Storage Temperature	-55°C to +125°C
Operating Temperature (Commercial)	0°C to +70°C
Operating Temperature (Industrial)	-40°C to +85°C
Short Circuit Output Current	10 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	V _{CC}	3.14	3.3	3.6	V
Supply Voltage	V _{SS}	0.0	0.0	0.0	V
Input High	V _{IH}	2.0	3.0	V _{CC} +0.3	V
Input Low	V _{IL}	-0.3	0.0	0.8	V
Input Leakage	I _{LI}	-2	1	2	μA
Output Leakage	I _{LO}	-2	1	2	μA

DC ELECTRICAL CHARACTERISTICS - READ CYCLE

Description	Symbol	Typ	Max				Units
			8.5	9	12	15	
Power Supply Current	I _{CC1}	1.55	2.2	2.1	2.1	2.0	A
Power Supply Current Device Selected, No Operation	I _{CC}	750	1.5	1.5	1.0	1.0	A
Snooze Mode	I _{CCZZ}	150	200	200	200	200	mA
CMOS Standby	I _{CC3}	400	600	600	600	600	mA
Clock Running-Deselect	I _{CCK}	600	1.0	1.0	0.75	0.75	mA

AC TEST CIRCUIT

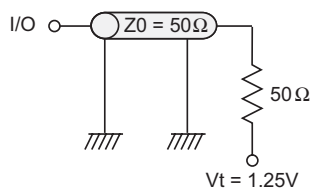


FIG. 2 AC Output Load Equivalent

AC TEST CONDITIONS

Parameter	I/O	Unit
Input Pulse Levels	V _{SS} to 3.0	V
Input and Output Timing Ref.	1.25	V
Output Test equivalencies	See figure at left	



BURST ADDRESS TABLE (MODE=NC/V_{CC})

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
A-A00	A-A01	A-A10	A-A11
A-A01	A-A00	A-A11	A-A10
A-A10	A-A11	A-A00	A-A01
A-A11	A-A10	A-A01	A-A00

BURST ADDRESS TABLE (MODE=V_{SS})

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
A-A00	A-A01	A-A10	A-A11
A-A01	A-A10	A-A11	A-A00
A-A10	A-A11	A-A00	A-A01
A-A11	A-A00	A-A01	A-A10

READ CYCLE TIMING PARAMETERS

Description	Sym	8.5ns		9ns		12ns		15ns		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Clock Cycle Time	t _{KHKH}	*	*	10		12		15		ns
Clock High Time	t _{KHKL}	*	*	4		5		5		ns
Clock Low Time	t _{KLKH}	*	*	4		5		5		ns
Clock to Output Valid	t _{KHQP}	*	*		9		10		12	ns
Clock to Output Invalid	t _{KHQX1}	*	*	3		3		3		ns
Clock to Output Low-Z	t _{KHQX}	*	*	2		2		2		ns
Output Enable to Output Valid	t _{GLQP}	*	*		4		4		5	ns
Output Enable to Output Low-Z	t _{GLQX}	*	*	0		0		0		ns
Output Enable to Output High-Z	t _{GHQZ}	*	*		4		4		5	ns
Address Setup	t _{AVKH}	*	*	2.5		2.5		2.5		ns
Bank Enable Setup	t _{EVKH}	*	*	2.5		2.5		2.5		ns
Address Hold	t _{KHAX}	*	*	1.0		1.0		1.0		ns
Bank Enable Hold	t _{KHEX}	*	*	1.0		1.0		1.0		ns

*TBD

FIG. 3 SYNCHRONOUS ONLY READ CYCLE

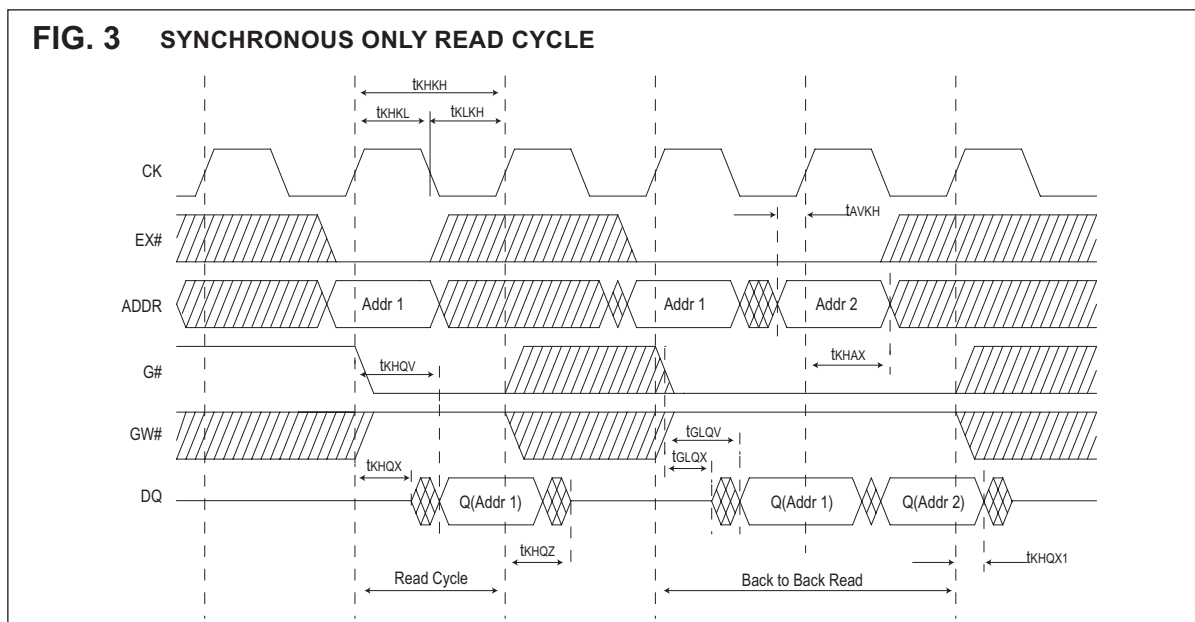
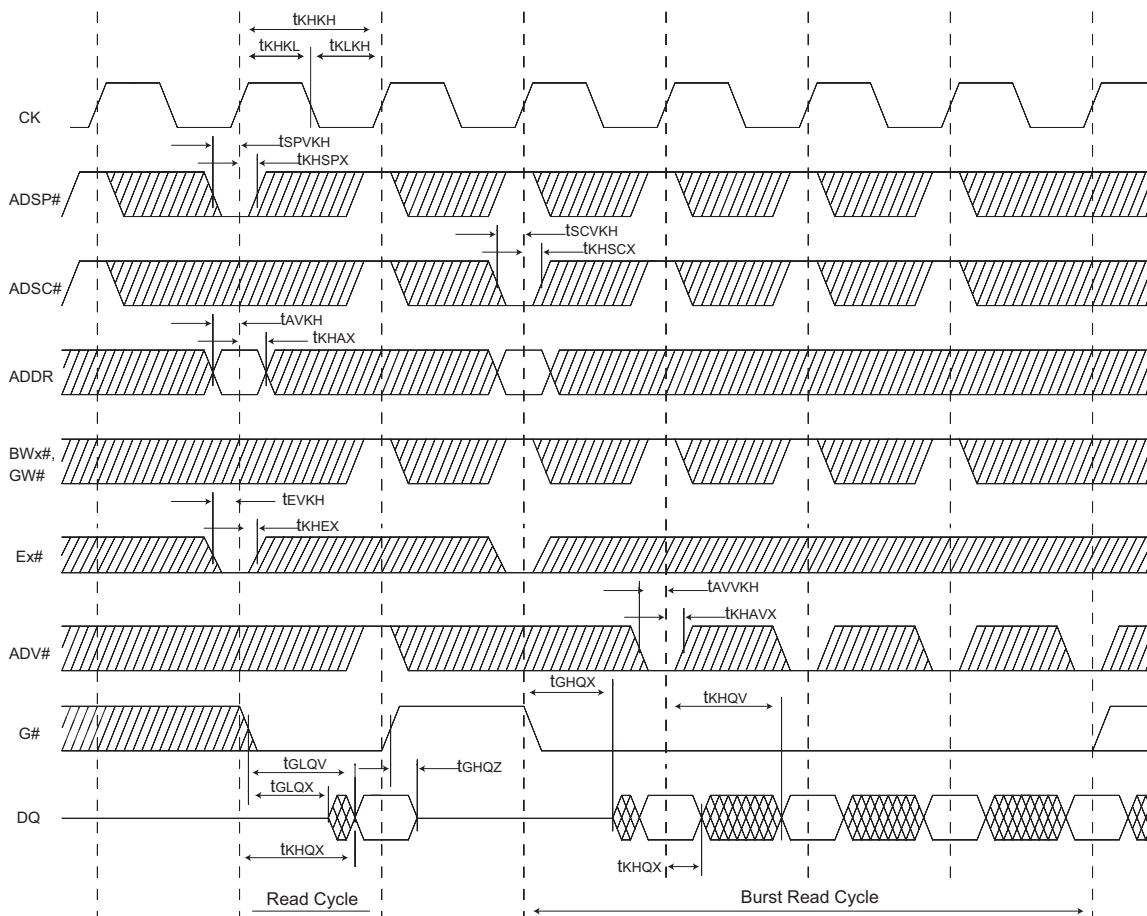




FIG. 4 SYNCHRONOUS-BURST READ CYCLE

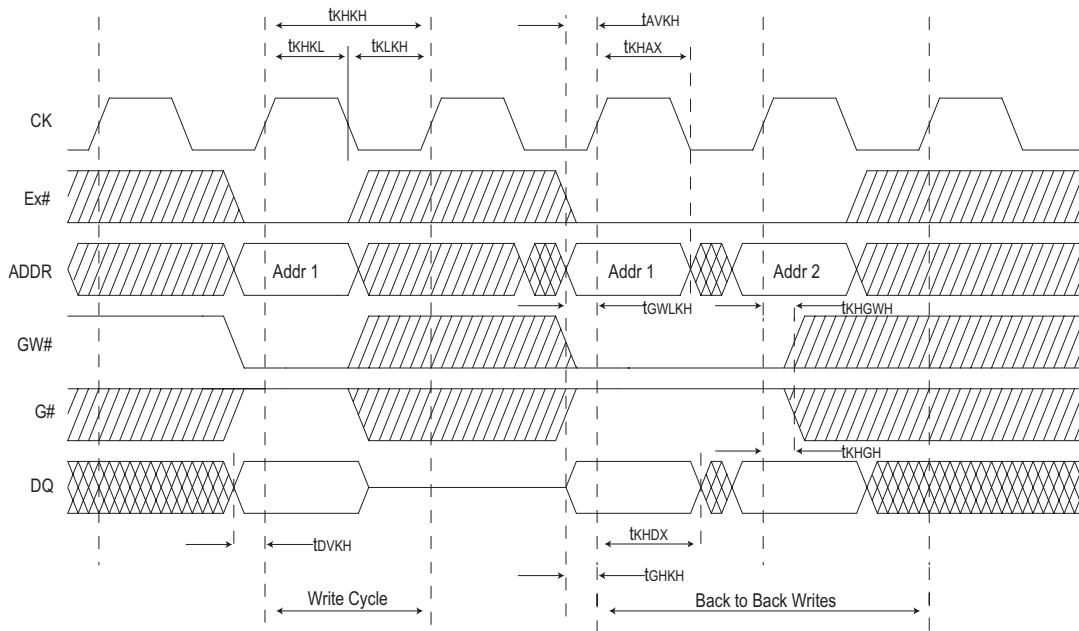




WRITE CYCLE TIMING PARAMETERS

Description	Sym	8.5ns		9ns		12ns		15ns		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Clock Cycle Time	t_{KHKH}			9		12		15		ns
Clock High Time	t_{KHKL}			4		5		5		ns
Clock Low Time	t_{KLKH}			4		5		5		ns
Address Setup	t_{AVKH}			2.5		2.5		2.5		ns
Address Hold	t_{KHAX}			1.0		1.0		1.0		ns
Bank Enable Setup	t_{EVKH}			2.5		2.5		2.5		ns
Bank Enable Hold	t_{KHGX}			1.0		1.0		1.0		ns
Global Write Enable Setup	t_{VWKH}			2.5		2.5		2.5		ns
Global Write Enable Hold	t_{KHGX}			1.0		1.0		1.0		ns
Data Setup	t_{DVKH}			2.5		2.5		2.5		ns
Data Hold	t_{KHDX}			1.0		1.0		1.0		ns

FIG. 5 SYNCHRONOUS (NON-BURST) WRITE CYCLE



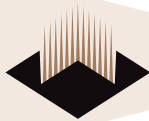
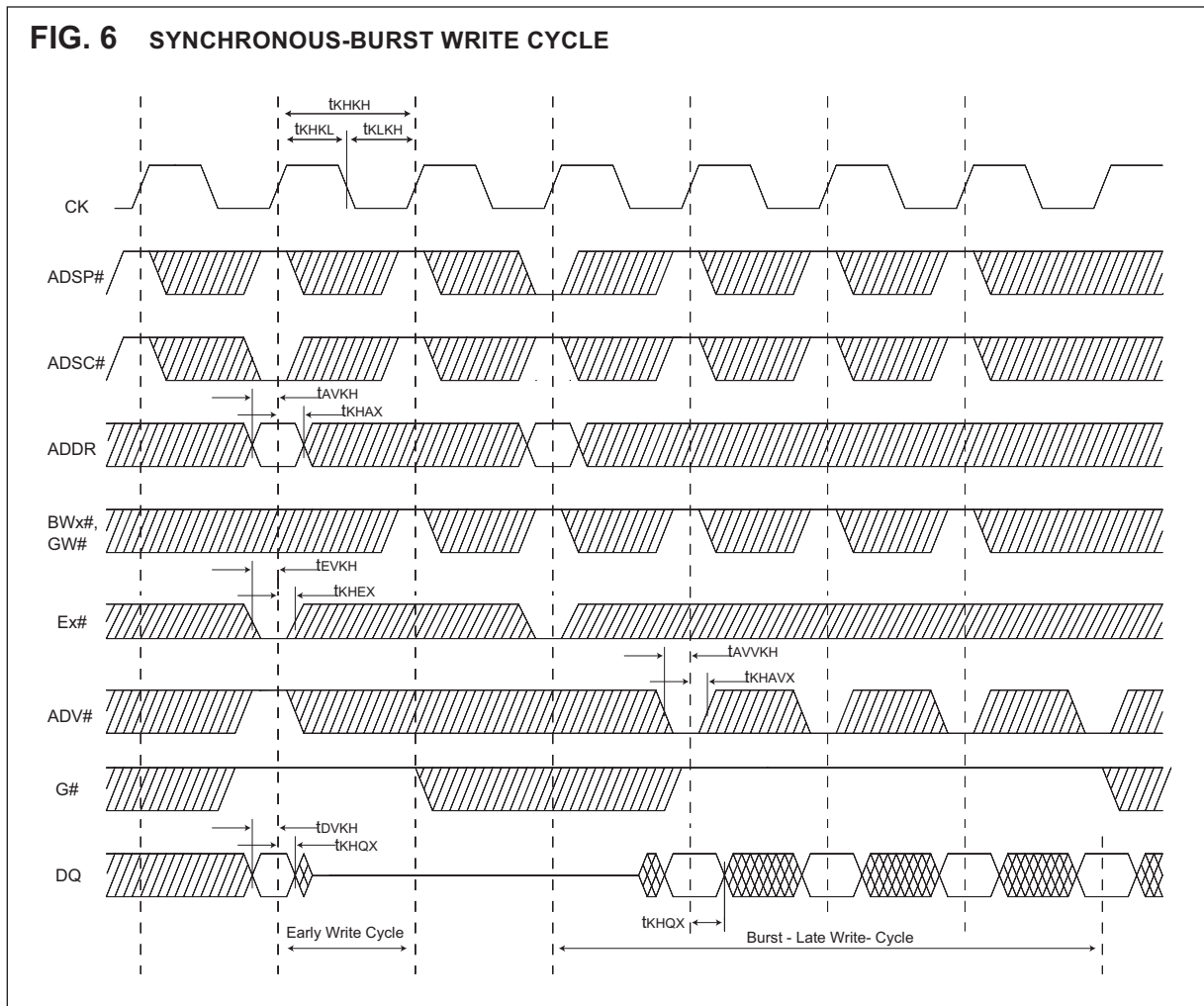


FIG. 6 SYNCHRONOUS-BURST WRITE CYCLE



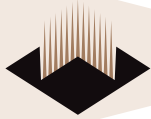
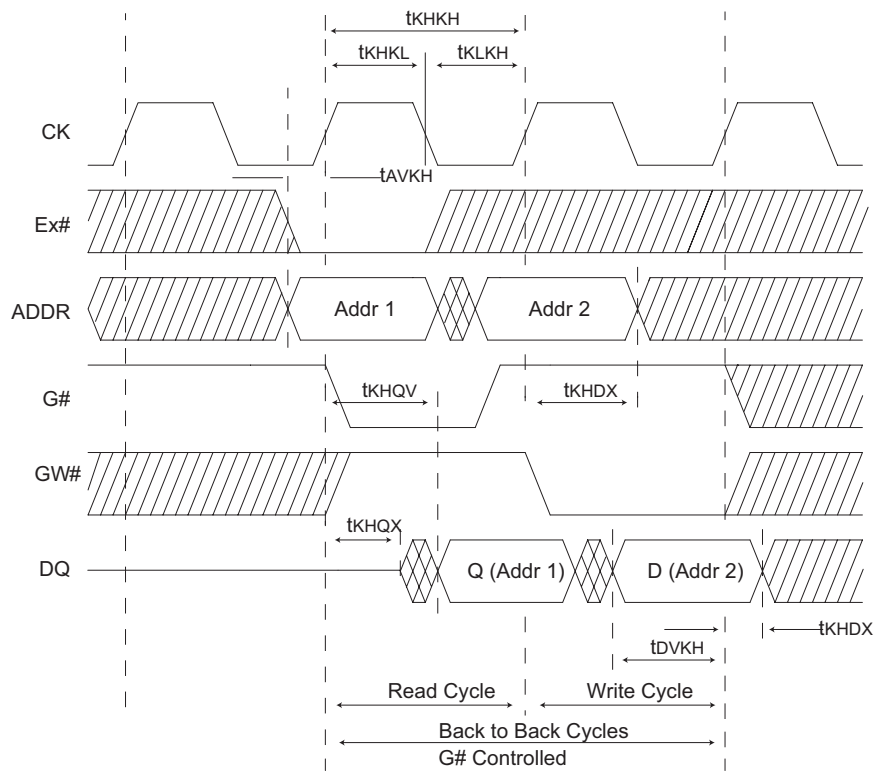
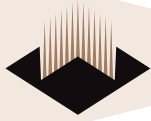
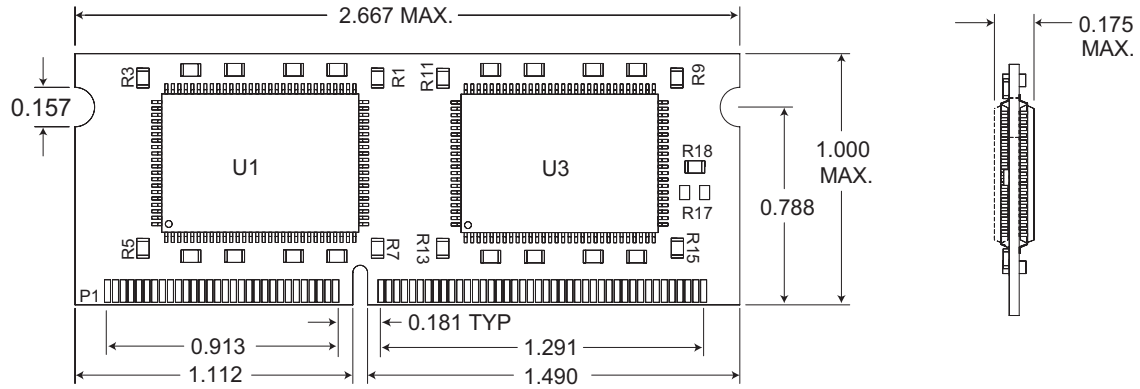


FIG. 7 SYNCHRONOUS (NON-BURST) READ/WRITE CYCLE





PACKAGE DESCRIPTION: 144 Lead SMALL OUTLINE DIMM
 Package No. 409



ALL DIMENSIONS ARE IN INCHES

ORDERING INFORMATION

Part Number	Organization	Voltage	Speed (ns)	Package
EDI2CG272128V85D1*	2x128Kx72	3.3	8.5	144 Small Outline DIMM
EDI2CG272128V9D1*	2x128Kx72	3.3	9	144 Small Outline DIMM
EDI2CG272128V12D1	2x128Kx72	3.3	12	144 Small Outline DIMM
EDI2CG272128V15D1	2x128Kx72	3.3	15	144 Small Outline DIMM

*Consult Factory for Availability