512Kx8 STATIC RAM CMOS, MODULE

FEATURES

- 512Kx8 bit CMOS Static
- Random Access Memory
  - Access Times 20 through 100ns
  - Data Retention Function (EDI8F8512LP)
  - TTL Compatible Inputs and Outputs
  - Fully Static, No Clocks
- High Density Packaging
  - 36 Pin SIP, No. 63
  - 32 Pin DIP, JEDEC Pinout, No. 91 (55-100ns)
  - 32 Pin DIP, JEDEC Pinout, No. 183 (20-35ns)
- Single +5V (±10%) Supply Operation

*This product is subject to change without notice.

DESCRIPTION

The EDI8F8512C is a 4096K bit CMOS Static RAM based on four 128Kx8 or 256Kx4 (high speed) Static RAMs mounted on a multi-layered epoxy laminate (FR4) substrate.

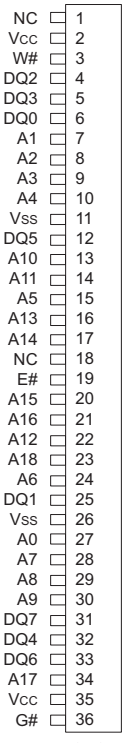
Functional equivalence to the monolithic four megabit Static RAM is achieved by utilization of an on-board decoder that interprets the higher order address(es) to select one of the128Kx8 or 256Kx4 Static RAMs.

The 32 pin DIP pinout adheres to the JEDEC standard for the four megabit device, to ensure compatibility with future monolithics.

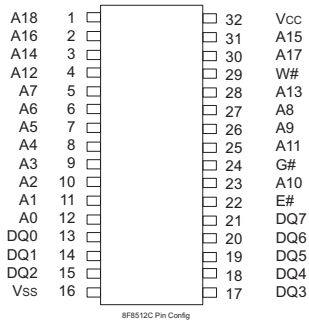
A low power version with data retention (EDI8F8512LP) is also available.

All inputs and outputs are TTL compatible and operate from a single 5V supply. Fully asynchronous, the EDI8F8512C requires no clocks or refreshing for operation.

FIG. 1 PIN CONFIGURATIONS



8F8512C Pin Config.

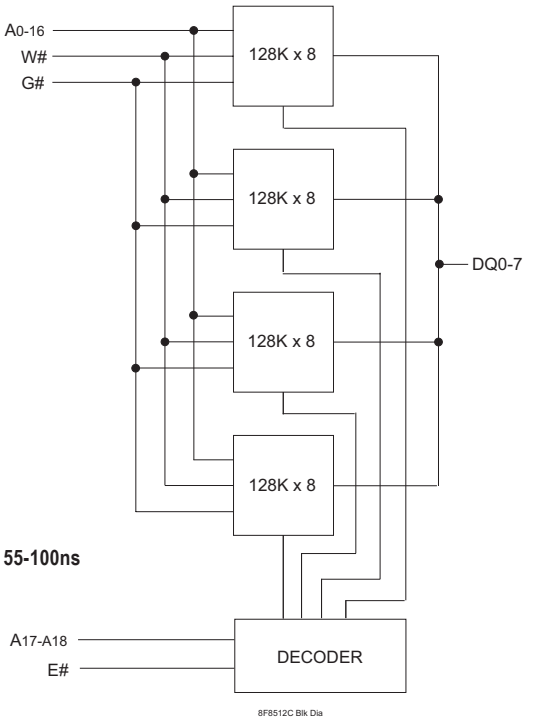


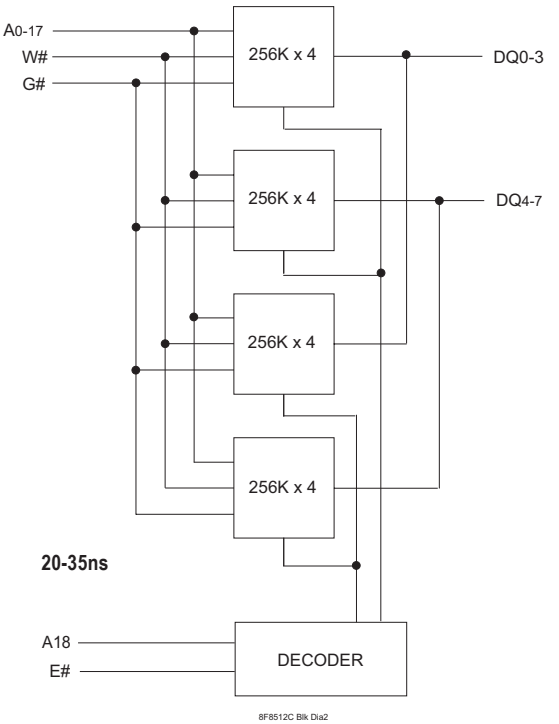
8F8512C Pin Config

PIN NAMES

A0-A18	Address Inputs
E#	Chip Enable
W#	Write Enable
G#	Output Enable
DQ0-DQ7	Common Data Input/Output
Vcc	Power (+5V±10%)
Vss	Ground
NC	No Connection

FIG. 2 BLOCK DIAGRAMS





ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS}	-0.5V to 7.0V
Operating Temperature T_A (Ambient) Commercial Industrial	 0°C to +70°C -40°C to +85°C
Storage Temperature	-55°C to +125°C
Power Dissipation	4 Watt
Output Current	20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	–	6.0	V
Input Low Voltage	V_{IL}	-0.3	–	0.8	V

AC TEST CONDITIONS

Input Pulse Levels		V_{SS} to 3.0V
Input Rise and Fall Times		5ns
Input and Output Timing Levels		1.5V
Output Load	20-35ns	1TTL = 30pF
	70-100ns	1TTL, CL = 100pF

(Note: For t_{EHQZ}, t_{GHQZ} and t_{WLQZ}, CL = 5pF)

DC ELECTRICAL CHARACTERISTICS

Parameter	Sym	Conditions		Min	Typ*		Max			Units
					≤35	≤55	20-25	35	55-100	
Operating Power Supply Current	I_{CC1}	W#, E# = V_{IL}, II/O = 0mA, Min Cycle			340	70	570	390	130	mA
Standby (TTL) Power Supply Current	I_{CC2}	E# ≥ V_{IH}, V_{IN} ≤ V_{IL} V_{IN} ≥ V_{IH}	DIP SIP	– –	50 –	10 –	85 –	85 –	55 65	mA
Full Standby Power Supply Current (CMOS)	I_{CC3}	E# ≥ V_{CC}-0.2V V_{IN} ≥ V_{CC}-0.2V or V_{IN} ≤ 0.2V	C LP	– –	5 –	2 40	40 –	40 –	5 400	mA µA
Input Leakage Current	I_{LI}	V_{IN} = 0V to V_{CC}		–	–	–	±10	±10	±10	µA
Output Leakage Current	I_{LO}	V I/O = 0V to V_{CC}		–	–	–	±10	±10	±10	µA
Output High Voltage	V_{OH}	I_{OH} = -1.0mA (≥70), or -4.0 (≤35)		2.4	–	–	–	–	–	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA (≥70), or 8.0mA (≤35)		–	–	–	0.4	0.4	0.4	V

*Typical: T_A = 25°C, V_{CC} = 5.0V

TRUTH TABLE

G#	E#	W#	Mode	Output	Power
X	H	X	Standby	HIGH Z	I_{CC2}/I_{CC3}
H	L	H	Output Deselect	HIGH Z	I_{CC1}
L	L	H	Read	D_{OUT}	I_{CC1}
X	L	L	Write	D_{IN}	I_{CC1}

CAPACITANCE

(f=1.0MHz, V_{IN}=V_{CC} or V_{SS})

Parameter	Sym	Max	Unit
Address Lines	CI	30	pF
Data Lines	CD/Q	43	pF
Chip Enable Line	CC	10	pF
Write and Output Enable Lines	CW	32	pF

These parameters are sampled, not 100% tested.

AC CHARACTERISTICS READ CYCLE

Parameter	Symbol JEDEC	Symbol Alt.	20ns Min.	20ns Max.	25ns Min.	25ns Max.	35ns Min.	35ns Max.	Units
Read Cycle Time	t_{AVAV}	t_{RC}	20		25		35		ns
Address Access Time	t_{AVQV}	t_{AA}		20		25		35	ns
Chip Enable Access Time	t_{ELQV}	t_{ACS}		20		25		35	ns
Chip Enable to Output in Low Z (1)	t_{ELQX}	t_{CLZ}	3		3		3		ns
Chip Disable to Output in High Z (1)	t_{EHQZ}	t_{CHZ}		10		12		15	ns
Output Hold from Address Change	t_{AVQX}	t_{OH}	3		3		3		ns
Output Enable to Output Valid	t_{GLQV}	t_{OE}		13		15		20	ns
Output Enable to Output in Low Z (1)	t_{GLQX}	t_{OLZ}	0		0		0		ns
Output Disable to Output in High Z (1)	t_{GHQZ}	t_{OHZ}		8		10		12	ns

Note: Parameter guaranteed, but not tested.

FIG. 3 READ CYCLE 1 - W# HIGH, G#, E# LOW

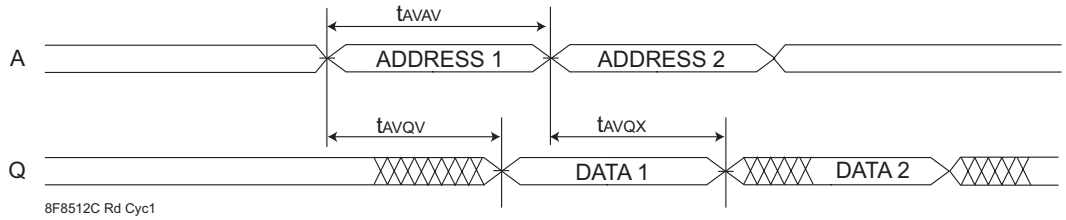
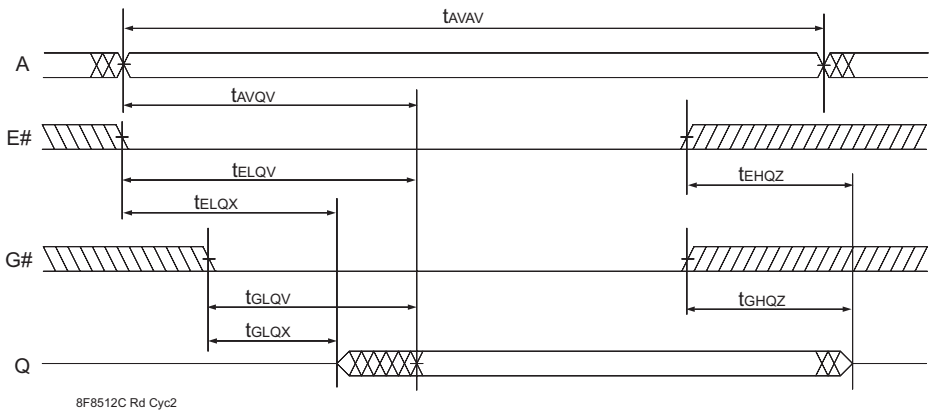


FIG. 4 READ CYCLE 2 - W# HIGH



AC CHARACTERISTICS READ CYCLE

Parameter	Symbol JEDEC	Symbol Alt.	55ns Min	55ns Max	70ns Min	70ns Max	85ns Min	85ns Max	100ns Min	100ns Max	Units
Read Cycle Time	t_{AVAV}	t_{RC}	55		70		85		100		ns
Address Access Time	t_{AVQV}	t_{AA}		55		70		85		100	ns
Chip Enable Access Time	t_{ELQV}	t_{ACS}		55		70		85		100	ns
Chip Enable to Output in Low Z (1)	t_{ELQX}	t_{CLZ}	5		5		5		5		ns
Chip Disable to Output in High Z (1)	t_{EHQZ}	t_{CHZ}		30		30		35		40	ns
Output Hold from Address Change	t_{AVQX}	t_{OH}	3		3		3		3		ns
Output Enable to Output Valid	t_{GLQV}	t_{OE}		40		40		45		50	ns
Output Enable to Output in Low Z (1)	t_{GLQX}	t_{OLZ}	0		0		0		0		ns
Output Disable to Output in High Z (1)	t_{GHQZ}	t_{OHZ}		30		30		35		40	ns

Note 1: Parameter guaranteed, but not tested.

AC CHARACTERISTICS WRITE CYCLE

Write Cycle Parameter	Symbol JEDEC	Symbol Alt.	20ns Min	20ns Max	25ns Min	25ns Max	35ns Min	35ns Max	Units
Write Cycle Time	t_{AVAV}	t_{WC}	20		25		35		ns
Chip Enable to End of Write	t_{ELWH} t_{ELEH}	t_{CW} t_{CW}	15 15		20 20		30 30		ns ns
Address Setup Time	t_{AVWL} t_{AVEL}	t_{AS} t_{AS}	0 0		0 0		0 0		ns ns
Address Valid to End of Write	t_{AVWH} t_{AVEH}	t_{AW} t_{AW}	15 15		20 20		30 30		ns ns
Write Pulse Width	t_{WLWH} t_{WLEH}	t_{WP} t_{WP}	15 15		20 20		25 25		ns ns
Write Recovery Time	t_{WHAX} t_{EHAX}	t_{WR} TWR	0 0		0 0		0 0		ns ns
Data Hold Time	t_{WHDX} t_{EHDX}	t_{DH} t_{DH}	3 3		3 3		3 3		ns ns
Write to Output in High Z (1)	t_{WLQZ}	t_{WHZ}	0	10	0	12	0	15	ns
Data to Write Time	t_{DVWH} t_{DVEH}	t_{DW} t_{DW}	12 12		15 15		20 20		ns ns
Output Active from End of Write (1)	t_{WHQX}	t_{WLZ}	3		3		3		ns

Note 1: Parameter guaranteed, but not tested.

AC CHARACTERISTICS WRITE CYCLE

Parameter	Symbol JEDEC	Symbol Alt.	55ns Min	55ns Max	70ns Min	70ns Max	85ns Min	85ns Max	100ns Min	100ns Max	Units
Write Cycle Time	t_{AVAV}	t_{WC}	55		70		85		100		ns
Chip Enable to End of Write	t_{ELWH} t_{ELEH}	t_{CW} t_{CW}	50 50		65 65		70 70		80 80		ns ns
Address Setup Time	t_{AVWL} t_{AVEL}	t_{AS} t_{AS}	0 0		0 0		0 0		0 0		ns ns
Address Valid to End of Write	t_{AVWH} t_{AVEH}	t_{AW} t_{AW}	50 50		65 65		70 70		80 80		ns ns
Write Pulse Width	t_{WLWH} t_{WLEH}	t_{WP} t_{WP}	50 50		65 65		70 70		80 80		ns ns
Write Recovery Time	t_{WHAX} t_{EHAX}	t_{WR} t_{WR}	0 0		0 0		0 0		0 0		ns ns
Data Hold Time	t_{WHDX} t_{EHDX}	t_{DH} t_{DH}	0 0		0 0		0 0		0 0		ns ns
Write to Output in High Z (1)	t_{WLQZ}	t_{WHZ}	0	30	0	30	0	35	0	40	ns
Data to Write Time	t_{DVWH} t_{DVEH}	t_{DW} t_{DW}	30 30		30 30		35 35		40 40		ns ns
Output Active from End of Write (1)	t_{WHQX}	t_{WLZ}	5		5		3		5		ns

Note 1: Parameter guaranteed, but not tested.

FIG. 7 WRITE CYCLE 1 - W# CONTROLLED

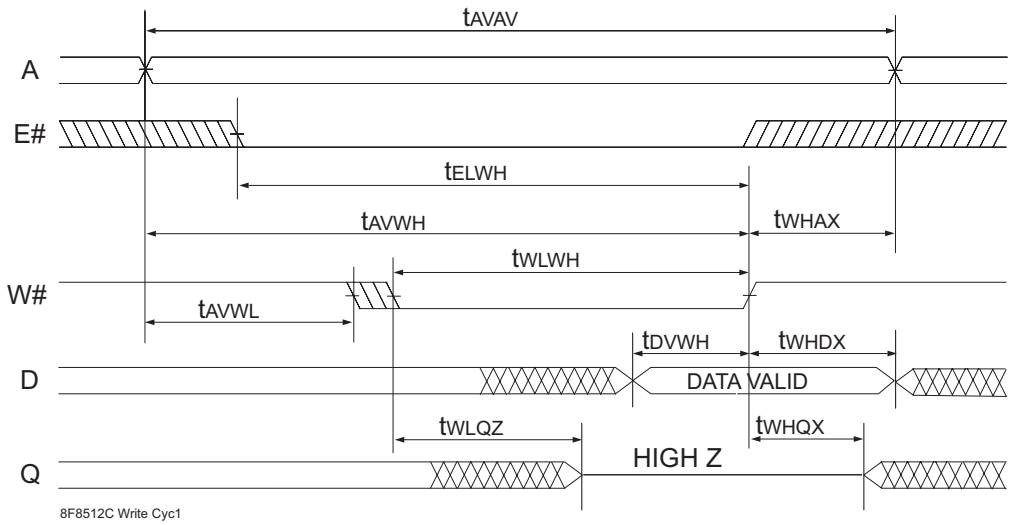
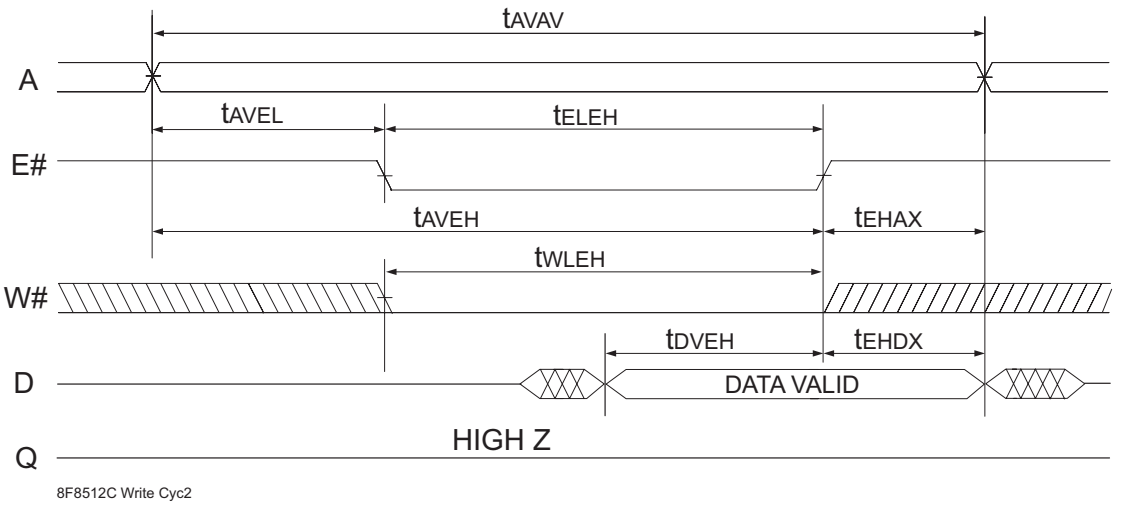


FIG. 8 WRITE CYCLE 2 - E# CONTROLLED



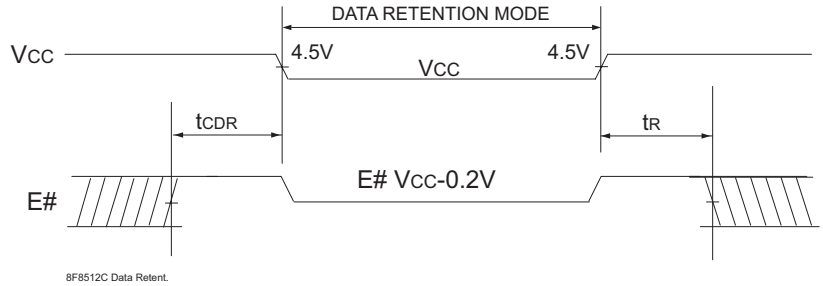
DATA RETENTION CHARACTERISTICS

LP 70-100ns Only

Characteristic	Sym	Test Conditions	Vcc	Min	Typ	Max		Unit
						70°C	85°C	
Data Retention Voltage	V_{CC}	V_{CC} = 0.2V		2	–	–	–	V
Data Retention Quiescent Current	I_{CCDR}	E# ≥ V_{CC} -0.2V	2V	–	10	125	185	µA
		V_{IN} ≥ V_{CC} -0.2V	3V	–	20	200	250	µA
Chip Disable to Data Retention Time (1)	t_{CDR}	or V_{IN} ≤ 0.2V		0	–	–	–	ns
Operation Recovery Time (1)	t_R			t_{AVAV}*	–	–	–	ns

*Read Cycle Time
Note: Parameter guaranteed, but not tested.

FIG. 9 DATA RETENTION E# CONTROLLED



ORDERING INFORMATION

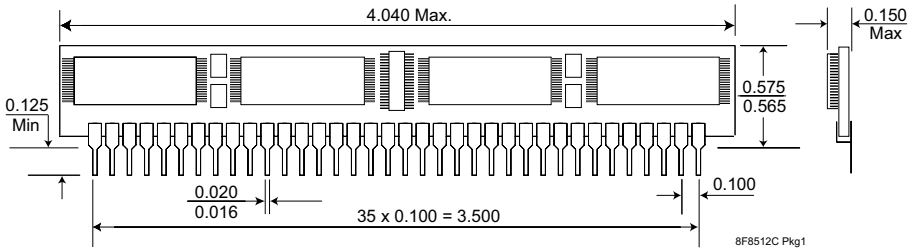
Standard Power	Speed (ns)	Package No.
EDI8F8512C20M6C	20	183
EDI8F8512C25M6C	25	183
EDI8F8512C35M6C	35	183
EDI8F8512C70BSC	70	63
EDI8F8512C85BSC	85	63
EDI8F8512C100BSC	100	63
EDI8F8512C55B6C	55	91
EDI8F8512C70B6C	70	91
EDI8F8512C85B6C	85	91
EDI8F8512C100B6C	100	91

Low Power with Data Retention	Speed (ns)	Package Leads
EDI8F8512LP70BSC	70	63
EDI8F8512LP85BSC	85	63
EDI8F8512LP100BSC	100	63
EDI8F8512LP70B6C	70	91
EDI8F8512LP85B6C	85	91
EDI8F8512LP100B6C	100	91

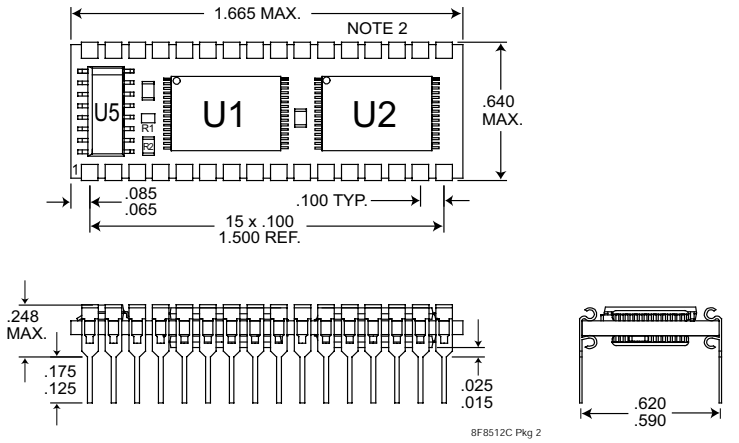
Note:
To order an Industrial grade product substitute the letter C in the Suffix with the letter I, e.g., EDI8F8512C70B6C becomes EDI8F8512C70B6I.

PACKAGE DESCRIPTIONS

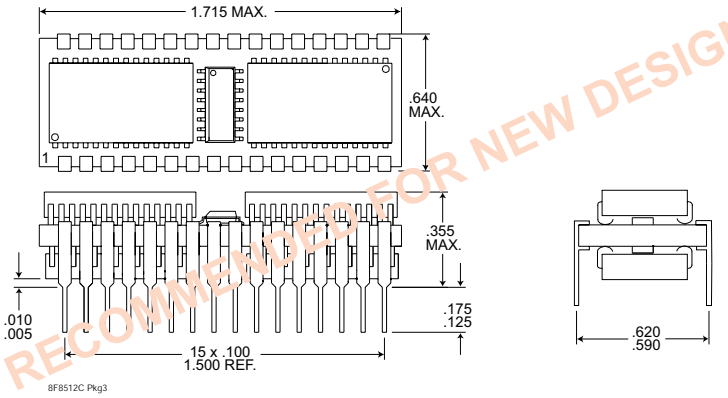
PACKAGE NO. 63: 36 PIN SINGLE-IN-LINE PACKAGE



PACKAGE NO. 91: 32 PIN DUAL-IN-LINE PACKAGE



PACKAGE NO. 183: 32 PIN DUAL-IN-LINE PACKAGE



ALL DIMENSIONS ARE IN INCHES