Digitally programmable 65 and 81 multiplex rate LCD Controller and Driver

Features

- Slim IC for COG, COF and COB technologies
- I²C & Serial bus interface
- Internal display data RAM
- 2 digitally programmable multiplex rates :
  - 81 rows x 102 columns
  - 65 rows x 118 columns
- LCD supply voltage internally generated and digitally programmable from 3V to 11V
- Low operating current consumption: 120µA (typ)
- No external components needed except one V_{LCD} capacitor
- On chip
  - 4 intermediate bias voltages generation
  - Oscillator for LCD refresh (no external components required)
- High noise immunity on inputs
- Row and column drivers mirroring for COG or COF connections flexibility
- Partial display mode with 17 active rows for current consumption reduction
- Sleep mode for a nearly null current consumption
- Wide V_{DD} supply voltage from 1.8V to 5V.
- Wide temperature range: -40°C to +85°C

Description

The EM6125 is a bit map controller and driver for full dot matrix monochrome STN LCD displays. The driving capability is 81 rows x 102 columns (10 rows of characters + one row of icons) or 65 rows x 118 columns (8 rows of characters + one row of icons). There is a one to one relation between LCD pixels and bits of the Display Data RAM.
The EM6125 is extremely low power consumption LCD controller and driver product. The typical current consumption is about 120µA with no external component except the capacitor connected to V_{LCD}. One important feature on EM6125 is the partial display mode, which enables important current consumption reduction. With this function selected, only 17 rows remain active, needed V_{LCD} decreases and the commutation frequencies of row and column drivers are also decreased. These three effects of partial display mode reduce drastically current consumption.

Typical Applications

- Mobile phones
- Smart cards
- Automotive displays
- Portable, battery operated products
- Balances and scales, utility meters

Typical Operating Configuration

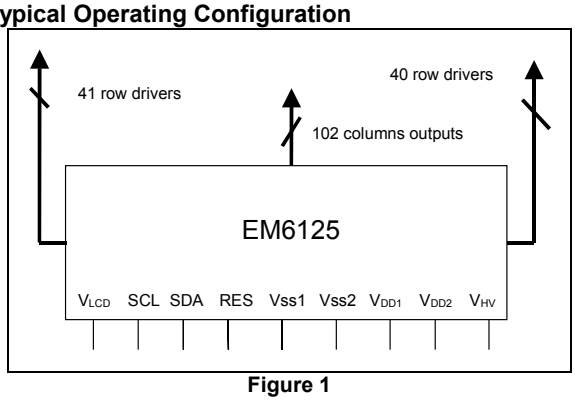


Figure 1

Pin Configuration

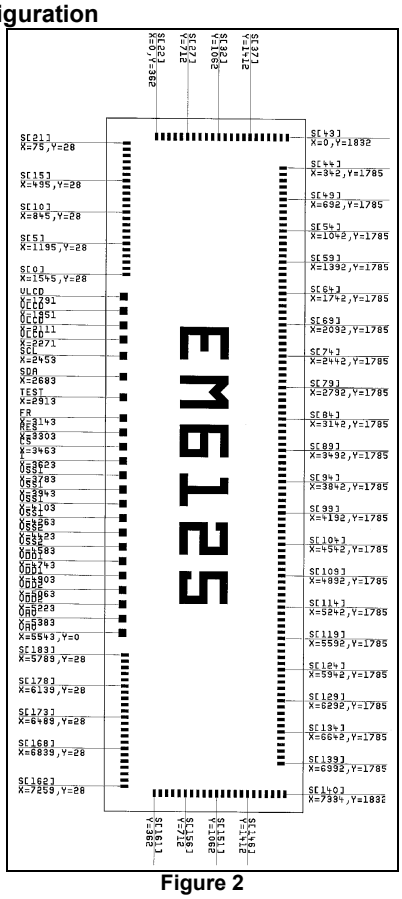


Figure 2

1 Absolute Maximum Ratings

Parameter	Symbol	Conditions
Supply voltage range	$V_{DD1,2}$	-0.3V to +6V
Supply voltage range	V_{HV}	-0.3V to +6V
Supply voltage range	V_{LCD}	V_{HV}-0.3V to +12V
All input voltages	V_{LOGIC}	-0.3V to $V_{DD1,2}$+0.3V
Voltages at S_0 to S_{184}	$V_{DISPLAY}$	-0.3V to V_{LCD} + 0.3V
Storage temperature range	T_{STO}	-65°C to +150 °C
Electrostatic discharge max. to MIL-STD-883C method 3015	V_{ESD}	1000V
Maximum soldering conditions	T_{SMAX}	250°C×10 s

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified electrical characteristics may affect device reliability or cause malfunction.

2 Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions should be taken as for any other CMOS components. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range.

3 Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	
Operating temperature	T_A	-40		+85	°C
Logic supply voltage	$V_{DD1,2}$	1.8	2.5	5.5	V
High voltage generator supply voltage	V_{HV}	2.4 *	2.5	5.5	V
LCD supply voltage	V_{LCD}	3	8	11	V

* Lower V_{HV} voltage is possible until the required V_{LCD} voltage is reached.

4 Electrical Characteristics

$V_{SS1,2}$ = 0V, V_{DD1} = V_{DD2} = 1.8V, V_{HV} = 2.4V, unless otherwise specified. T_A = -40°C to +85 °C unless otherwise specified.
Minimum required capacitor: 1µF on V_{LCD}, 100nF on $V_{DD1,2}$ and V_{HV}.

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Units
Supply Current						
Sleep mode	I_{DD}	Sleep = 1		10		nA
Sleep mode	I_{HV}	Sleep = 1		0.5		µA
Normal LCD refresh mode	I_{DD}	(note 1)		15	21	µA
Normal LCD refresh mode	I_{HV}	(note 2)		124	180	µA
Partial LCD refresh mode	I_{HV}	(note 3)		50	87	µA
Control Input Signals						
Input leakage	I_{IN}	V_i = V_{ss1} or V_{DD1}	-1		1	µA
Input capacitance	C_{IN}			8		pF
Low level input voltage	V_{IL}				0.3xV_{DD1}	V
High level input voltage	V_{IH}		0.7xV_{DD1}			V
LCD Outputs						
Internally generated LCD supply voltage	V_{LCD} 00000000b			3.02		V
	V_{LCD} 10001110b			8.02		V
V_{LCD} step between 2 consecutive programmed V_{LCD} Level	V_{LCD} step			35.2		mV
V bias tolerance	V bias tol.	(note 5)	-80		80	mV

Note 1: Measured on V_{DD1} + V_{DD2}, all outputs open, SDA and SCL at V_{SS}, RES at V_{DD1}, multiplex rate 81, x5 voltage multiplier, V_{LCD} = 10001110b, DDRAM loaded with checker pattern
Note 2: Measured on V_{HV}, same conditions as (note 1).
Note 3: Measured on V_{HV}, all outputs open, SDA and SCL at V_{SS}, RES at V_{DD1}, partial display mode, ×2 voltage multiplier, V_{LCD} = 00101011b, DDRAM loaded with checker pattern.
Note 4: With internal voltage multiplier, the maximum V_{LCD} voltage depends on V_{HV}, programmed voltage multiplier and display load.
Note 5: V_1, V_2, V_3 and V_4 bias levels measured with V_{LCD} = 7V, on 1 LCD row driver output and 1 LCD column driver output, multiplex rate 81, T_A = 25 °C, load = ±10µA.

5 Timing Characteristics

$V_{SS1,2}$ = 0V, **V_{DD1} = V_{DD2} = 1.8V**, V_{HV} = 2.4V, T_A = -40°C to +85 °C unless otherwise specified.

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Units
Internal frame frequency for LCD refresh	f_{FR}	(note 1)		75 x mux		Hz
Minimum reset pulse width	t_{RW}		70			ns
I2C timing characteristics						
SCL frequency	f_{I2C}				1600	kHz
SCL low period	t_{LOW}		350			ns
SCL high period	t_{HIGH}		100			ns
SDA setup time	t_{SUDAT}		10			ns
SDA hold time	t_{HDDAT}		20			ns
SCL and SDA rise time	t_R				200	ns
SCL and SDA fall time	t_F				200	ns
Setup time for a repeated start condition	t_{SUSTA}		20			ns
Hold time for a start condition	t_{HDSTA}		20			ns
Setup time for a stop condition	t_{SUSTO}		20			ns
Spike width on SCL and SDA	t_{SW}				20	ns
Time before a new transmission can start	t_{BUF}		100			ns
Capacitive bus line load	C_b				400	pF
Serial bus timing characteristics						
SCL frequency	f_{SER}				4	MHz
SCL low period	t_{CL}		70			ns
SCL high period	t_{CH}		130			ns
SDA setup time	t_{DS}		20			ns
SDA hold time	t_{DH}		50			ns
SCL rise time	t_{CR}				200	ns
SCL fall time	t_{CF}				200	ns
CS setup time	t_{SUCS}		10			ns
CS hold time	t_{HDCS}		130			ns
Time before a new transmission can start, CS minimum high time.	t_{BUFCS}		70			ns

Note 1: Measured on pad FR.

$V_{SS1,2}$ = 0V, **V_{DD1} = V_{DD2} = 2.5V**, V_{HV} = 2.4V, T_A = -40°C to +85 °C unless otherwise specified.

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Units
Minimum reset pulse width	t_{RW}		50			
I2C timing characteristics						
SCL frequency	f_{SCL}				2100	kHz
SCL low period	t_{LOW}		190			ns
SCL high period	t_{HIGH}		60			ns
SDA setup time	t_{SUDAT}		10			ns
SDA hold time	t_{HDDAT}		20			ns
SCL and SDA rise time	t_R				200	ns
SCL and SDA fall time	t_F				200	ns
Setup time for a repeated start condition	t_{SUSTA}		20			ns
Hold time for a start condition	t_{HDSTA}		20			ns
Setup time for a stop condition	t_{SUSTO}		20			ns
Spike width on SCL and SDA	t_{SW}				10	ns
Time before a new transmission can start	t_{BUF}		40			ns
Capacitive bus line load	C_b				400	pF
Serial bus timing characteristics						
SCL frequency	f_{SCL}				5.2	MHz
SCL low period	t_{CL}		50			ns
SCL high period	t_{CH}		80			ns
SDA setup time	t_{DS}		15			ns
SDA hold time	t_{DH}		40			ns
SCL rise time	t_{CR}				200	ns
SCL fall time	t_{CF}				200	ns
CS setup time	t_{SUCS}		10			ns
CS hold time	t_{HDCS}		80			ns
Time before a new transmission can start, CS minimum high time.	t_{BUFCS}		50			ns

5.1 Timing Waveforms

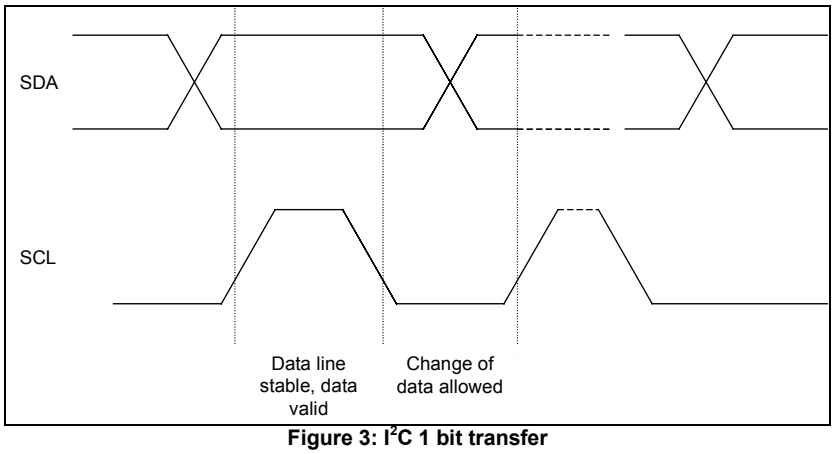


Figure 3: I²C 1 bit transfer

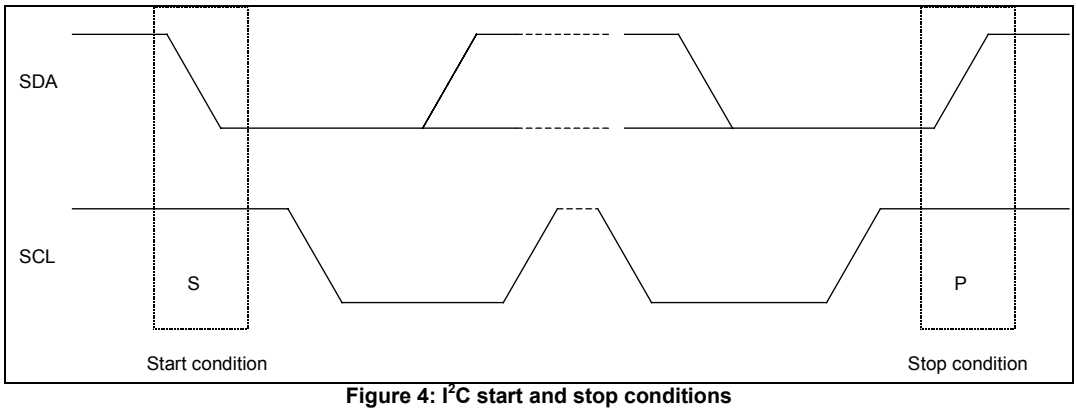


Figure 4: I²C start and stop conditions

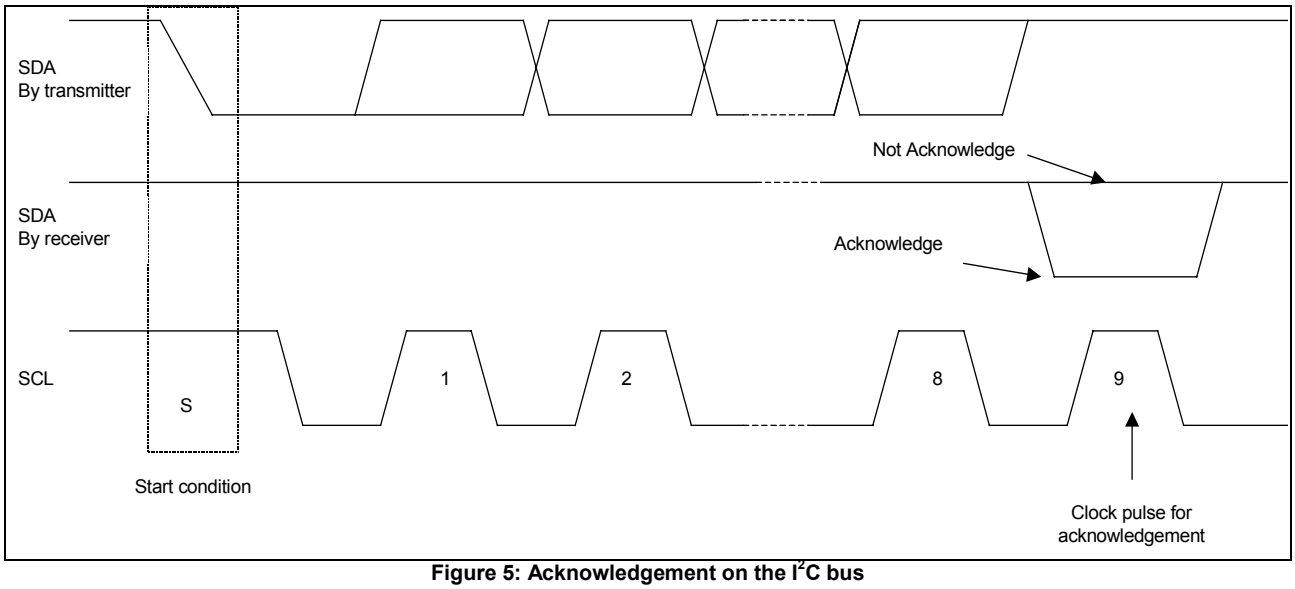


Figure 5: Acknowledgement on the I²C bus

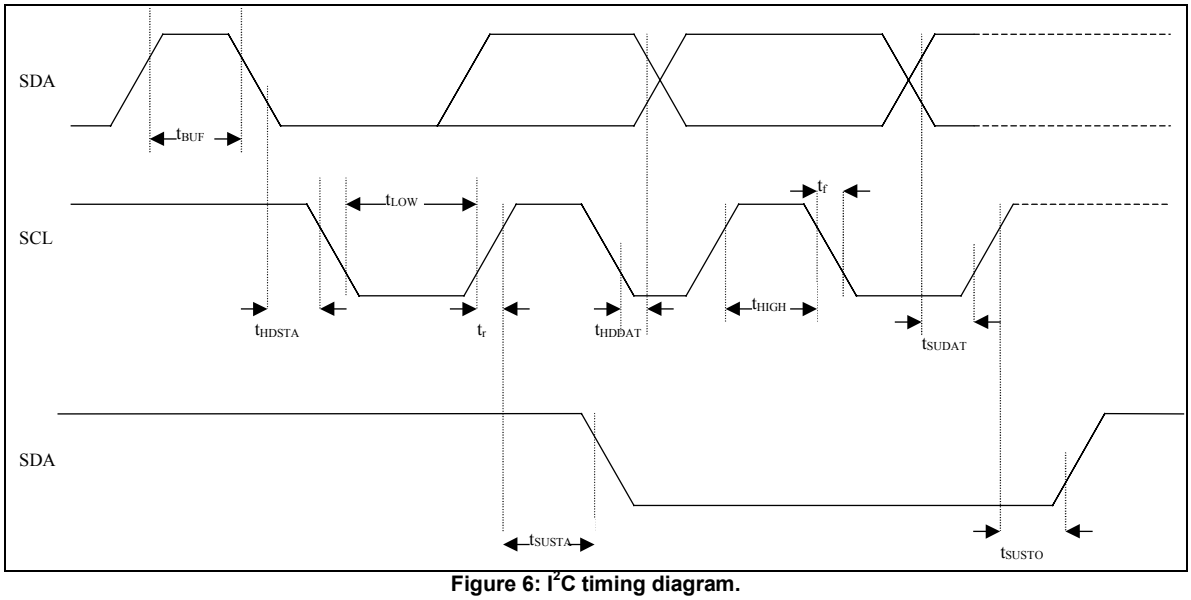


Figure 6: I²C timing diagram.

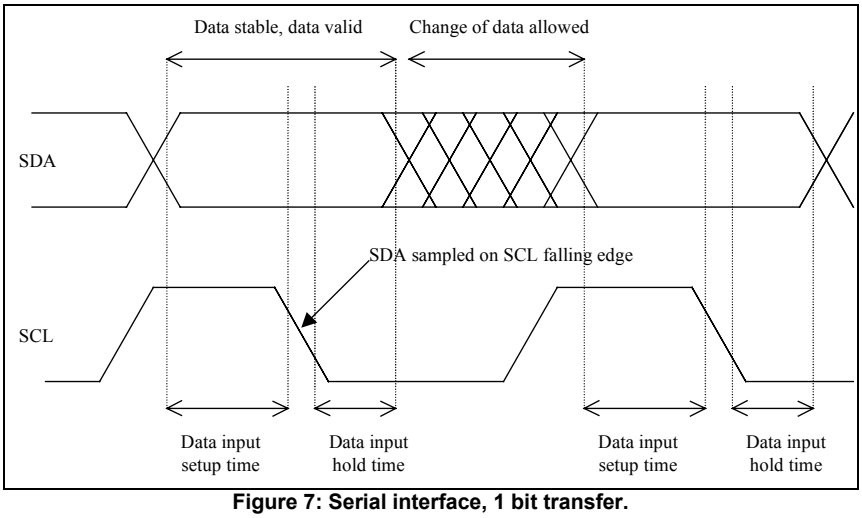


Figure 7: Serial interface, 1 bit transfer.

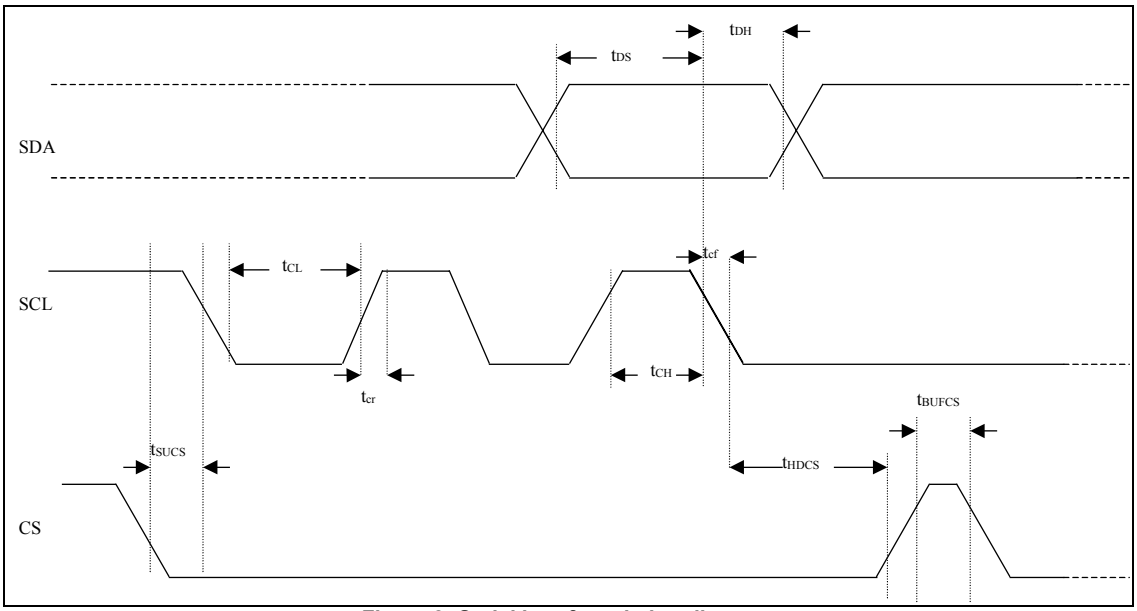


Figure 8: Serial interface timing diagram.

6 Block diagram

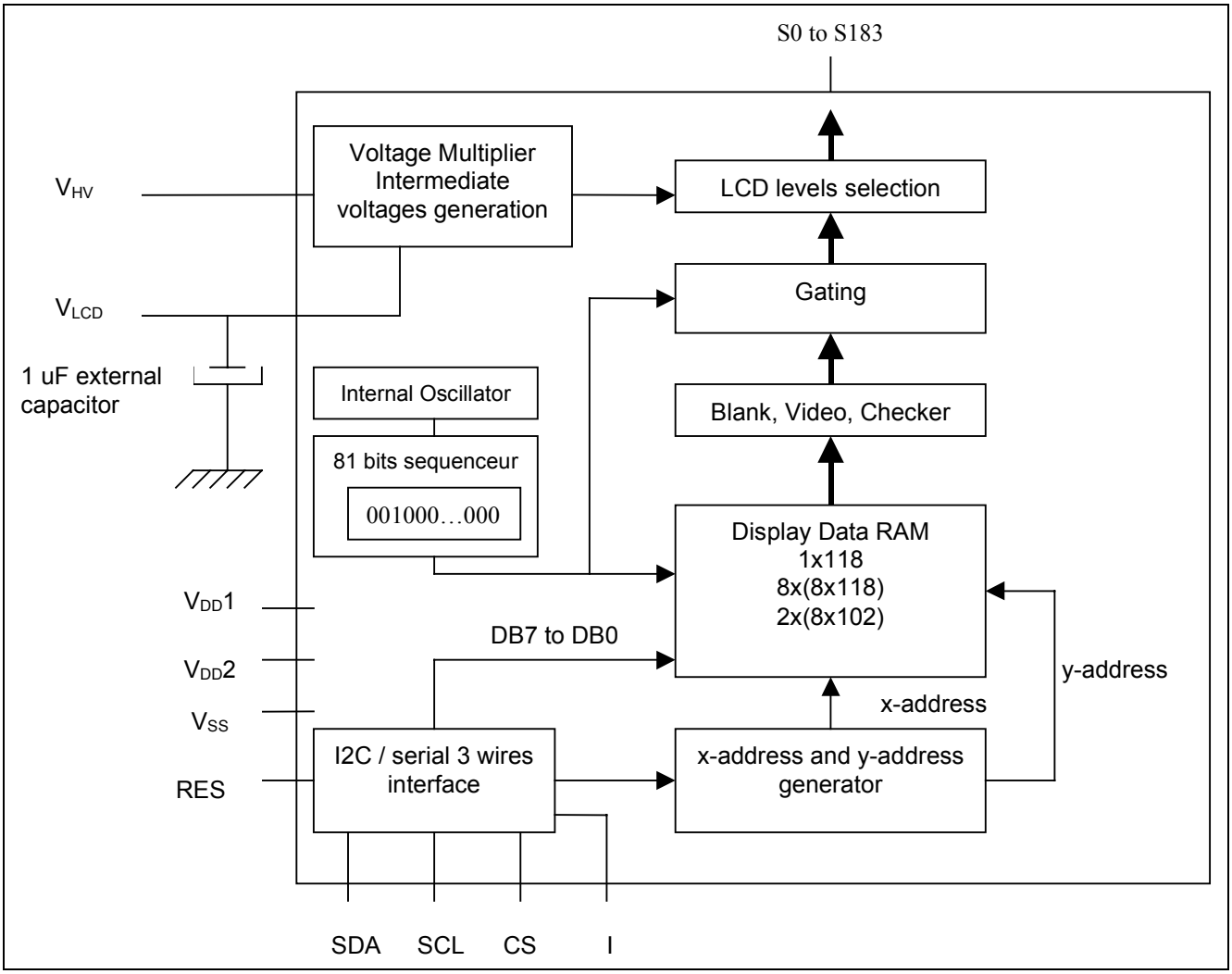


Figure 9: Block diagram.

7 Pin description

Symbol	Pad Type	Description
S_0 to S_{183}	Output	LCD driver outputs
S_0 to S_{32} and S_{151} to S_{183}	Output	LCD row driver outputs $S_0 = S_{184}$
S_{33} to S_{40} and S_{143} to S_{150}	Output	LCD row driver outputs when multiplex rate 81 is selected LCD column driver outputs when multiplex rate 65 is selected
S_{41} to S_{142}	Output	LCD column driver outputs
V_{HV}	Positive power supply	Supply voltage for internal voltage multiplier
$V_{DD1,2}$	Positive power supply	Supply voltage for logical and analog parts
$V_{SS1,2}$	Ground power supply	Ground power supply
I	Input	Interface protocol selection input
RES	Input	External reset input, active low
CS	Input	Chip select input
FR	Input/output	Frame frequency input/output
TEST	Input/output	Test
SDA	Input/output	Serial data input
SCL	Input	Serial clock
V_{LCD}	Positive power supply	LCD supply voltage

Table 1: Pin description

S0 to S183: Connected to LCD electrodes, it should be left open if not used. S0 and S183 are internally connected together.

V_{HV}: Supply voltage for internal voltage multiplier, it could be a different voltage value than for $V_{DD1,2}$.

$V_{DD1,2}$: Logic and analog power supplies. V_{DD1} and V_{DD2} are not connected inside EM6125 but have to be connected outside to the same potential. For chip on glass application, it is advised to keep V_{DD1} and V_{DD2} separated until their connection to 1 µF capacitor.

$V_{SS1,2}$: Ground supply for logic and high voltage generator. V_{SS1} is connected to substrate. Same precautions than for $V_{DD1,2}$ should be taken to connect these pads.

I: Selects the chosen interface protocol. For chip on glass applications, it can be directly connected to V_{SS1} or V_{DD1} on glass.

RES: External reset, a reset cycle must be applied at power on (reset at low level when power on).

CS: Active low chip select, when serial interface is used it enables data transfer. If I^2C is used, it must be connected at V_{SS1} or V_{DD1} pads.

FR: Outputs LCD refresh frame frequency, used for test. It must be left open.

TEST: Test pad, it must be left open.

SDA: Serial data input used for I^2C interface as for 3 wires serial interface.

SCL: Serial clock input used to latch SDA for I^2C interface as for 3 wires serial interface.

V_{LCD}: LCD voltage supply (generation of LCD waveforms applied to S0 to S183). It is normally internally generated from V_{HV} supply voltage. 1 µF capacitor is required between V_{LCD} and V_{SS}. External power supply is also possible; in this configuration V_{LCD} must be programmed at its lower value and V_{HV} connected to V_{SS2}.

8 Functional description

8.1 Selection of interface type

There are two different serial interfaces available on EM6125. Selection depends on logical value applied on pad I.

- If I = 0, serial interface is selected: 3 wires with Chip Select CS, Serial Clock SCL and Serial Data SDA.
- If I = 1, I^2C protocol is selected: 2 wires with Serial Clock SCL and Serial Data SDA. CS must be connected to V_{SS} or V_{DD1}.

I	Interface
0	3 wires serial interface
1	I^2C

Table 2: Interface selection

8.2 Serial interface

The serial interface consists of 3 wires: Chip Select CS, Serial Clock SCL and Serial Data SDA. The information is exchanged byte-wide and is shifted serially in the LCD driver at SCL fall edge.

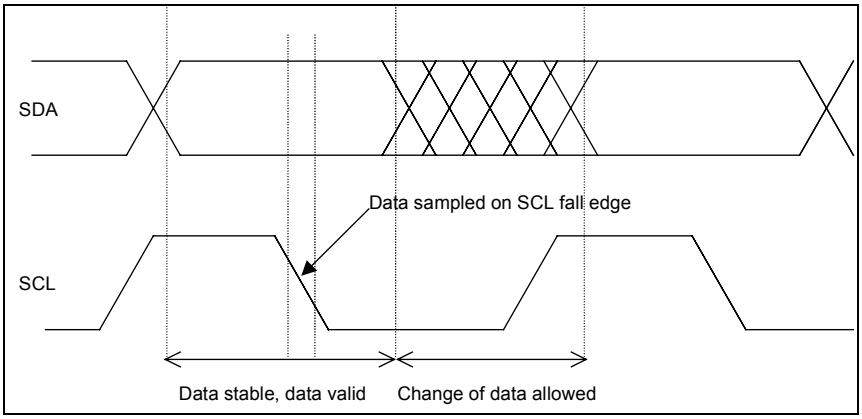


Figure 10: Serial interface, 1 bit transfer

Transfer of data is unidirectional from micro controller to EM6125. When CS is activated at low level the communication is enabled and must stay low for the rest of the transaction. Data transfer begins with one control byte. This control bytes is transferred MSB first, it consists in:

MSB							LSB
C0	DC	Test[2]	Test[1]	Test[0]	Ini[2]	Ini[1]	Ini[0]

C_0 is the continuation bit:

- If C_0 = 1, the control byte is followed by 1 data byte only, the next byte is a new control byte.
- If C_0 = 0, all the following bytes are data bytes until data transfer is stopped.

DC selects data bytes or command bytes to be send after the control byte:

- If DC = 1, the following data byte(s) is (are) written in the Display Data RAM. First data byte is stored at the address specified by the x-address and y-address pointers. Data pointers are automatically updated for each byte written in the DDRAM (see DDRAM description).
- IF DC = 0, the following data byte is a command byte. It enables initialization of functions (multiplex rate, number of voltage multiplier stages, V_{LCD} programming, partial display settings…).

Bits ini2, ini1 and ini0 select the initialization register to be set by the following command byte (see Table 4: EM6125 instructions).

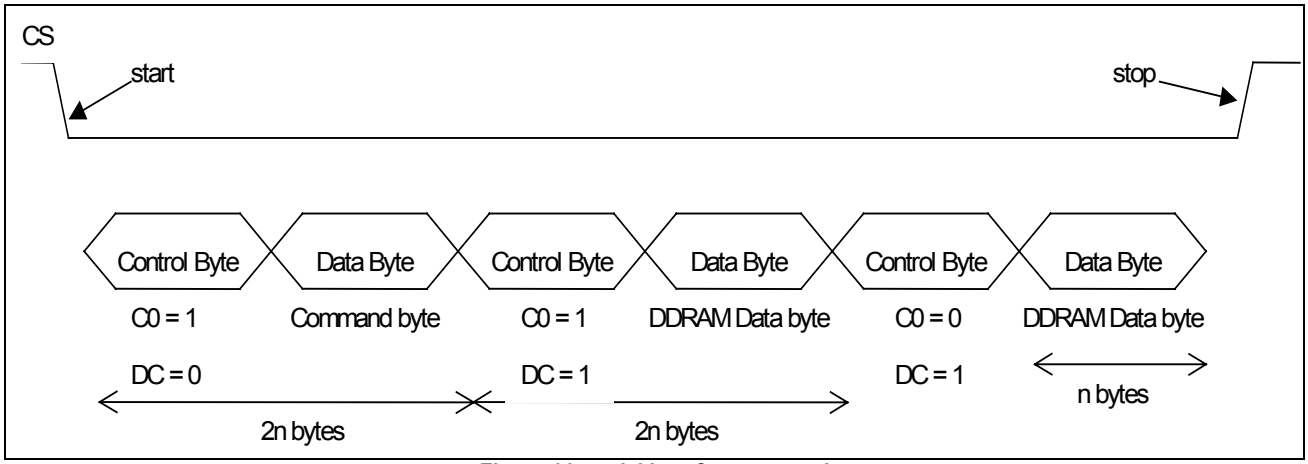
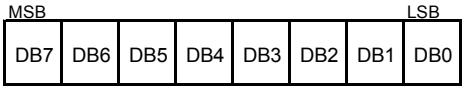


Figure 11: serial interface protocol

Data byte is transferred with MSB bit first, LSB bit last:



If CS goes high during a byte transfer, this byte is invalid but all previously transmitted data are valid. While CS is high the serial interface is kept in reset that means internal interface counter and disables data transfer. To prevent transmission errors, CS should be at high level when transfer is stopped.

8.3 I²C interface

The EM6125 can be interfaced with a slave I²C protocol (see description I2C protocol). The I²C bus consists in 2 wires: SCL (Serial Clock Line) and SDA (Serial Data Line). Both lines must be connected to $V_{DD1,2}$ via a pull up resistor. EM6125 pad SCL is input, pad SDA is bi-directional with pull down open drain. EM6125 supports initialization and RAM write and status read access.

8.3.1 Start and stop conditions

Data transfer begins by a falling edge on SDA when SCL is at high level, this is the start condition (S), initiated by the I²C bus master. It is stopped with a rising edge on SDA and SCL at high level, this is the stop condition (P) (see Figure 4: I2C start and stop conditions).

8.3.2 Bit transfer

One data bit is transferred during each SCL pulse. The data on the SDA line must remain stable during the high period of SCL pulses, as any changes at this time would be interpreted as start or stop conditions. Data is always transferred with MSB first.

8.3.3 Acknowledge

After a start condition, data bits are transferred to EM6125. Each byte is followed by an acknowledge bit: the transmitter let the SDA line high (no pull down) and generates a high SCL pulse; if transfer concerns the EM6125 slave receiver and has performed correctly, it generates a low SDA level (pull down activated). SDA remains stable during the high period of the acknowledge related SCL pulse. After acknowledge, EM6125 let SDA line free, enabling the transmitter to continue transfer or to generate a stop condition.

8.4 I²C protocol

The EM6125 has a slave address, coded on 7 bits: 0000000.

After a start condition, the slave address + RW bit must be send first. If the slave address does not match with the EM6125 ones there is no acknowledge from LCD driver and the following data transfer will not affect the chip.

If the slave address corresponds to EM6125 slave address, it will acknowledge (pull SDA down to logical low level) and data transfer is enabled.

The 8th bit RW sets the chip in write mode or read status mode, it is read for data transfer.

8.4.1 Write mode

If RW = 0, EM6125 is accessed by the micro controller.

Data transfer bytes can be either control bytes or data bytes. Data transfer always begins with a control byte (described in fig.1). It sets bits C0, DC, ini2, ini1 and ini0.

C0 is the continuation bit:

- If C_0 = 1, the control byte is followed by 1 data byte only, the next byte is a new control byte.
- If C_0 = 0, all the following bytes are data bytes until data transfer is stopped.

DC selects data bytes or command bytes to be send after the control byte:

- If DC = 1, the following data byte(s) is (are) written in the Display Data RAM. First data byte is stored at the address specified by the x-address and y-address pointers. Data pointers are automatically updated for each byte written in the DDRAM (see DDRAM description).
- IF DC = 0, the following data byte is a command byte. It enables initialization of functions (multiplex rate, number of voltage multiplier stages, V_{LCD} programming, partial display settings…).

Bits ini2, ini1 and ini0 select the initialization register to be set by the following command byte (see Table 4: EM6125 instructions).

8.4.2 Read Mode (RW = 1)

EM6125 will output one status byte after slave address. This status byte consists in 8 initialization bits previously set by command bytes or the reset cycle (see Table 4: EM6125 instructions).

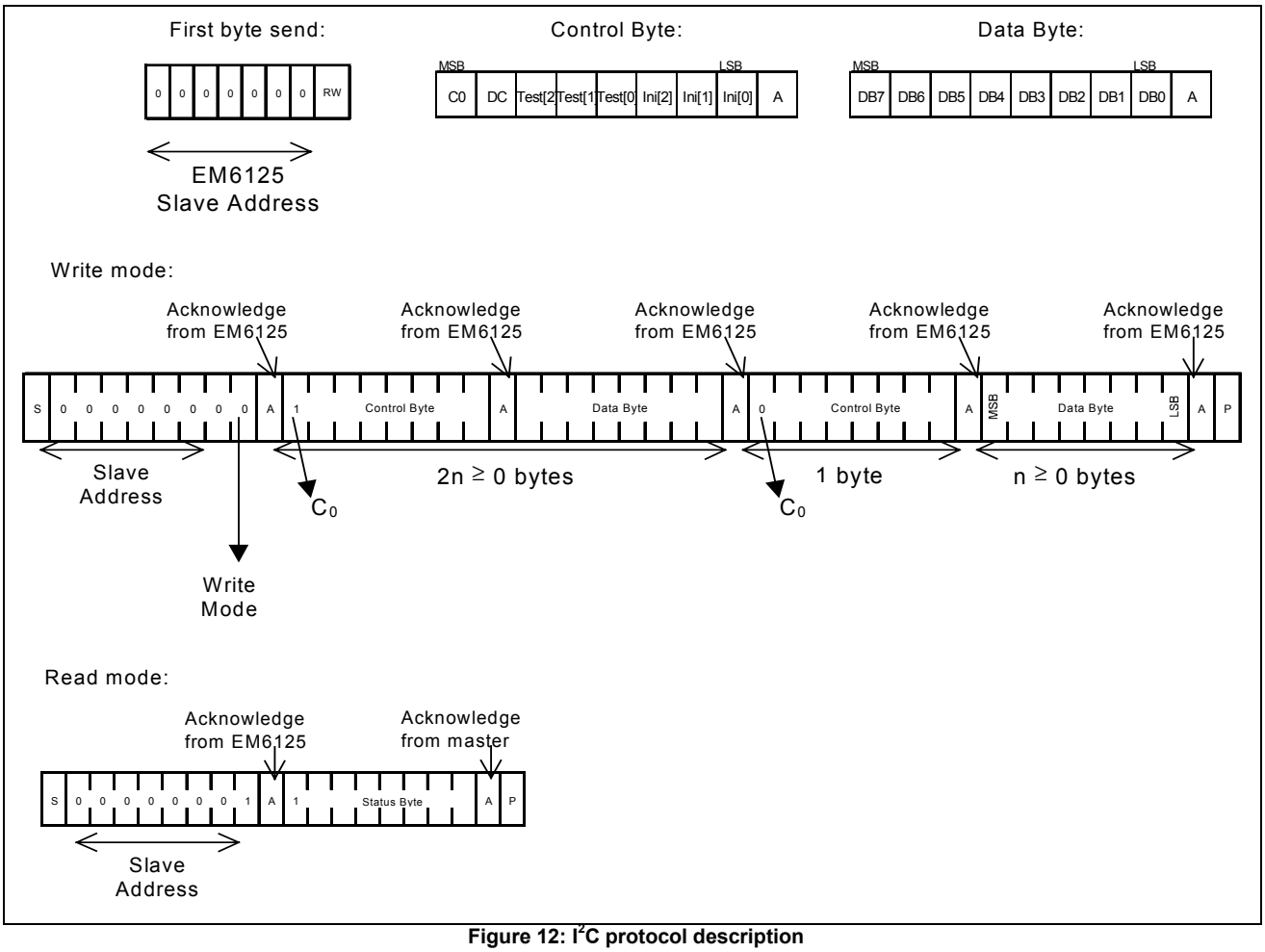


Figure 12: I²C protocol description

8.5 Display Data RAM

The EM6125 contains a RAM, which stores the display data; there is a one to one correspondence between the bit stored in the RAM and one LCD pixel.

8.5.1 DDRAM description

DDRAM consists in:

- 1 bank of 118 bits (row 0)
- 8 banks of 118 bytes (rows 1 to 64)
- 2 banks of 102 bytes (rows 65 to 80)

DDRAM is read row by row for display refresh. Each row corresponds to one pad, which is activated when the corresponding row is read.

DDRAM is accessed via the interface. Bytes are stored at the column specified by x-address pointer and the bank specified by y-address pointer. These pointers are set by the corresponding instruction “Initialization 1” and “Initialization 2” and are automatically incremented or decrement after each byte written in the DDRAM (see

DDRAM addressing and Table 5: Internal functions after reset.)

For bank 0 only data byte 7 (DB7) is stored in row 0, DB6 to DB0 are not used. For bank 1 to 10 (y-address = 1 to 10), DBX is stored at row ((8 x y-address)-X).

If Mux Mode = 0, the DDRAM provides a 65 rows and 118 columns matrix.
Bank 9 and 10 are not used for display refresh, the cells can not be addressed.

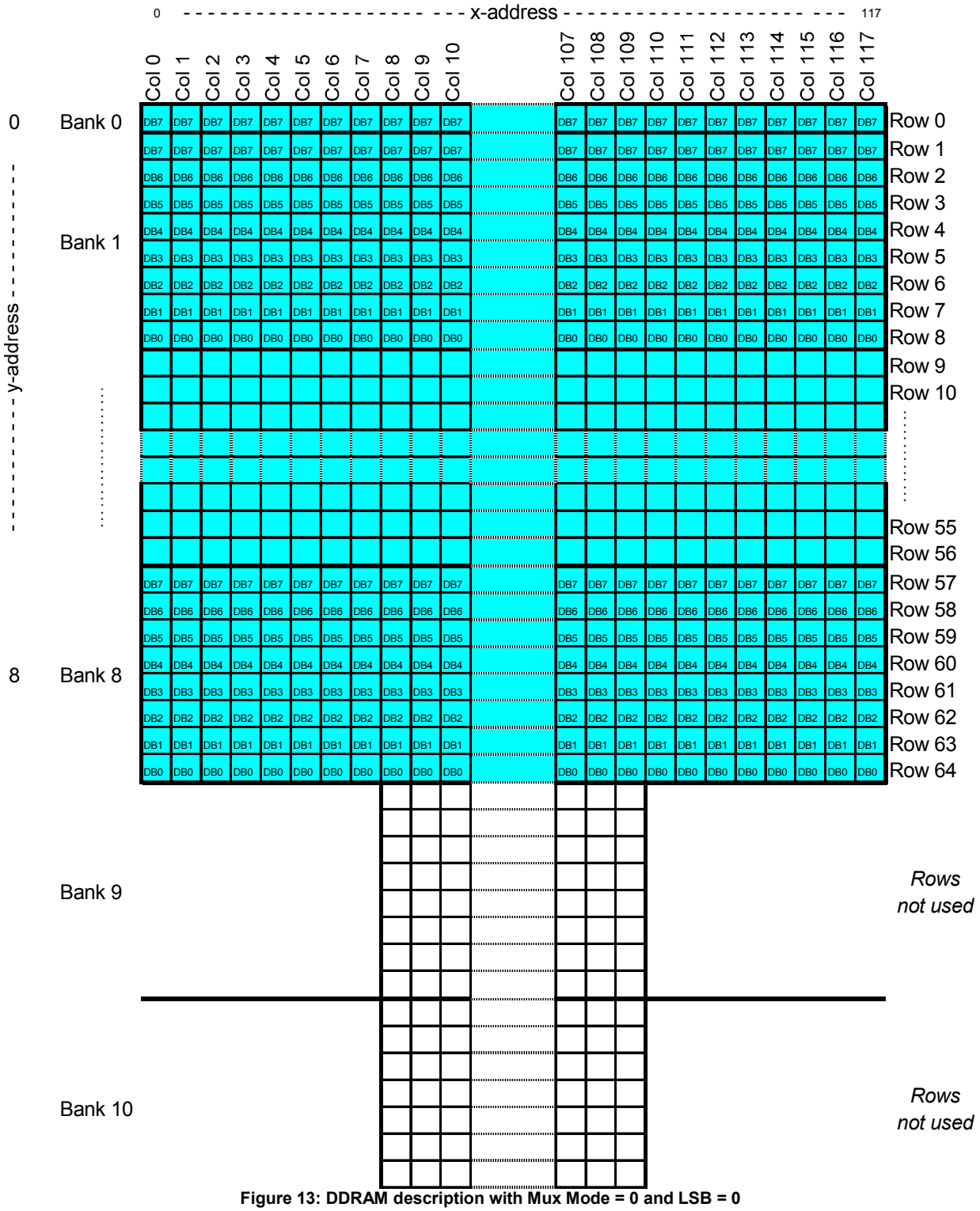


Figure 13: DDRAM description with Mux Mode = 0 and LSB = 0

If Mux Mode = 1, the DDRAM provides a 81 rows and 102 columns matrix.
8 columns on the left + 8 columns on the right are not used for display refresh, the cells can not be addressed.

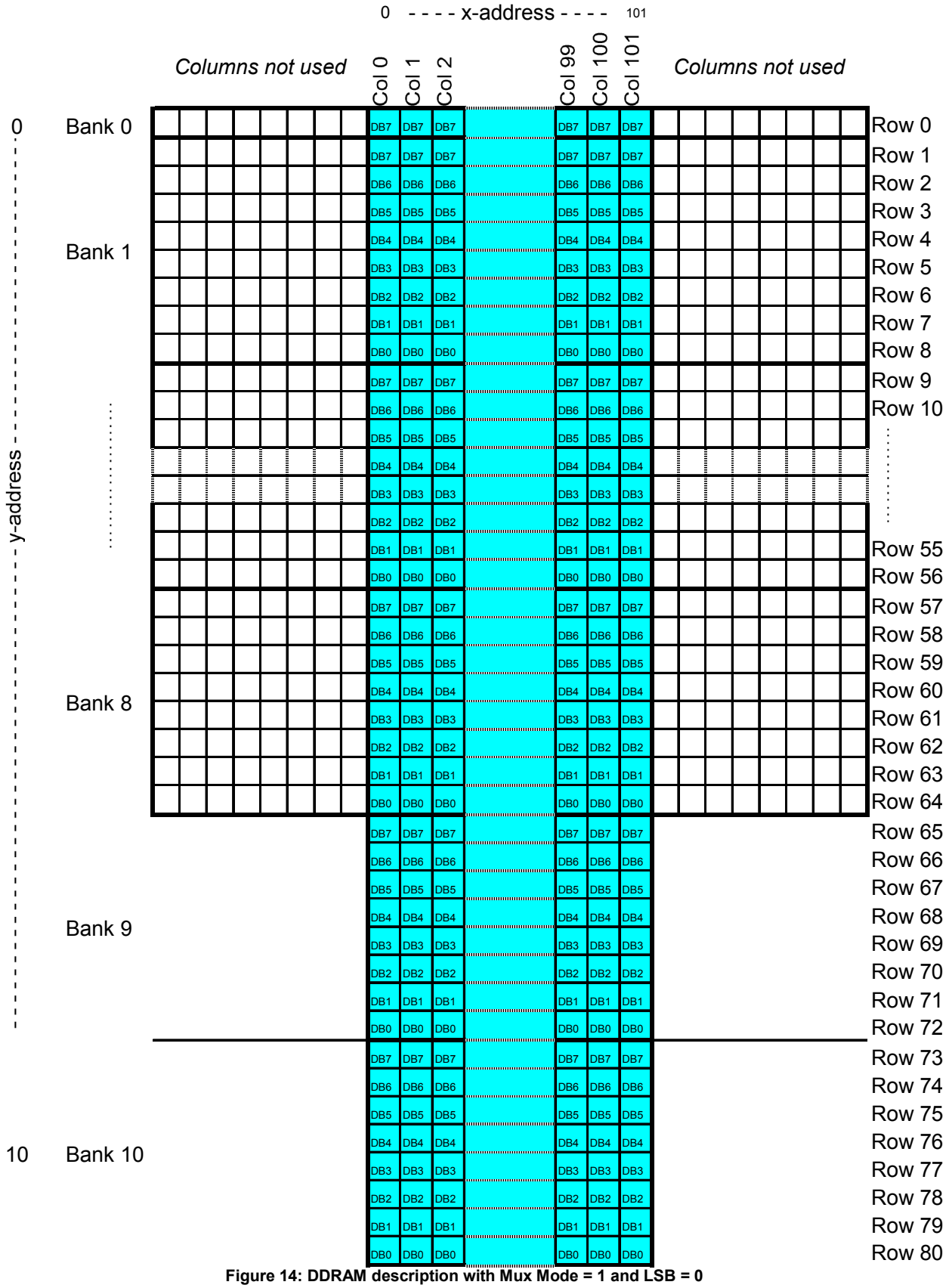


Figure 14: DDRAM description with Mux Mode = 1 and LSB = 0

If Mux Mode = 1 and LSB=1.

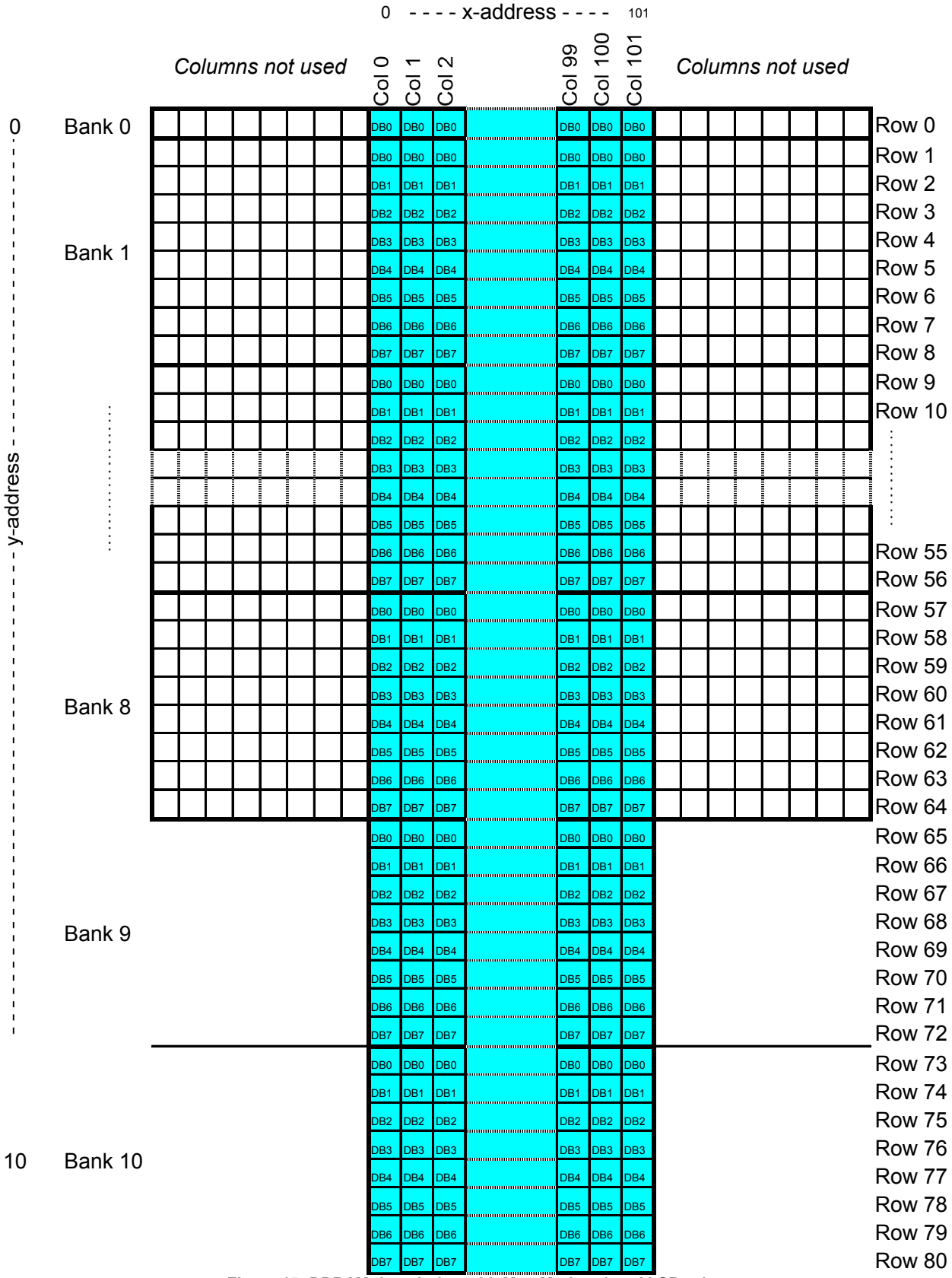


Figure 15: DDRAM description with Mux Mode = 1 and LSB = 1

8.5.2 DDRAM addressing

The x-address and the y-address pointers are used to address RAM cells. They are set by instructions “initialization 1” and “initialization 2”. As EM6125 offers 2 digitally programmable multiplex rates, number of row drivers and number of column drivers are not fixed.

As DDRAM is an image of LCD display, address ranges also depend on multiplex rate (Mux Mode):

- If Mux Mode = 0: $0 \leq$ x-address ≤ 117
  $0 \leq$ y-address ≤ 8
- If Mux Mode = 1: $0 \leq$ x-address ≤ 101
  $0 \leq$ y-address ≤ 10

Addresses outside these ranges are not allowed.

There are three functions that affects the pointers: DEC, V and MX. They are set by instructions “initialization 1” and “initialization 2” (see Table 4: EM6125 instructions).

- Instruction DEC increment or decrement x-address:
  - If DEC = 0, x-address increments after each byte written to the RAM. After the last x-address, x-address wraps around to 0 and y-address increments.
  - If DEC = 1, x-address decrements after each byte written to the RAM. After x-address=0, x-address wraps around to the higher x-address for the select mux mode and y-address increments.

  DEC allows write to the RAM in two ways right and left easily.

- Instruction V horizontal or vertical mode addressing:
  - If V = 0 (horizontal mode addressing), x-address increments or decrements after each byte written to the RAM. After the last x-address, x-address wraps around to 0 or to the higher x-address and y-address increments.
  - If V = 1 (vertical mode addressing), y-address increments after each byte written to the RAM. After the last y-address, y-address wraps around to 0 and x-address increments or decrements.

- Instruction MX mirrored the DDRAM columns:
  - If MX = 0, x-address 0000000b corresponds to DDRAM column 0.
  - If MX = 1, x-address 0000000b corresponds to DDRAM column 117 or 101.

The table below represents the next address select after pointers are in the last allowed address:

Mux Mode	DEC	Last allowed address		Next address	
		x-address	y-address	x-address	y-address
0	0	117	8	0	0
1	0	101	10	0	0
0	1	0	8	117	0
1	1	0	10	101	0

Table 3

The following tables represent the way that the pointers x-address and y-address are working according with the setting of the instructions Mux Mode, V, MX and DEC.

Mux Mode = 0, V = 0, DEC =0, MX = 0:

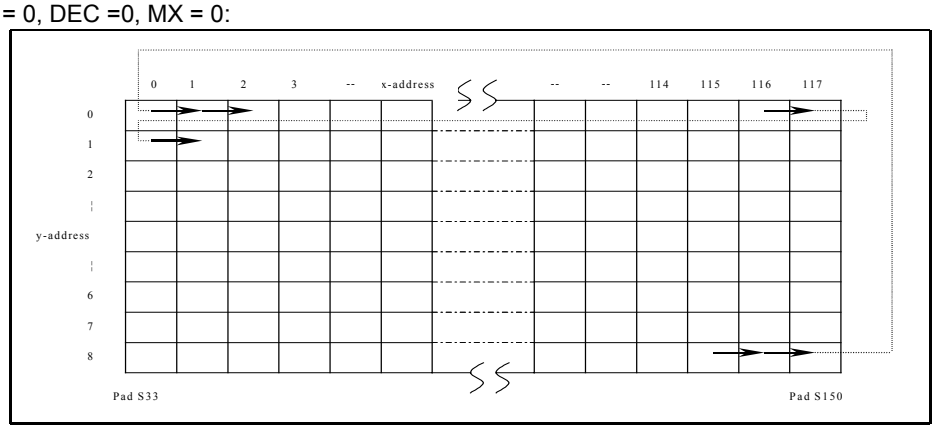


Figure 16

Mux Mode = 0, V = 0, DEC =1, MX = 0:

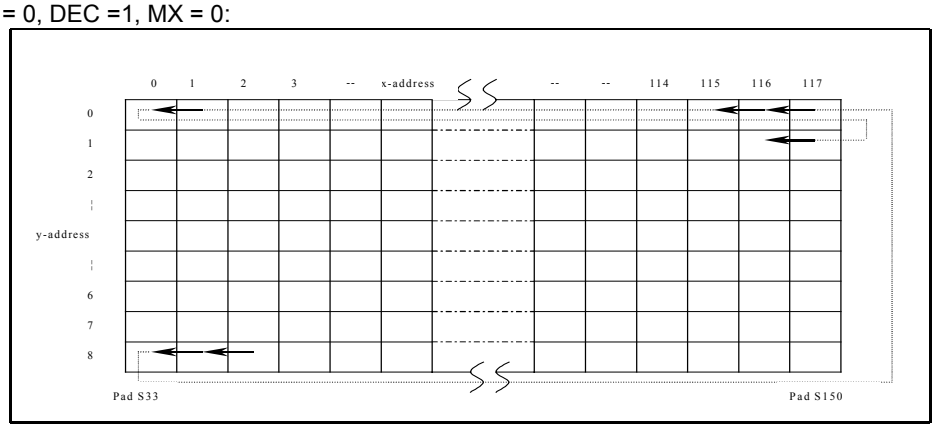


Figure 17

Mux Mode = 1, V = 0, DEC =0, MX = 0:

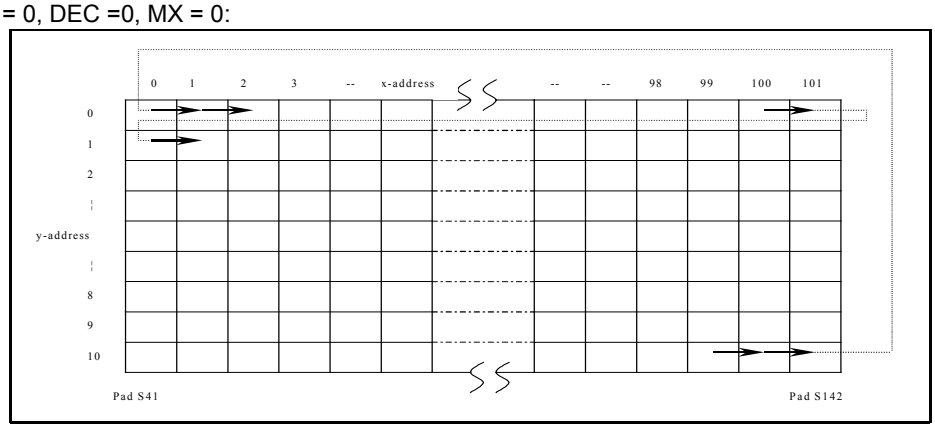


Figure 18

Mux Mode = 1, V = 0, DEC =1, MX = 0:

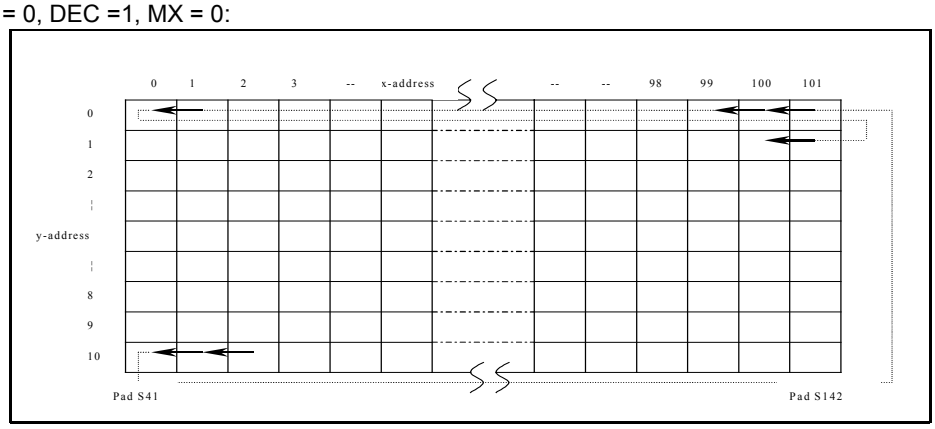


Figure 19

Mux Mode = 0, V = 1, DEC =0,MX = 0:

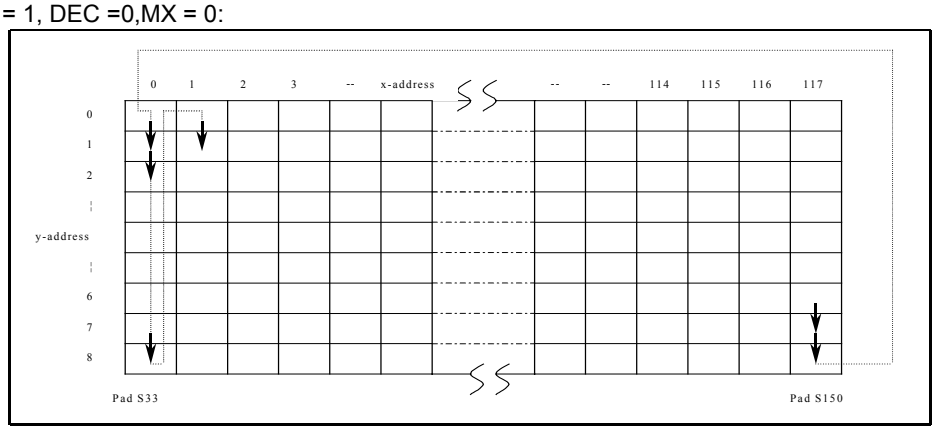


Figure 20

Mux Mode = 0, V = 1, DEC =1,MX = 0:

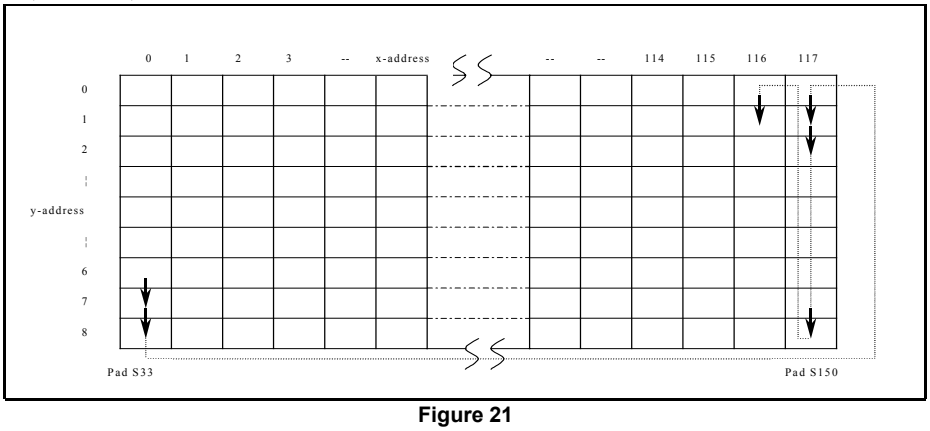


Figure 21

Mux Mode = 1, V = 1, DEC =0, MX = 0:

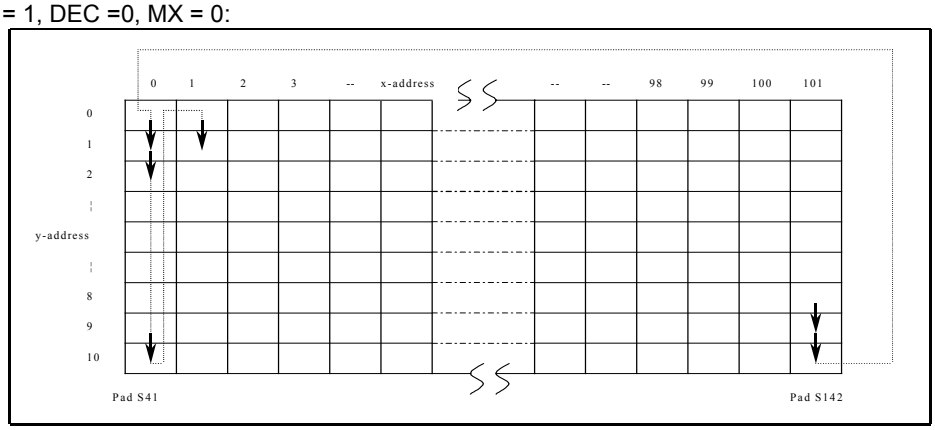


Figure 22

Mux Mode = 1, V = 1, DEC =1, MX = 0:

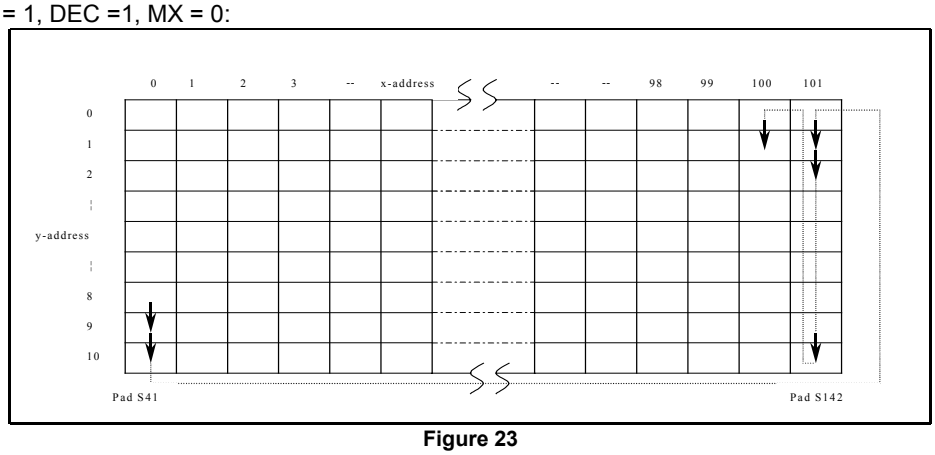


Figure 23

Mux Mode = 0, V = 0, DEC =0, MX = 1:

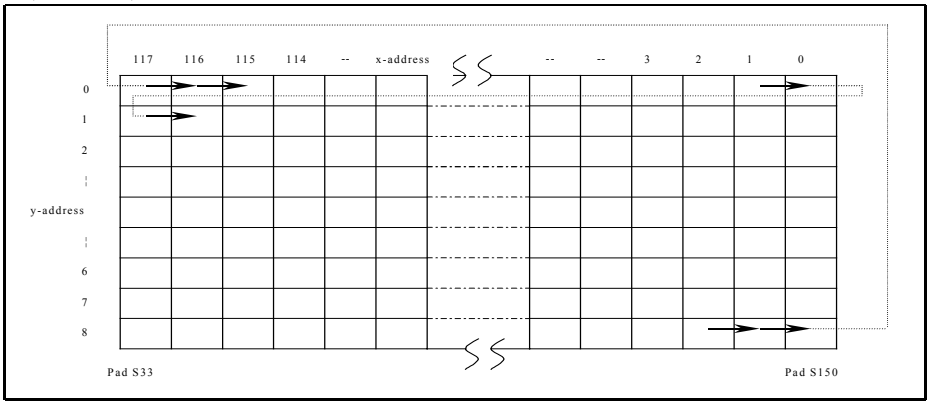


Figure 24

Mux Mode = 0, V = 0, DEC =1, MX = 1:

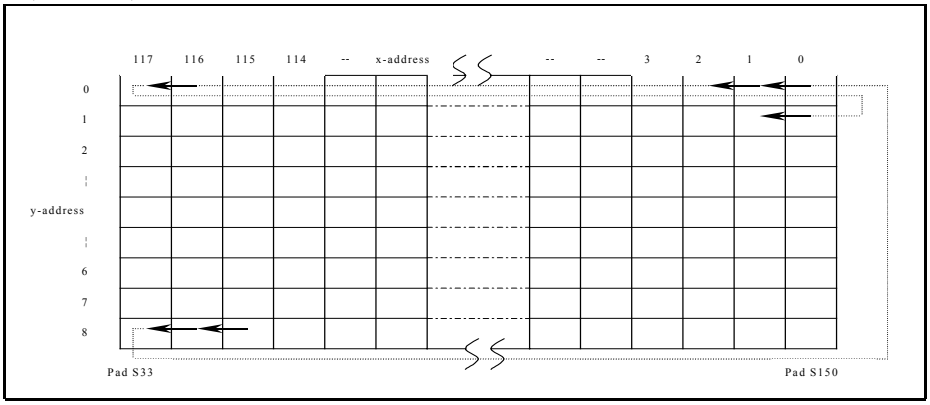


Figure 25

Mux Mode = 1, V = 0, DEC =0, MX = 1:

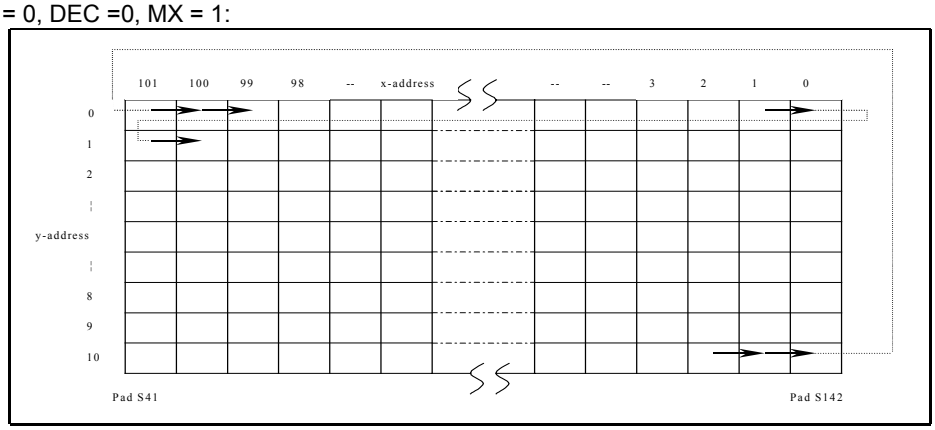


Figure 26

Mux Mode = 1, V = 0, DEC =1, MX = 1:

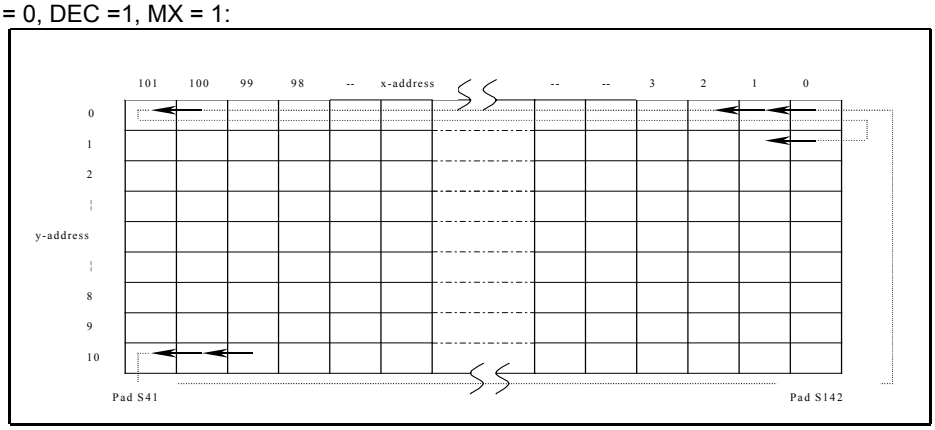


Figure 27

Mux Mode = 0, V = 1, DEC =0,MX = 1:

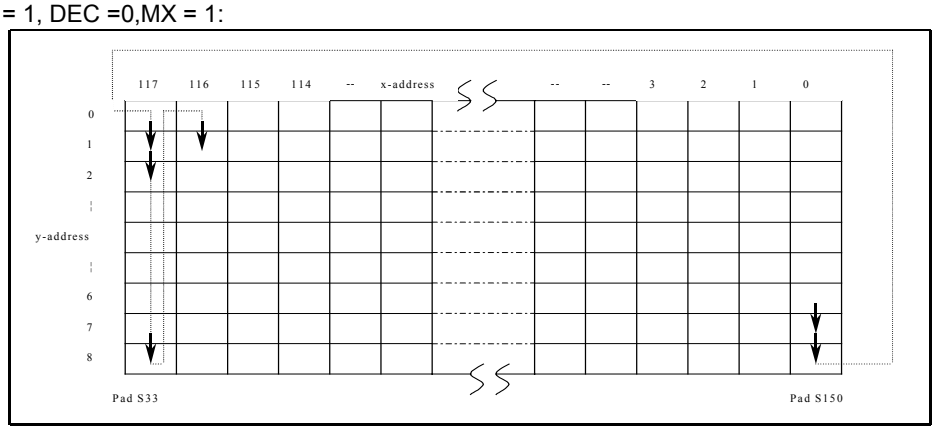


Figure 28

Mux Mode = 0, V = 1, DEC =1,MX = 1:

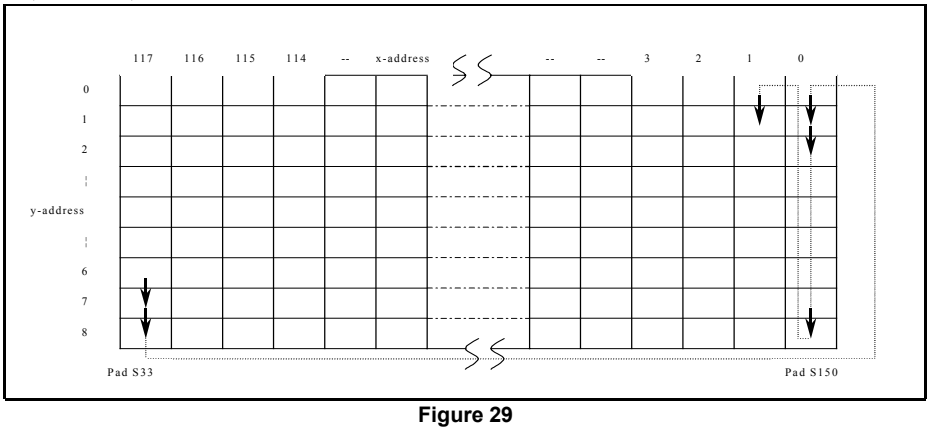


Figure 29

Mux Mode = 1, V = 1, DEC =0, MX = 1:

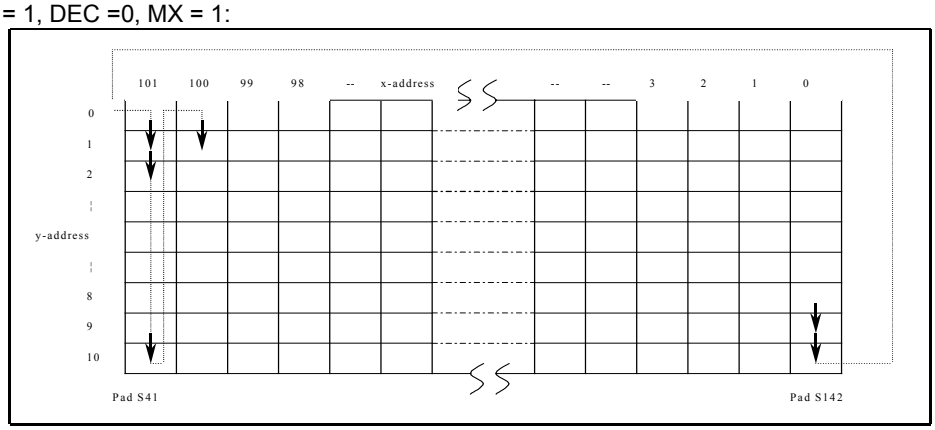


Figure 30

Mux Mode = 1, V = 1, DEC =1, MX = 1:

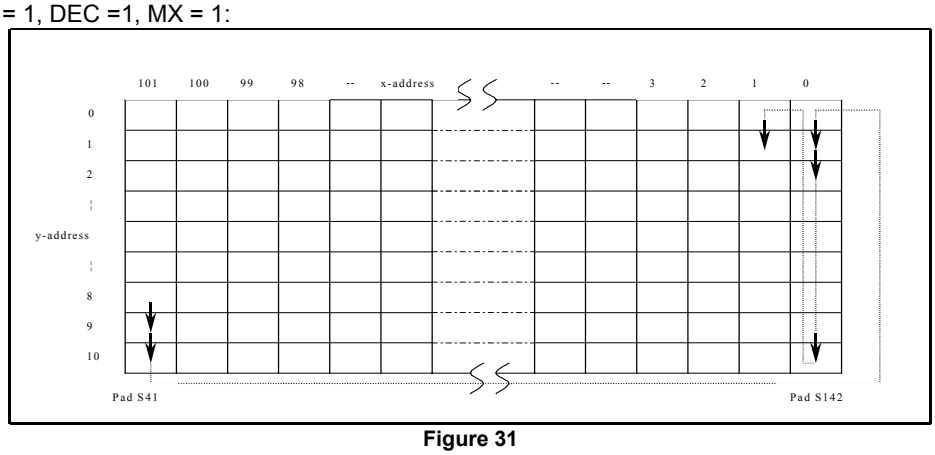


Figure 31

8.6 Initialization of EM6125

Data loaded in EM6125 can be divided in two parts:

- The bits stored in the DDRAM, which are corresponding to LCD pixels.
- The command bits, which are used to set functions of the LCD controller.

The way of addressing these bits is described in table below:

	Instruction	RW	Control Byte								Control Byte								Description
			CO	DC	test[2]	test[1]	test[0]	ini[2]	ini[1]	ini[0]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Initialization of functions	Initialization 0	0	1	0	0	0	0	0	0	0	Mux Mode	TC [1]	TC [0]	Inv. Row	MX	Blank	Checker	Inv. Video	Set functions
	Initialization 1	0	1	0	0	0	0	0	0	1	X[6]	X[5]	X[4]	X[3]	X[2]	X[1]	X[0]	V	Set column adress for DDRAM write access and vertical/horizontal addressing
	Initialization 2	0	1	0	0	0	0	0	1	0	Y[3]	Y[2]	Y[1]	Y[0]	0	Vlcd Dischg	DEC	LSB	Set bank adress for DDRAM write access, increment /decrement pointer and LSB/MSB mode
	Initialization 3	0	1	0	0	0	0	0	1	1	Vlcd Level [7]	Vlcd Level [6]	Vlcd Level [5]	Vlcd Level [4]	Vlcd Level [3]	Vlcd Level [2]	Vlcd Level [1]	Vlcd Level [0]	Programming the internally generated LCD voltage supply V_{LCD}
	Initialization 4	0	1	0	0	0	0	1	0	0	Mult [1]	Mult [0]	Partial Display	First Row PD [3]	First Row PD [2]	First Row PD [1]	First Row PD [0]	Sleep	Number of voltage multiplier stages Partial display parameters Sleep mode
Test	Test 0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	Byte test 0, all bits must be set to 0
	Test 1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	Byte test 1, all bits must be set to 0
	Test 2	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	Byte test 2, all bits must be set to 0
	Test 3	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	Byte test 3, all bits must be set to 0
Write DDRAM	Write 1 byte in DDRAM	0	1/0	1	0	0	0	0	0	0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Write data byte to the Display Data Ram
Read Status	Read 1 byte in initialization	1	-	-	-	-	-	-	-	-	Mux Mode	TC [1]	TC [0]	Inv. Row	MX	Blank	Checker	Inv. Video	Read Status Byte from EM6125 Status Byte = initialization 0 using I^2C interface

Table 4: EM6125 instructions

Bits of instructions from Table 4 and active levels and state after reset:

Bits	0	1	State after reset
Mux Mode	Multiplex rate 65	Multiplex rate 81	0
TC[1:0]	Select V_{LCD} Temperature Coefficient		00b
Inv. Row.	Normal row drivers	Mirrored row drivers	0
MX	Normal column drivers	Mirrored column drivers	0
Blank	Display DDRAM content	LCD blanked (all OFF)	0
Checker	Display DDRAM content	LCD = checker board	0
Inv. Video	LCD = DDRAM	LCD = NOT (DDRAM)	0
X[6:0]	x-address pointer. Selects DDRAM columns to be accessed		0000000b
V	Horizontal addressing	Vertical addressing	0
Y[3:0]	y-address pointer. Selects DDRAM bank to be accessed		0000b
V_{LCD} Dischg	Normal Mode	Discharge Capacitor	0b
DEC	x-address pointer incremented	x-address pointer decrement	0
LSB	DB7 copied to the higher row of the selected bank	DB0 copied to the higher row of the selected bank	0
V_{LCD} Level[7:0]	Program the required LCD supply voltage		00000000b
Mult[1:0]	Number of voltage multiplier stages		00b
Partial Display	Mux Mode multiplex rate	17 LCD rows active only	0
First RowPD[3:0]	Position of first active row when partial display mode		0000b
Sleep	Normal mode	No LCD pixel active, low power consumption	0

Table 5: Internal functions after reset.

8.7 Description of instructions

8.7.1 Initialization 0

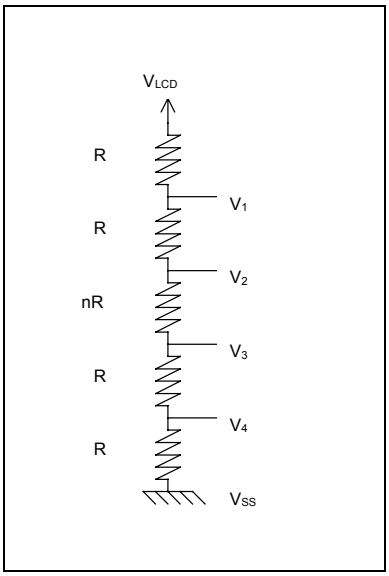
8.7.1.1 Mux Mode

Set the multiplex rate.

Mux Mode	0	1
Multiplex rate (number of row drivers)	65	81
Row drivers	S0 ⟶ S32 S151 ⟶ S182	S0 ⟶ S40 S143 ⟶ S182
Number of column drivers	118	102
Column drivers	S33 ⟶ S150	S41 ⟶ S142
Bias system	1/9	1/10

Table 6

The bias system sets the voltages V_1, V_2, V_3 and V_4 applied to row and column drivers. Assuming these voltages comes from a resistive divider, we have:



The value of the corresponding bias system is:
$V_1 / V_{LCD} = 1/(n+4)$.
It is chosen to optimize the value of the RMS voltage applied to a LCD pixel ON divided by the RMS voltage applied to a LCD pixel OFF: $(V_{ON})_{RMS}/(V_{OFF})_{RMS}$.

This condition leads to:

$$\frac{1}{(n+4)} = \frac{1}{(1+\sqrt{\text{MultiplexRate}})}$$

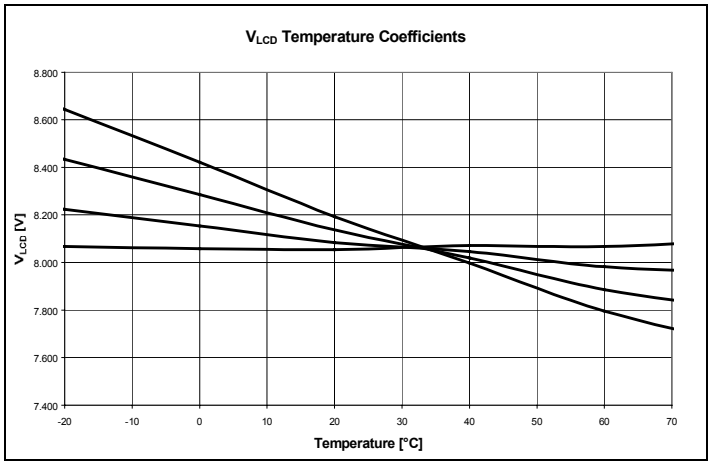
- bias systems ≅ 1/5 for multiplex rate 17 (partial display mode)
- bias systems ≅ 1/9 for multiplex rate 65
- bias systems = 1/10 for multiplex rate 81

8.7.1.2 TC[1:0]

It sets the V_{LCD} temperature compensation.
4 temperature coefficients are available for the internally generated voltage supply V_{LCD}. One of these coefficients is chosen depending one the LCD crystal needs. The temperature coefficient is proportional to V_{LCD}.

TC[1]	TC[0]	V_{LCD} Temperature coefficient (mV/°C)
0	0	0
0	1	-0.39×V_{LCD}
1	0	-0.86×V_{LCD}
1	1	-1.34×V_{LCD}

Table 7



8.7.1.3 Inv. Row

Row driver pads can be mirrored to give more flexibility for LCD interconnects.
This function acts on the row driver that is activated when a given DDRAM row is read: it becomes active with no need of rewriting the RAM (see Table 8 and Figure 34: LCD output pads configuration depending on Mux Mode, Inv. Row and MX).

Read data when Inv. Row=0:

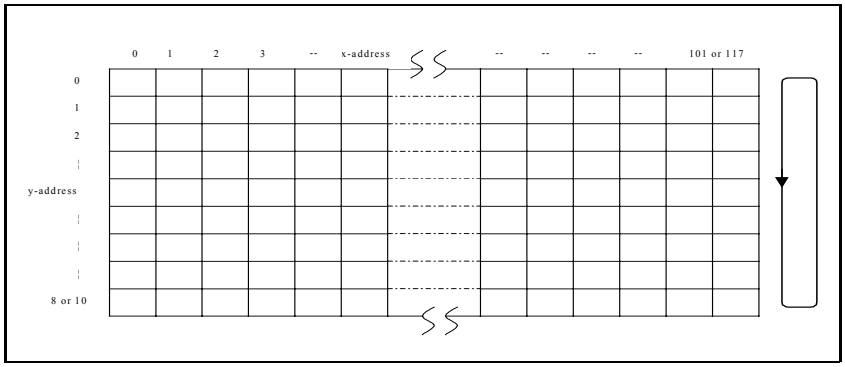


Figure 32

Read data when Inv. Row=1:

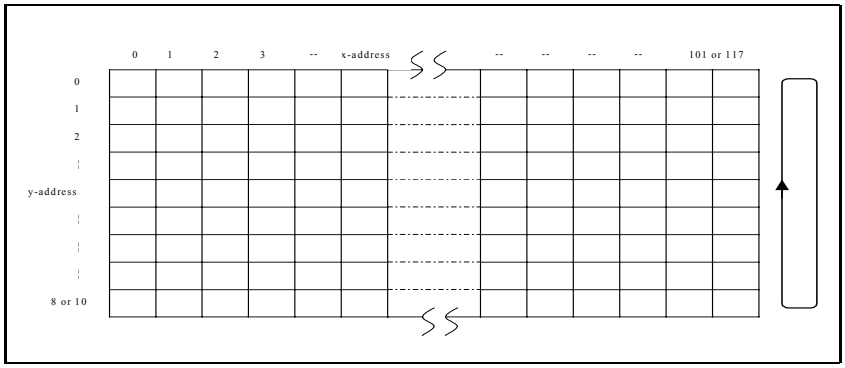


Figure 33

	Inv. Row	0	1	0	1
	Mux Mode	0	0	1	1
Pad name	S0	Row 0	Row 64	Row 0	Row 80
	S1	Row 1	Row 63	Row 1	Row 79
	⋮	⋮	⋮	⋮	⋮
	S32	Row 32	Row 32	Row 32	Row 48
	S33	x-addreess = 0		Row 33	Row 47
	S34	x-addreess = 1		Row 34	Row 46
	S35	x-addreess = 2		Row 35	Row 45
	S36	x-addreess = 3		Row 36	Row 44
	S37	x-addreess = 4		Row 37	Row 43
	S38	x-addreess = 5		Row 38	Row 42
	S39	x-addreess = 6		Row 39	Row 41
	S40	x-addreess = 7		Row 40	Row 40
	S41 to S142	x-addreess = 8 to x-addreess = 109		x-addreess = 0 to x-addreess = 101	
	S143	x-addreess = 110		Row 80	Row 0
	S144	x-addreess = 111		Row 79	Row 1
	S145	x-addreess = 112		Row 78	Row 2
	S146	x-addreess = 113		Row 77	Row 3
	S147	x-addreess = 114		Row 76	Row 4
	S148	x-addreess = 115		Row 75	Row 5
	S149	x-addreess = 116		Row 74	Row 6
	S150	x-addreess = 117		Row 73	Row 7
	S151	Row 64	Row 0	Row 72	Row 8
	S152	Row 63	Row 1	Row 71	Row 9
	⋮	⋮	⋮	⋮	⋮
	S182	Row 33	Row 31	Row 41	Row 39
	S183 = S0	Row 0	Row 64	Row 0	Row 80

Table 8

8.7.1.4 MX

Column driver pads can also be mirrored to give more flexibility for LCD interconnects.

This function change the x-address pointer to reverse columns of the DDRAM accessed during a write cycle: a rewrite cycle is required to observe changes on outputs (see Figure 34: LCD output pads configuration depending on Mux Mode, Inv. Row and MX)

Table 9 shows how the DDRAM is connected to LCD output pads, depending on bits Mux Mode, MX and Inv. Row.

	MX	0	1	0	1
	Mux Mode	0	0	1	1
Pad name	S0	Row 0		Row 0	
	⋮	⋮		⋮	
	S32	Row 32		Row 32	
	S33	x-address = 0	x-address = 117	Row 33	
	S34	x-address = 1	x-address = 116	Row 34	
	S35	x-address = 2	x-address = 115	Row 35	
	S36	x-address = 3	x-address = 114	Row 36	
	S37	x-address = 4	x-address = 113	Row 37	
	S38	x-address = 5	x-address = 112	Row 38	
	S39	x-address = 6	x-address = 111	Row 39	
	S40	x-address = 7	x-address = 110	Row 40	
	S41	x-address = 8	x-address = 109	x-address = 0	x-address = 101
	S42	x-address = 9	x-address = 108	x-address = 1	x-address = 100
	S43	x-address = 10	x-address = 107	x-address = 2	x-address = 99
	S44 to S139	x-address =11 to x-address =106	x-address =106 to x-address =11	x-address =3 to x-address = 98	x-address = 98 to x-address = 3
	S140	x-address = 107	x-address = 10	x-address = 99	x-address = 2
	S141	x-address = 108	x-address = 9	x-address = 100	x-address = 1
	S142	x-address = 109	x-address = 8	x-address = 101	x-address = 0
	S143	x-address = 110	x-address = 7	Row 80	
	S144	x-address = 111	x-address = 6	Row 79	
	S145	x-address = 112	x-address = 5	Row 78	
	S146	x-address = 113	x-address = 4	Row 77	
	S147	x-address = 114	x-address = 3	Row 76	
	S148	x-address = 115	x-address = 2	Row 75	
	S149	x-address = 116	x-address = 1	Row 74	
	S150	x-address = 117	x-address = 0	Row 73	
	S151	Row 64		Row 72	
	⋮	⋮		⋮	
	S182	Row 33		Row 41	
	S183 = S0	Row 0		Row 0	

Table 9: Relation between LCD output pads and row and columns of DDRAM

The combination of Mux Mode, Inv. Row and MX gives the following figures (next page) of output pads.

8.7.1.5 Blank

Sets all the LCD pixels OFF.

Every row drivers and column drivers are at V_{SS} level.

DDRAM content is not affected by this instruction.

8.7.1.6 Checker

Sets all the LCD pixels in a checker mode, LCD displays alternately ON and OFF pixels.

DDRAM content is not affected by this instruction.

8.7.1.7 Inv. Video

Sets an inverse video mode.

- If Inv. Video = 0, a logical 1 level stored in the DDRAM leads to a “ON” pixel displayed the LCD.
- If Inv. Video = 1, a logical 1 level stored in the DDRAM leads to a “OFF” pixel displayed the LCD.

DDRAM content is not affected by this instruction.

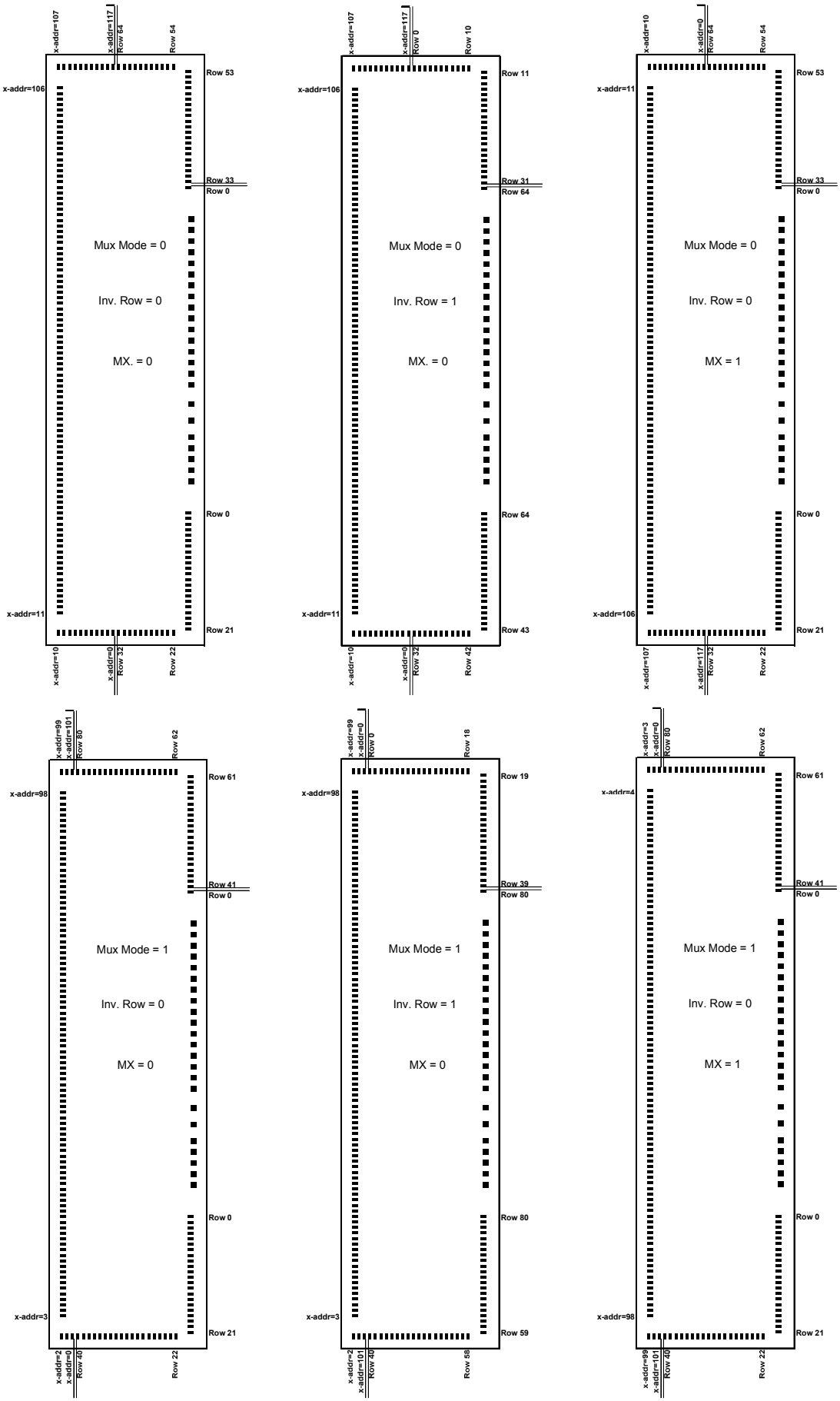


Figure 34: LCD output pads configuration depending on Mux Mode, Inv. Row and MX

8.7.2 Initialization 1

8.7.2.1 X[6:0]

These 7 bits set the x-address pointer of the DDRAM.

Data are written in column “x-address” with: X[6] = MSB, X[0] = LSB.

As the number of column drivers depends on the chosen multiplex rate, the DDRAM x-address pointer should also satisfy the following relationships:

- If Mux Mode = 0 then 0 ≤ x-address ≤ 1110101b. (117).
- If Mux Mode = 1 then 0 ≤ x-address ≤ 1100101b. (101).

8.7.2.2 V

Vertical addressing:

- If V = 0, DDRAM x-address pointer is incremented or decrement after each data byte send.
- If V = 1, DDRAM y-address pointer is incremented or decrement after each data byte send.

8.7.3 Initialization 2

8.7.3.1 Y[3:0]

These 4 bits set the y-address pointer of the DDRAM.

Data are written in bank “y-address” with Y[3]= MSB, Y[0]= LSB.

As the multiplex rate is digitally programmable, the DDRAM y-address pointer should also satisfy the following relationships:

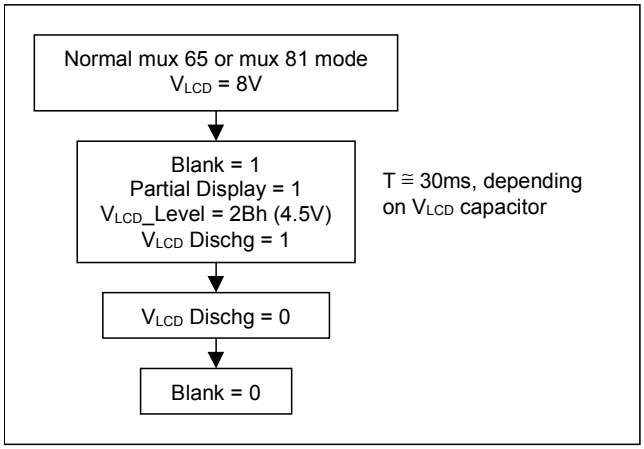
- If Mux Mode = 0 then 0 ≤ y-address ≤ 1000b.
- If Mux Mode = 1 then 0 ≤ y-address ≤ 1010b.

8.7.3.2 Vlcd Dischg.

V_{LCD} Discharge works to discharge the capacitor connected to PAD V_{LCD}. This operation becomes necessary when programming Partial Display Mode. In this case, a lower V_{LCD} is required than the voltage used for normal mux 65 or 81 operation, the display at beginning of partial mode operation could be completely ‘ON’ until V_{LCD} is low enough.

To avoid this, an internal pull down helps the V_{LCD} voltage to come down and hence reach the new optimum value in a short time. This pull down is on until bit *‘Vlcd Dischg’* is at 1L.

Typical use of *‘Vlcd Dischg’* command:



Using this command with external power supply on V_{LCD} can damage the IC.

8.7.3.3 DEC

H controls the DDRAM writing direction:

- If DEC = 0 then x-address pointer increments after each byte written to the DDRAM.
- If DEC = 1 then x-address pointer decrements after each byte written to the DDRAM.

8.7.3.4 LSB

This instruction change the bytes send to the DDRAM before writing them. For instance, for bank 1 we have:

- If LSB = 0 then DB7 is written on Row 1.
- If LSB = 1 then DB0 is written on Row 1 (see Figure 14 and Figure 15).

8.7.4 Initialization 3

8.7.4.1 Vlcd Level[7:0]

Set the internally generated voltage level.

These 8 bits generate integer “V_{LCD} Level”, V_{LCD} Level [7] = MSB, V_{LCD} Level [0] = LSB.

V_{LCD} is given by the following formula:

$$V_{LCD} = 3.02 + 0.0352 \times V_{LCD}\_Level$$

8.7.5 Initialization 4

8.7.5.1 Mult[1:0]

Set the internal voltage multiplier factor.

These bits should be chosen depending on the V_{HV} supply voltage level, the desired V_{LCD} voltage and the current consumption due to LCD load.

If low V_{LCD} is required, for instance when partial display mode is enabled, lower voltage multiplier range can be used, leading in current consumption reduction (improved voltage multiplier efficiency).

Mult1	Mult0	Voltage multiplier
0	0	$\times 2$
0	1	$\times 3$
1	0	$\times 4$
1	1	$\times 5$

Table 10

8.7.5.2 Partial Display

Set the partial display configuration of the driver (multiplex ratio 17).

In this configuration, 17 rows only are active:

- The row which corresponds to RAM address 0.
- 16 other rows, first one is defined by First Row PD [3:0].

Partial Display	Multiplex rate
0	65 or 81 (depending on Mux Mode)
1	17

Table 11

8.7.5.3 First Row PD[3:0]

Partial display mode yields to a LCD with 2 banks activated only.

Row 0 is always active, it could be used to drive icons.

The 16 other active rows are chosen from 64 or 80 row as shown on table:

Mux Mode	*First Row PD[3]*	*First Row PD[2]*	*First Row PD[1]*	*First Row PD[0]*	First active row (DDRAM)	Last active row (DDRAM)	Activated banks
0 or 1	0	0	0	0	Row 1	Row 16	0,1,2
	0	0	0	1	Row 9	Row 24	0,2,3
	0	0	1	0	Row 17	Row 32	0,3,4
	0	0	1	1	Row 25	Row 40	0,4,5
	0	1	0	0	Row 33	Row 48	0,5,6
	0	1	0	1	Row 41	Row 56	0,6,7
	0	1	1	0	Row 49	Row 64	0,7,8
1	0	1	1	1	Row 57	Row 72	0,8,9
	1	0	0	0	Row 65	Row 80	0,9,10

Table 12

- If Mux Mode = 0, 0 ≤ First_Row PD [3:0] ≤ 0110b.
- If Mux Mode = 1, 0 ≤ First_Row PD [3:0] ≤ 1000b.

Values for “First_Row PD [3:0]” outside these ranges are not allowed.

8.7.5.4 Sleep

This function stops all functionality, internal oscillator and voltage multiplier are off, and LCD is blanked. It yields to a very low current consumption with leakage currents only.

8.7.6 Test 0 to 3

All bits must be set to 0 (see example in typical application page 35).

8.8 LCD outputs

The LCD output pads are connected to LCD electrodes, signals and voltages are optimized for the best LCD contrast and a null DC component of voltage applied to LCD pixels. Table 13 gives bias voltages referring to V_{LCD}.

Multiplex Rate	V_{LCD}	V_1	V_2	V_3	V_4	V_{SS}
n	1	$1-\left(\frac{1}{\sqrt{n}+1}\right)$	$1-\left(\frac{2}{\sqrt{n}+1}\right)$	$\frac{2}{\sqrt{n}+1}$	$\frac{1}{\sqrt{n}+1}$	0
81 (Mux Mode = 1)	1	0.90	0.80	0.20	0.10	0
65 (Mux Mode = 0)	1	0.89	0.78	0.22	0.11	0
17 (Partial Display = 1)	1	0.80	0.60	0.40	0.20	0

Table 13: Values of intermediate bias voltages

Table 14 gives values of V_{LCD} in reference to RMS voltage applied to a pixel OFF and the contrast achieved between a ON pixel and a OFF pixel. These values correspond to bias voltages described on Table 13.

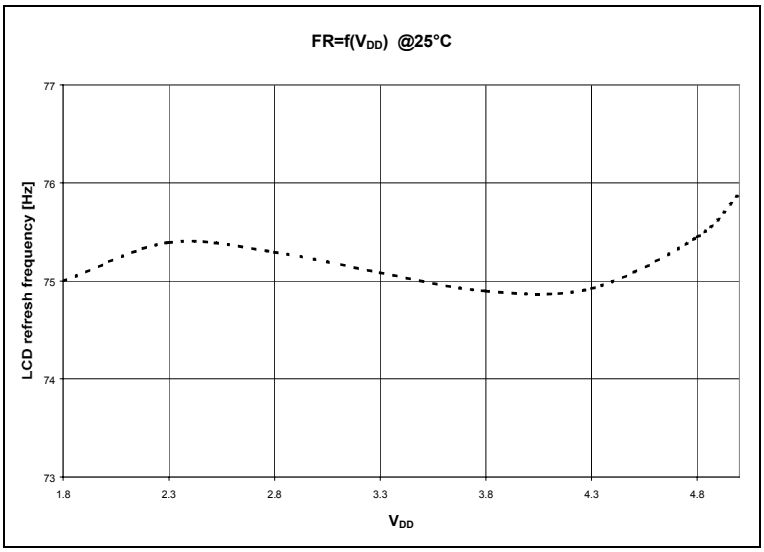
Programmed multiplex rate	LCD Bias configuration	$\frac{V_{LCD}}{V_{OFF}(RMS)}$	$\frac{V_{ON}(RMS)}{V_{OFF}(RMS)}$
81	6 levels	$\sqrt{\frac{\sqrt{n}(\sqrt{n}+1)^2}{2(\sqrt{n}-1)}}=7.500$	$\sqrt{\frac{\sqrt{n}+1}{\sqrt{n}-1}}=1.118$
65	6 levels	$\sqrt{\frac{\sqrt{n}(\sqrt{n}+1)^2}{2(\sqrt{n}-1)}}=6.847$	$\sqrt{\frac{\sqrt{n}+1}{\sqrt{n}-1}}=1.133$
17	6 levels	$\sqrt{\frac{\sqrt{n}(\sqrt{n}+1)^2}{2(\sqrt{n}-1)}}=4.162$	$\sqrt{\frac{\sqrt{n}+1}{\sqrt{n}-1}}=1.281$

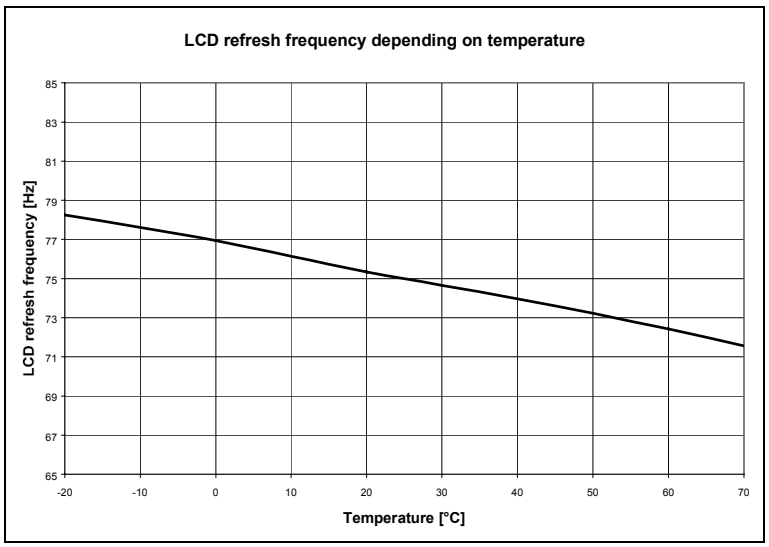
Table 14: Required LCD supply voltage and achieved LCD contrast

The chosen LCD gives the value of $V_{OFF}(RMS)$ and the value of $\frac{V_{LCD}}{V_{OFF}(RMS)}$ gives the required V_{LCD} voltage supply. We can observe that the Partial Display mode decreases V_{LCD}, leading to lower power consumption. Current consumption is also decreased because lower V_{LCD} leads to choose fewer stages for voltage multiplier and the efficiency is improved.

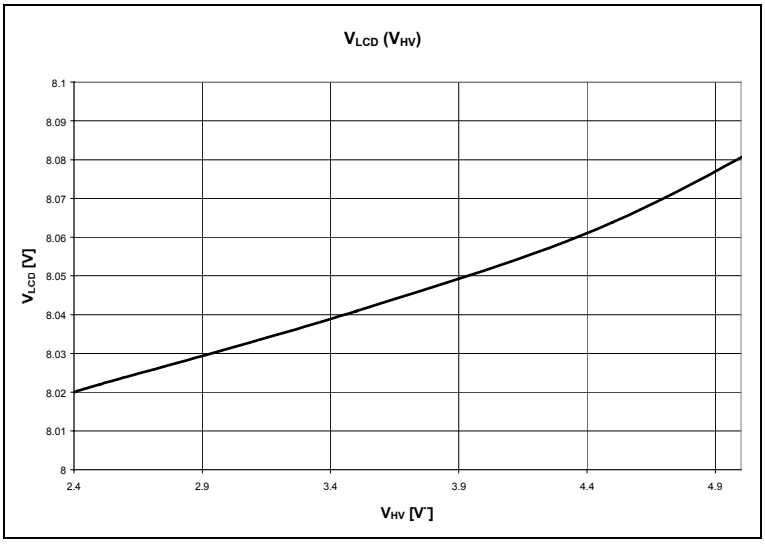
8.9 LCD refresh frequency

LCD refresh frequency depends on an internal RC oscillator. Pad FR outputs this frequency multiplied by the multiplex rate. Following figures display typical variations depending on V_{DD} power supply and temperature.





8.10 V_{LCD} depending on V_{HV}



8.11 LCD driver waveforms

Row and Column Multiplexing Waveform EM6125 (81)

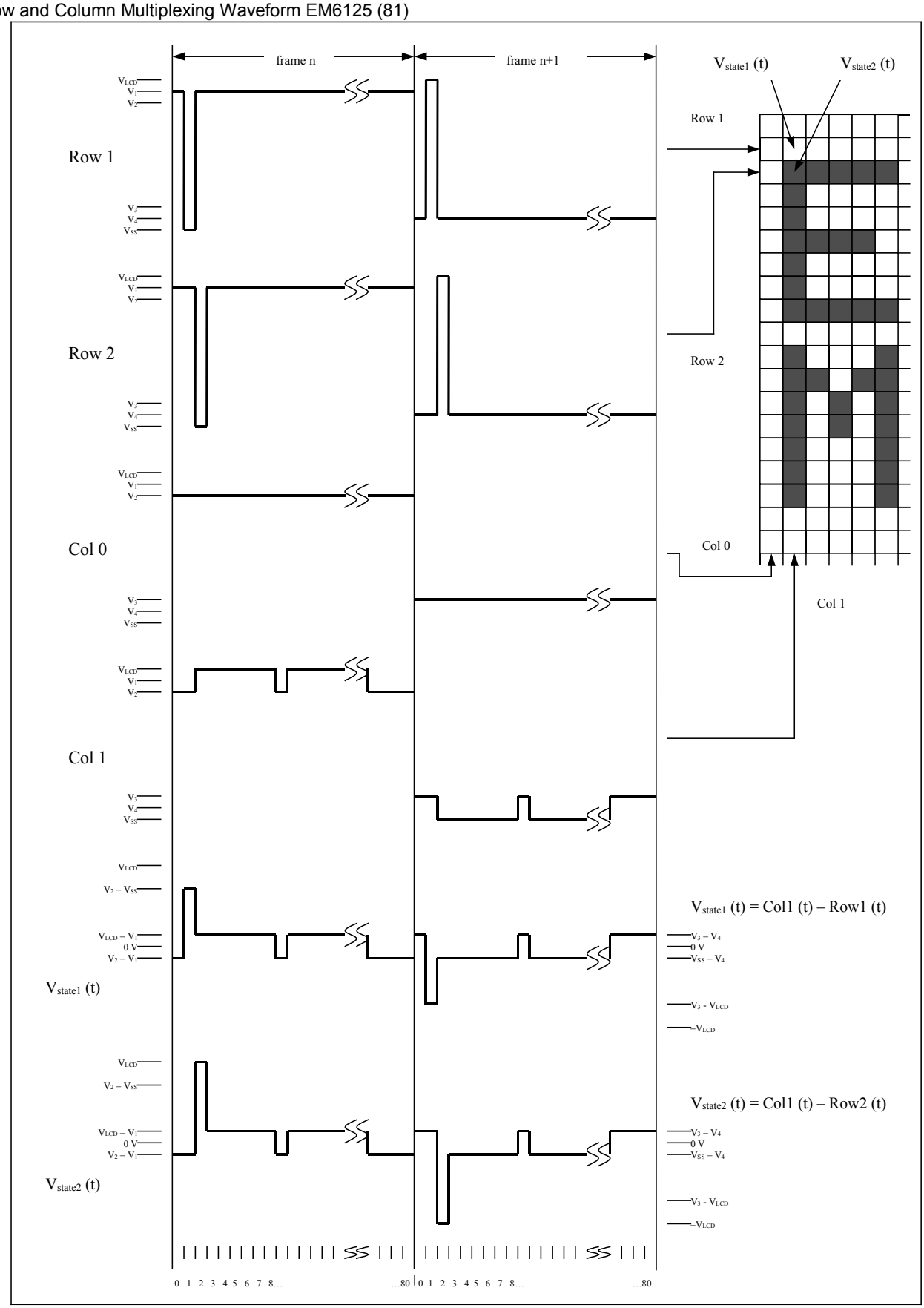


Figure 35

Row and Column Multiplexing Waveform EM6125 (65)

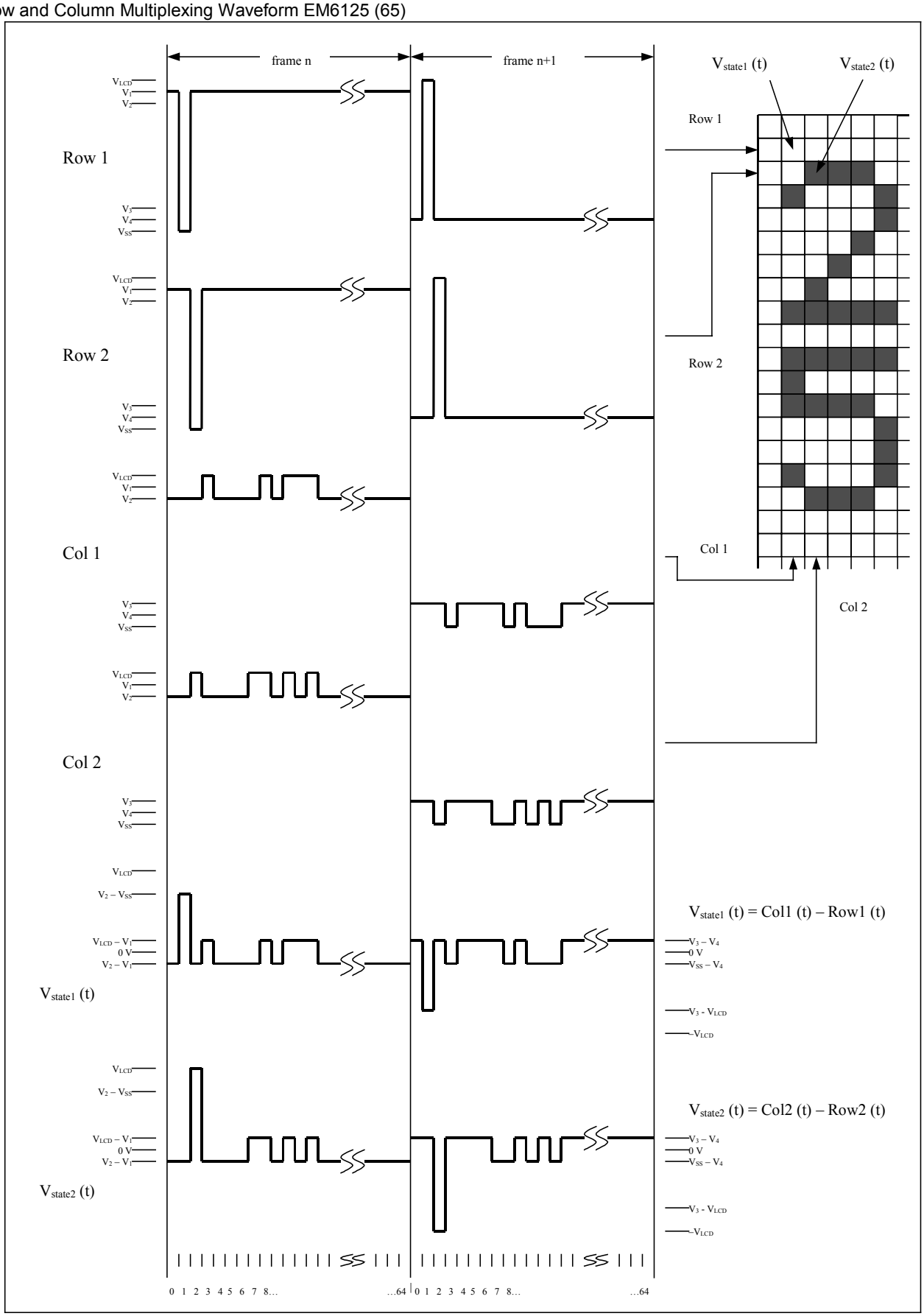


Figure 36

8.11.1 Partial Display

Row and Column Multiplexing Waveform EM6125 (17)

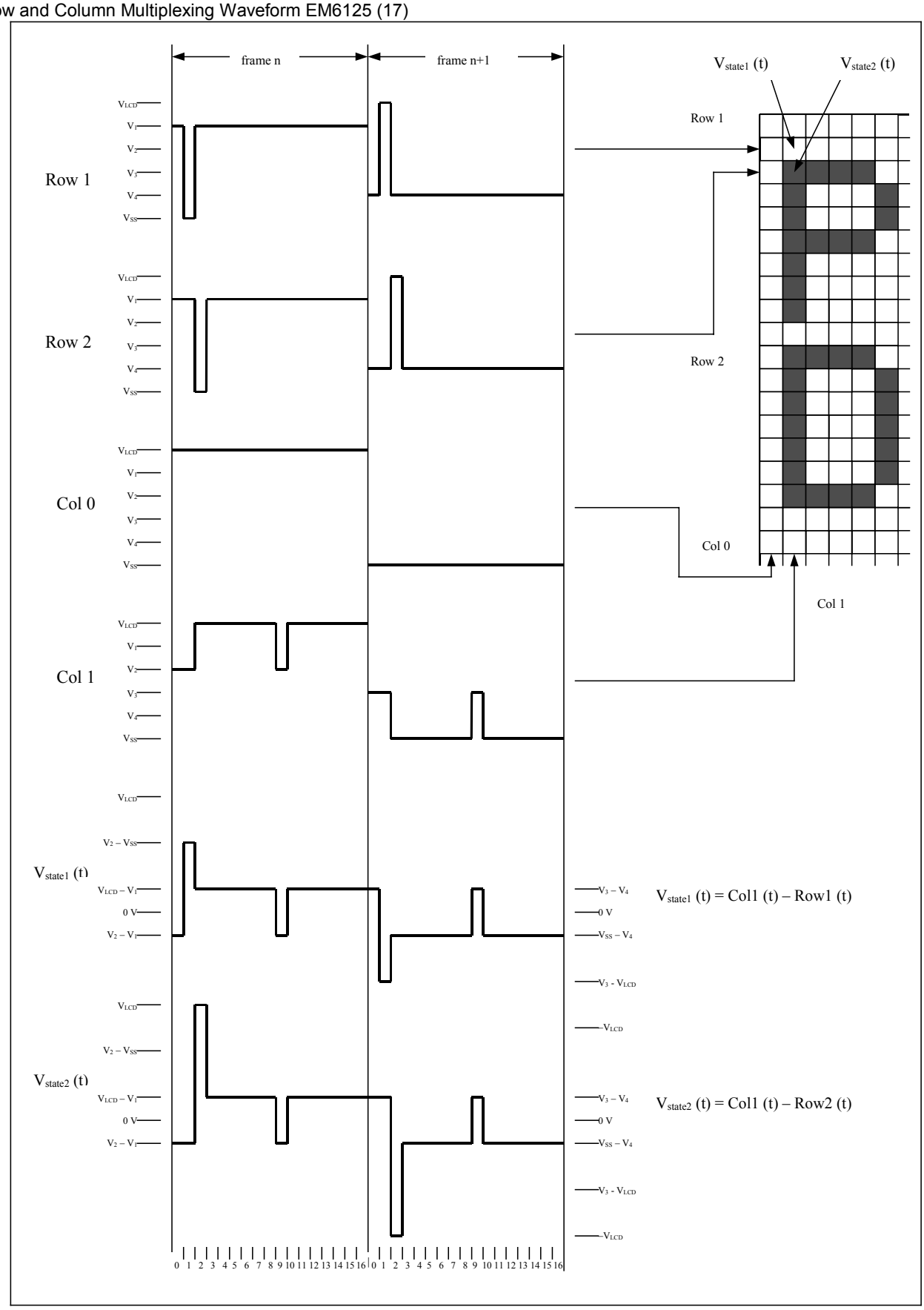


Figure 37

9 Typical Application

This example gives typical programming steps for EM6125 with I²C interface, for serial interface, start and stop conditions should be replaced by CS at 0L and CS at 1L. LCD display is connected as described on Figure 38:

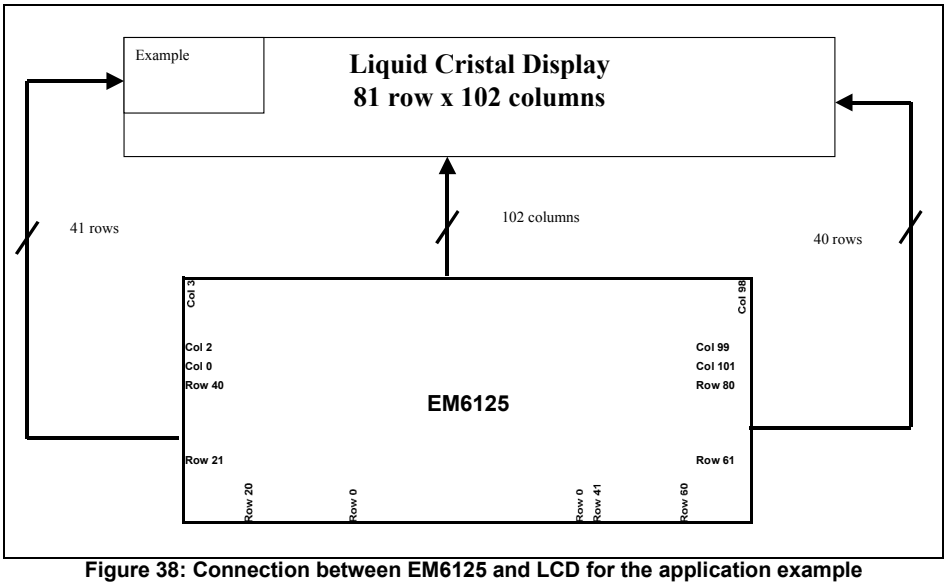
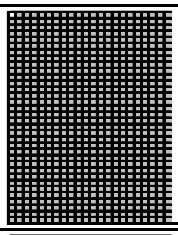
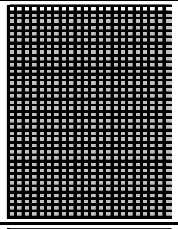
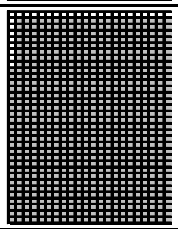
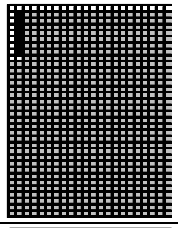
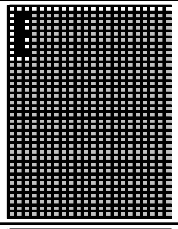
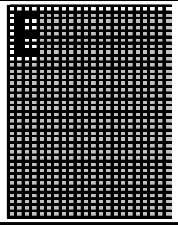
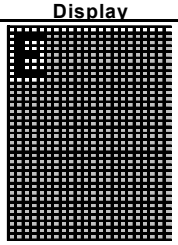
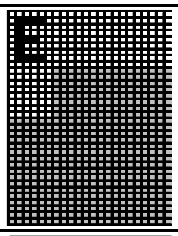
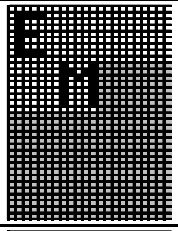
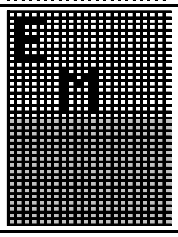
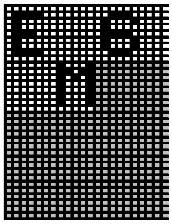
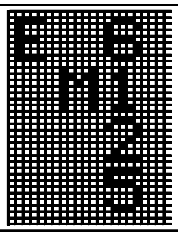
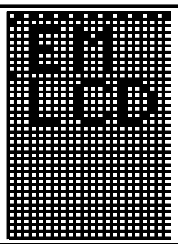
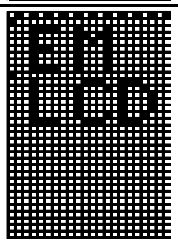
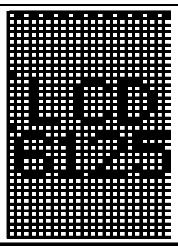


Figure 38: Connection between EM6125 and LCD for the application example

Step	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Comment	Display
1	Power on									Undefined
2	Reset								A reset cycle must always follow the power on	Blank
3	I2C start condition									Blank
4	x	x	x	x	x	x	x	0	EM6125 slave address + write mode	Blank
5	1	0	0	0	0	0	0	0	Control byte for initialization 0	Blank
6	1	0	1	0	0	0	0	0	**Data byte = initialization 0** Multiplex Rate = 81 Vlcd Temperature Coefficient = -0.39 x Vlcd (mV/°C) No row or column mirroring No blank, Checker or Video functions.	Blank
7	1	0	0	0	0	0	1	1	Control byte for initialization 3	Blank
8	1	0	0	0	1	1	1	0	**Data byte = initialization 3** Programmed Vlcd_level = 10001110b (8Eh=142) Vlcd = 3.02 + 142*0.0352 = 8.02V	Blank
9	1	0	0	0	0	1	0	0	Control byte for initialization 4	Blank
10	1	1	0	0	0	0	0	0	**Data byte = initialization 4** x 5 Voltage Multiplier No partial display mode. No sleep mode	Undefined
11	1	0	1	0	0	0	0	0	Control byte for test 0	Undefined
12	0	0	0	0	0	0	0	0	bits test must be set to 0L	
13	1	0	1	0	1	0	0	0	Control byte for test 1	
14	0	0	0	0	0	0	0	0	bits test must be set to 0L	
15	1	0	1	1	0	0	0	0	Control byte for test 2	
16	0	0	0	0	0	0	0	0	bits test must be set to 0L	
17	1	0	1	1	1	0	0	0	Control byte for test 3	
18	0	0	0	0	0	0	0	0	bits test must be set to 0L	

Step	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Comment	Display
19	0	1	0	0	0	0	0	0	Last control byte DDRAM write selected Fisrt DDRAM byte stored at x-address = 0, y-address = 0 Horizontal addressing is selected (state after reset)	Undefined
20	0	x	x	x	x	x	x	x	Only DB7 is stored at row 0 of DDRAM, column 0	
21 to 121	0	x	x	x	x	x	x	x	Only DB7 is stored at row 0, columns 1 to 101	
122	0	0	0	0	0	0	0	0	DB7 to DB0 are stored at column 0, rows 1 to 8	
123	1	1	1	1	1	1	1	0	DB7 to DB0 are stored at column 1, rows 1 to 8	
124	1	0	0	1	0	0	1	0	DB7 to DB0 are stored at column 2, rows 1 to 8	
125	1	0	0	1	0	0	1	0	DB7 to DB0 are stored at column 3, rows 1 to 8	

Step	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Comment	Display
126	1	0	0	0	0	0	1	0	DB7 to DB0 are stored at column 4, rows 1 to 8	
127 to 229	0	0	0	0	0	0	0	0	DB7 to DB0 are stored at column 5 to 101, rows 1 to 8 column 0 to 5, rows 9 to 16	
230	0	0	0	0	0	0	0	0	Write letter M	
231	1	1	1	1	1	1	1	0		
232	0	1	0	0	0	0	0	0		
233	0	0	1	0	0	0	0	0		
234	0	1	0	0	0	0	0	0		
235	1	1	1	1	1	1	1	0		
236 to 325	0	0	0	0	0	0	0	0	DB7 to DB0 are stored at column 12 to 101, rows 9 to 16	
326	I2C stop condition + new start condition									Unchanged
327	x	x	x	x	x	x	x	0	EM6125 slave address + write mode	Unchanged
328	1	0	0	0	0	0	0	1	Control byte for initialization 1	Unchanged
329	0	0	0	1	1	0	0	0	x-address = 12 , Horizontal mode addressing	Unchanged
330	1	0	0	0	0	0	1	0	Control byte for initialization 2	Unchanged
331	0	0	0	1	0	0	0	0	y-address = 1	Unchanged
332	0	0	0	0	0	0	0	0	Write 6	
333	0	1	1	1	1	1	0	0		
334	1	0	0	1	0	0	1	0		
335	1	0	0	1	0	0	1	0		
336	1	0	0	1	0	0	1	0		
337	0	1	0	0	1	1	0	0		
338	x	x	x	x	x	x	x	x	Continuation…	

Step	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Comment	Display
1	I2C start condition									Previously set
2	x	x	x	x	x	x	x	0	EM6125 slave address + write mode	Unchanged
3	1	0	0	0	0	0	0	0	Control byte for initialization 0	Unchanged
4	1	0	1	0	0	1	0	0	Blank = 1	All pixels OFF
5	1	0	0	0	0	0	1	1	Control byte for initialization 3	All pixels OFF
6	0	0	1	0	1	0	1	1	Vlcd_level = 2Bh	All pixels OFF
7	1	0	0	0	0	0	1	0	Control byte for initialization 2	All pixels OFF
8	0	0	0	0	0	1	0	0	Vlcd_Dischg = 1	All pixels OFF
9	1	0	0	0	0	1	0	0	Control byte for initialization 4	All pixels OFF
10	1	1	1	0	0	0	0	0	Partial display on banks: 0, 1 and 2	All pixels OFF
Wait 30 ms										
11	1	0	0	0	0	0	1	0	Control byte for initialization 32	All pixels OFF
12	0	0	0	0	0	0	0	0	Vlcd_Dischg = 0	All pixels OFF
13	1	0	0	0	0	0	0	0	Control byte for initialization 0	All pixels OFF
14	1	0	1	0	0	0	0	0	Blank = 0 Partial display on banks: 0, 1 and 2	
15	1	0	0	0	0	1	0	0	Control byte for initialization 4	
16	1	1	1	0	0	0	1	0	Partial display on banks: 0, 2 and 3	

Remark:

This typical application example shows a LCD display 'ON' before the DDRAM is completely written, parts of the LCD are undefined as DDRAM data is random at power on. However, blank function can remain active until DDRAM is completed to avoid randomly ON or OFF pixels to appear on the LCD.

10 Pad location

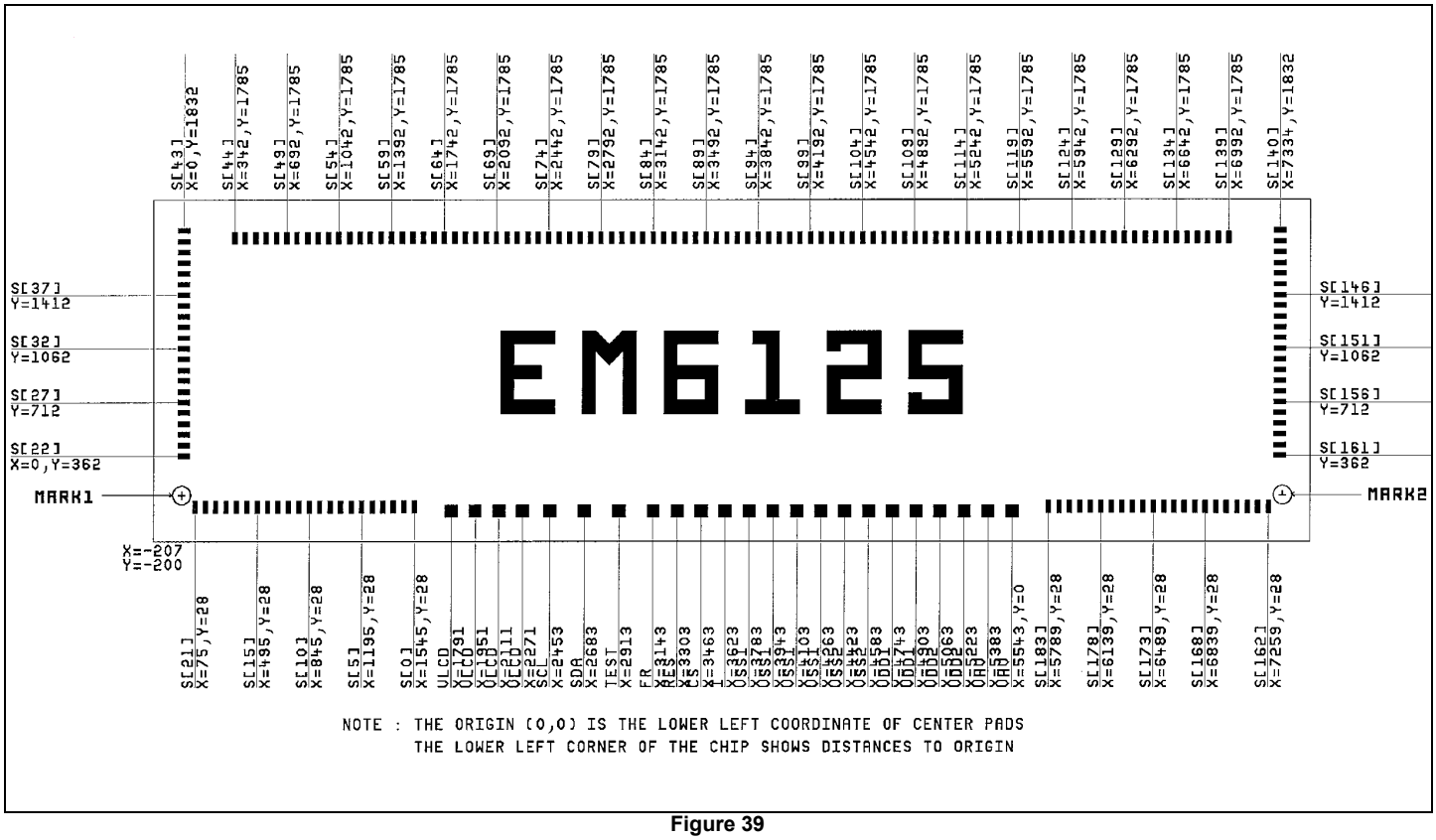
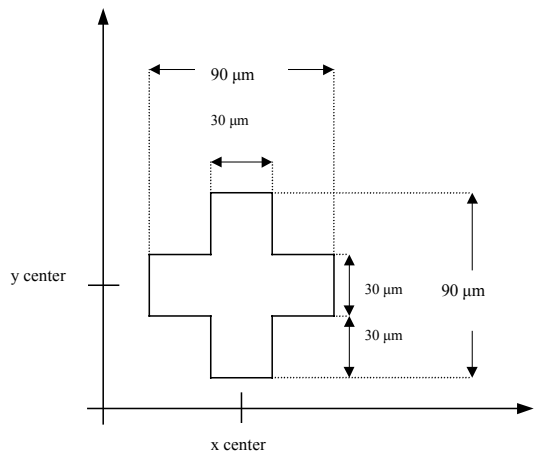


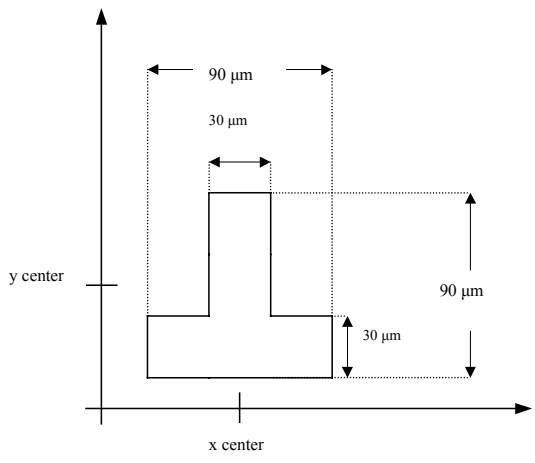
Figure 39

Mechanical Dimensions:

	Typical value	Unit
Minimum pad pitch	70	µm
Bump size pads from S[0] to S[183]	50×100×17.5	µm
Bump size interface pads	102×102×17.5	µm
Bump hardness	50	Vickers
Wafer thickness	380	µm
Chip Size	7775 ×2175	µm



MARK 1 : x = - 61, y = 209



MARK 2 : x = 7397, y = 209

Pad	Serial number	x	y
VHV	1	5543	0
VHV	2	5383	0
VDD2	3	5223	0
VDD2	4	5063	0
VDD1	5	4903	0
VDD1	6	4743	0
VSS2	7	4583	0
VSS2	8	4423	0
VSS1	9	4263	0
VSS1	10	4103	0
VSS1	11	3943	0
VSS1	12	3783	0
I	13	3623	0
CS	14	3463	0
RES	15	3303	0
FR	16	3143	0
TEST	17	2913	0
SDA	18	2683	0
SCL	19	2453	0
VLCD	20	2271	0
VLCD	21	2111	0
VLCD	22	1951	0
VLCD	23	1791	0
S0	24	1545	28
S1	25	1475	28
S2	26	1405	28
S3	27	1335	28
S4	28	1265	28
S5	29	1195	28
S6	30	1125	28
S7	31	1055	28
S8	32	985	28
S9	33	915	28
S10	34	845	28
S11	35	775	28
S12	36	705	28
S13	37	635	28
S14	38	565	28
S15	39	495	28
S16	40	425	28
S17	41	355	28
S18	42	285	28
S19	43	215	28
S20	44	145	28
S21	45	75	28
S22	46	0	362
S23	47	0	432
S24	48	0	502
S25	49	0	572
S26	50	0	642
S27	51	0	712
S28	52	0	782
S29	53	0	852
S30	54	0	922

Pad	Serial number	x	y
S31	55	0	992
S32	56	0	1062
S33	57	0	1132
S34	58	0	1202
S35	59	0	1272
S36	60	0	1342
S37	61	0	1412
S38	62	0	1482
S39	63	0	1552
S40	64	0	1622
S41	65	0	1692
S42	66	0	1762
S43	67	0	1832
S44	68	342	1785
S45	69	412	1785
S46	70	482	1785
S47	71	552	1785
S48	72	622	1785
S49	73	692	1785
S50	74	762	1785
S51	75	832	1785
S52	76	902	1785
S53	77	972	1785
S54	78	1042	1785
S55	79	1112	1785
S56	80	1182	1785
S57	81	1252	1785
S58	82	1322	1785
S59	83	1392	1785
S60	84	1462	1785
S61	85	1532	1785
S62	86	1602	1785
S63	87	1672	1785
S64	88	1742	1785
S65	89	1812	1785
S66	90	1882	1785
S67	91	1952	1785
S68	92	2022	1785
S69	93	2092	1785
S70	94	2162	1785
S71	95	2232	1785
S72	96	2302	1785
S73	97	2372	1785
S74	98	2442	1785
S75	99	2512	1785
S76	100	2582	1785
S77	101	2652	1785
S78	102	2722	1785
S79	103	2792	1785
S80	104	2862	1785
S81	105	2932	1785
S82	106	3002	1785
S83	107	3072	1785
S84	108	3142	1785

Pad	Serial number	x	y
S85	109	3212	1785
S86	110	3282	1785
S87	111	3352	1785
S88	112	3422	1785
S89	113	3492	1785
S90	114	3562	1785
S91	115	3632	1785
S92	116	3702	1785
S93	117	3772	1785
S94	118	3842	1785
S95	119	3912	1785
S96	120	3982	1785
S97	121	4052	1785
S98	122	4122	1785
S99	123	4192	1785
S100	124	4262	1785
S101	125	4332	1785
S102	126	4402	1785
S103	127	4472	1785
S104	128	4542	1785
S105	129	4612	1785
S106	130	4682	1785
S107	131	4752	1785
S108	132	4822	1785
S109	133	4892	1785
S110	134	4962	1785
S111	135	5032	1785
S112	136	5102	1785
S113	137	5172	1785
S114	138	5242	1785
S115	139	5312	1785
S116	140	5382	1785
S117	141	5452	1785
S118	142	5522	1785
S119	143	5592	1785
S120	144	5662	1785
S121	145	5732	1785
S122	146	5802	1785
S123	147	5872	1785
S124	148	5942	1785
S125	149	6012	1785
S126	150	6082	1785
S127	151	6152	1785
S128	152	6222	1785
S129	153	6292	1785
S130	154	6362	1785
S131	155	6432	1785
S132	156	6502	1785
S133	157	6572	1785
S134	158	6642	1785

Pad	Serial number	x	y
S135	159	6712	1785
S136	160	6782	1785
S137	161	6852	1785
S138	162	6922	1785
S139	163	6992	1785
S140	164	7334	1832
S141	165	7334	1762
S142	166	7334	1692
S143	167	7334	1622
S144	168	7334	1552
S145	169	7334	1482
S146	170	7334	1412
S147	171	7334	1342
S148	172	7334	1272
S149	173	7334	1202
S150	174	7334	1132
S151	175	7334	1062
S152	176	7334	992
S153	177	7334	922
S154	178	7334	852
S155	179	7334	782
S156	180	7334	712
S157	181	7334	642
S158	182	7334	572
S159	183	7334	502
S160	184	7334	432
S161	185	7334	362
S162	186	7259	28
S163	187	7189	28
S164	188	7119	28
S165	189	7049	28
S166	190	6979	28
S167	191	6909	28
S168	192	6839	28
S169	193	6769	28
S170	194	6699	28
S171	195	6629	28
S172	196	6559	28
S173	197	6489	28
S174	198	6419	28
S175	199	6349	28
S176	200	6279	28
S177	201	6209	28
S178	202	6139	28
S179	203	6069	28
S180	204	5999	28
S181	205	5929	28
S182	206	5859	28
S183	207	5789	28

Table 15: Pad location.

11 Ordering Information

When ordering please specify the complete part number and package.

Part Number	Die Form & Thickness	Bumping
EM6125WS27	Sawn Wafer, 27mils	No bumps
EM6125WP15	Waffle pack, 15mils	No bumps
EM6125WP15E	Waffle pack, 15mils	Gold Bumps

Other delivery form might be available upon request and for a minimum order quantity. Please contact EM sales.

12 Updates

Date ,Name Version	Chapter concerned	Old Version (Text, Figure, etc.)	New Version (Text, Figure, etc.)
22.11.01	All	First version	
02.04.02	8.5.1 Fig13,14,15	Row 17 Row 18	Row 9 Row10