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# HM5117400B Series

4,194,304-word × 4-bit Dynamic Random Access Memory

# HITACHI

ADE-203-369A (Z)

Rev. 1.0

Nov. 15, 1995

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## Description

The Hitachi HM5117400B is a CMOS dynamic RAM organized 4,194,304 word × 4 bit. It employs the most advanced CMOS technology for high performance and low power. The HM5117400B offers Fast Page Mode as a high speed access mode.

## Features

- Single 5 V ( $\pm 10\%$ )
- High speed
  - Access time : 60 ns/ 70 ns/ 80 ns (max)
- Low power dissipation
  - Active mode : 605 mW/550 mW/495 mW(max)
  - Standby mode : 11 mW (max)  
: 0.83 mW (max) (L-version)
- Fast page mode capability
- Long refresh period
  - 2048 refresh cycles : 32 ms  
: 128 ms (L-version)
- 3 variations of refresh
  - $\overline{\text{RAS}}$ -only refresh
  - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh
  - Hidden refresh
- Battery backup operation (L-version)
- Test function
  - 16-bit parallel test mode

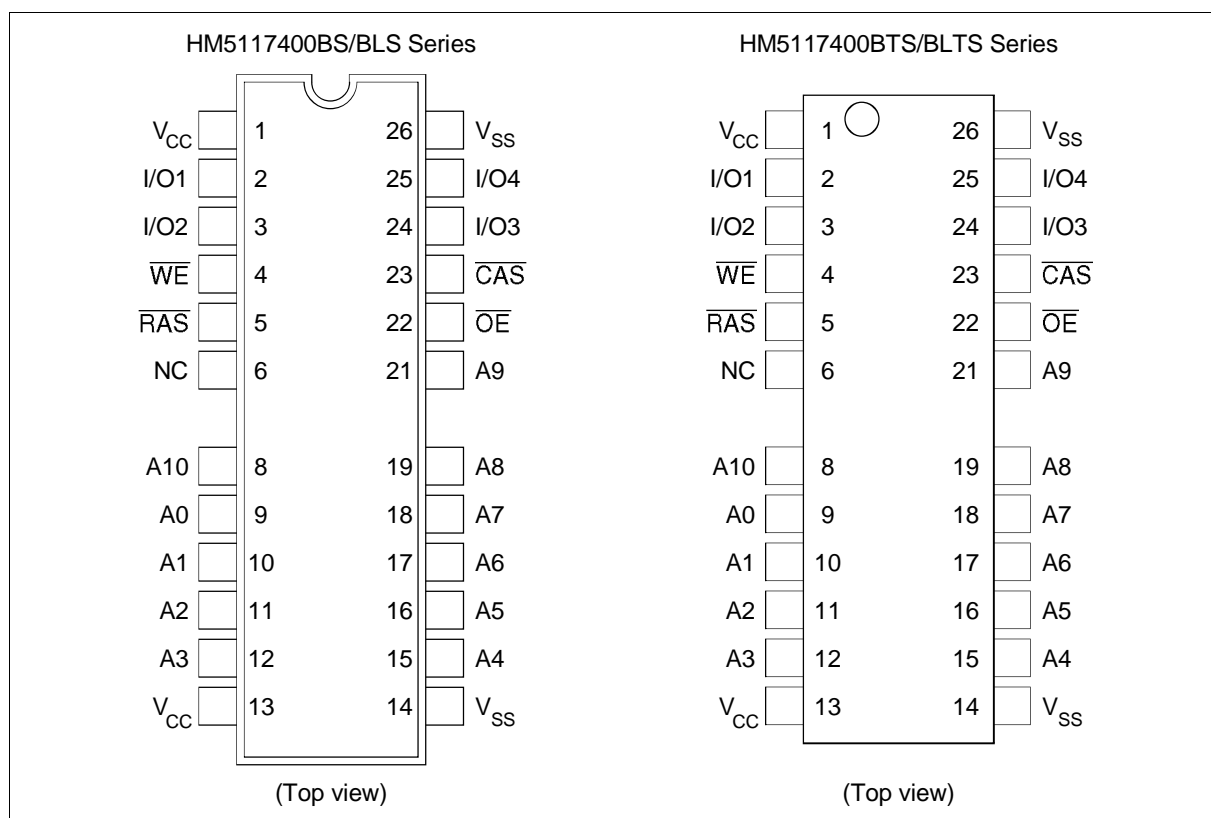
This specification is fully compatible with the 16-Mbit DRAM specifications from TEXAS INSTRUMENTS.

## HM5117400B Series

### Ordering Information

Type No.	Access Time	Package
HM5117400BS-6	60 ns	300-mil 26-pin plastic SOJ (CP-26/24DB)
HM5117400BS-7	70 ns	
HM5117400BS-8	80 ns	
HM5117400BLS-6	60 ns	300-mil 26-pin plastic TSOP II (TTP-26/24DA)
HM5117400BLS-7	70 ns	
HM5117400BLS-8	80 ns	
HM5117400BTS-6	60 ns	300-mil 26-pin plastic TSOP II (TTP-26/24DA)
HM5117400BTS-7	70 ns	
HM5117400BTS-8	80 ns	
HM5117400BLTS-6	60 ns	300-mil 26-pin plastic TSOP II (TTP-26/24DA)
HM5117400BLTS-7	70 ns	
HM5117400BLTS-8	80 ns	

### Pin Arrangement

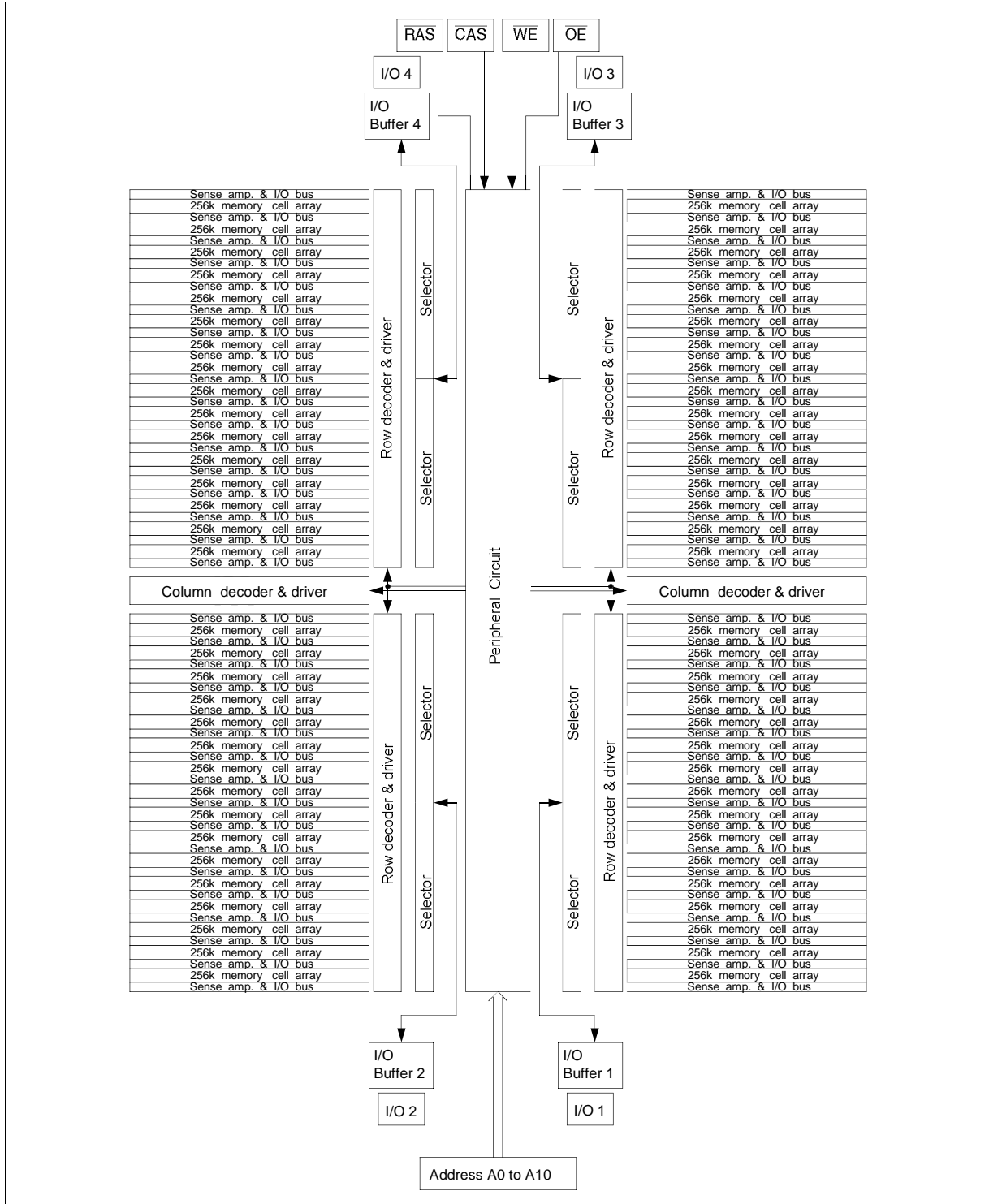


**Pin Description**

<b>Pin Name</b>	<b>Function</b>
A0 to A10	Address input
A0 to A10	Refresh address input
I/O1 to I/O4	Data input/data output
$\overline{\text{RAS}}$	Row address strobe
$\overline{\text{CAS}}$	Column address strobe
$\overline{\text{WE}}$	Write enable
$\overline{\text{OE}}$	Output enable
$V_{\text{CC}}$	Power supply (+5 V)
$V_{\text{SS}}$	Ground
NC	No connection

# HM5117400B Series

## Block Diagram



HITACHI

**Absolute Maximum Ratings**

Parameter	Symbol	Value	Unit
Voltage on any pin relative to $V_{SS}$	$V_T$	-1.0 to +7.0	V
Supply voltage relative to $V_{SS}$	$V_{CC}$	-1.0 to +7.0	V
Short circuit output current	$I_{out}$	50	mA
Power dissipation	$P_T$	1.0	W
Operating temperature	$T_{opr}$	0 to +70	°C
Storage temperature	$T_{stg}$	-55 to +125	°C

**Recommended DC Operating Conditions ( $T_a = 0$  to  $+70^\circ\text{C}$ )**

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	$V_{CC}$	4.5	5.0	5.5	V	1
Input high voltage	$V_{IH}$	2.4	—	6.5	V	1
Input low voltage	$V_{IL}$	-1.0	—	0.8	V	1

Note: 1. All voltage referred to  $V_{SS}$

**DC Characteristics ( $T_a = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ )**

Parameter	Symbol	HM5117400B						Unit	Test Conditions
		-6		-7		-8			
		Min	Max	Min	Max	Min	Max		
Operating current <sup>*1,*2</sup>	$I_{CC1}$	—	110	—	100	—	90	mA	$t_{RC} = \text{min}$
Standby current	$I_{CC2}$	—	2	—	2	—	2	mA	TTL interface $\overline{\text{RAS}}, \overline{\text{CAS}} = V_{IH}$ Dout = High-Z
		—	1	—	1	—	1	mA	CMOS interface $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{CC} - 0.2\text{V}$ Dout = High-Z
Standby current (L-version)	$I_{CC2}$	—	150	—	150	—	150	$\mu\text{A}$	CMOS interface $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{CC} - 0.2\text{V}$ Dout = High-Z

## HM5117400B Series

**DC Characteristics** ( $T_a = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	HM5117400B						Unit	Test Conditions
		-6		-7		-8			
		Min	Max	Min	Max	Min	Max		
$\overline{\text{RAS}}$ -only refresh current <sup>*2</sup>	$I_{CC3}$	—	110	—	100	—	90	mA	$t_{RC} = \text{min}$
Standby current <sup>*1</sup>	$I_{CC5}$	—	5	—	5	—	5	mA	$\overline{\text{RAS}} = V_{IH}$ , $\overline{\text{CAS}} = V_{IL}$ Dout = enable
$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh current	$I_{CC6}$	—	110	—	100	—	90	mA	$t_{RC} = \text{min}$
Fast page mode current <sup>*1, *3</sup>	$I_{CC7}$	—	80	—	70	—	65	mA	$t_{PC} = \text{min}$
Battery backup current	$I_{CC10}$	—	350	—	350	—	350	$\mu\text{A}$	CMOS interface Dout = High-Z CBR refresh: $t_{RC} = 62.5\ \mu\text{s}$ $t_{RAS} \leq 0.3\ \mu\text{s}$
Input leakage current	$I_{LI}$	-10	10	-10	10	-10	10	$\mu\text{A}$	$0\text{ V} \leq V_{in} \leq 7\text{ V}$
Output leakage current	$I_{LO}$	-10	10	-10	10	-10	10	$\mu\text{A}$	$0\text{ V} \leq V_{out} \leq 7\text{ V}$ Dout = disable
Output high voltage	$V_{OH}$	2.4	$V_{CC}$	2.4	$V_{CC}$	2.4	$V_{CC}$	V	High Iout = -5 mA
Output low voltage	$V_{OL}$	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA

Notes: 1.  $I_{CC}$  depends on output load condition when the device is selected.  $I_{CC}$  max is specified at the output open condition.

2. Address can be changed once or less while  $\overline{\text{RAS}} = V_{IL}$ .

3. Address can be changed once or less while  $\overline{\text{CAS}} = V_{IH}$ .

**Capacitance** ( $T_a = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{ V} \pm 10\%$ )

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	$C_{I1}$	—	5	pF	1
Input capacitance (Clocks)	$C_{I2}$	—	7	pF	1
Output capacitance (Data-in, Data-out)	$C_{I/O}$	—	7	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2.  $\overline{\text{CAS}} = V_{IH}$  to disable Dout.

## HM5117400B Series

**AC Characteristics** ( $T_a = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ )<sup>\*1, \*2, \*18, \*19</sup>

### Test Conditions

- Input rise and fall time: 5 ns
- Input timing reference levels : 0.8 V, 2.4 V
- Output load : 2 TTL gate +  $C_L$  (100 pF) (Including scope and jig)

### Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

		HM5117400B							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	$t_{RC}$	110	—	130	—	150	—	ns	
$\overline{\text{RAS}}$ precharge time	$t_{RP}$	40	—	50	—	60	—	ns	
$\overline{\text{CAS}}$ precharge time	$t_{CP}$	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ pulse width	$t_{RAS}$	60	10000	70	10000	80	10000	ns	
$\overline{\text{CAS}}$ pulse width	$t_{CAS}$	15	10000	18	10000	20	10000	ns	
Row address setup time	$t_{ASR}$	0	—	0	—	0	—	ns	
Row address hold time	$t_{RAH}$	10	—	10	—	10	—	ns	
Column address setup time	$t_{ASC}$	0	—	0	—	0	—	ns	
Column address hold time	$t_{CAH}$	10	—	15	—	15	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	$t_{RCD}$	20	45	20	52	20	60	ns	3
$\overline{\text{RAS}}$ to column address delay time	$t_{RAD}$	15	30	15	35	15	40	ns	4
$\overline{\text{RAS}}$ hold time	$t_{RSH}$	15	—	18	—	20	—	ns	
$\overline{\text{CAS}}$ hold time	$t_{CSH}$	60	—	70	—	80	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	$t_{CRP}$	5	—	5	—	5	—	ns	
$\overline{\text{OE}}$ to Din delay time	$t_{OED}$	15	—	18	—	20	—	ns	5
$\overline{\text{OE}}$ delay time from Din	$t_{DZO}$	0	—	0	—	0	—	ns	6
$\overline{\text{CAS}}$ delay time from Din	$t_{DZC}$	0	—	0	—	0	—	ns	6
Transition time (rise and fall)	$t_T$	3	50	3	50	3	50	ns	7

## HM5117400B Series

### Read Cycle

Parameter	Symbol	HM5117400B						Unit	Notes
		-6		-7		-8			
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{\text{RAS}}$	$t_{\text{RAC}}$	—	60	—	70	—	80	ns	8, 9, 20
Access time from $\overline{\text{CAS}}$	$t_{\text{CAC}}$	—	15	—	18	—	20	ns	9, 10, 17, 20
Access time from address	$t_{\text{AA}}$	—	30	—	35	—	40	ns	9, 11, 17, 20
Access time from $\overline{\text{OE}}$	$t_{\text{OEA}}$	—	15	—	18	—	20	ns	9, 20
Read command setup time	$t_{\text{RCS}}$	0	—	0	—	0	—	ns	
Read command hold time to $\overline{\text{CAS}}$	$t_{\text{RCH}}$	0	—	0	—	0	—	ns	12
Read command hold time to $\overline{\text{RAS}}$	$t_{\text{RRH}}$	0	—	0	—	0	—	ns	12
Column address to $\overline{\text{RAS}}$ lead time	$t_{\text{RAL}}$	30	—	35	—	40	—	ns	
Column address to $\overline{\text{CAS}}$ lead time	$t_{\text{CAL}}$	30	—	35	—	40	—	ns	
$\overline{\text{CAS}}$ to output in low-Z	$t_{\text{CLZ}}$	0	—	0	—	0	—	ns	
Output data hold time	$t_{\text{OH}}$	3	—	3	—	3	—	ns	
Output data hold time from $\overline{\text{OE}}$	$t_{\text{OHO}}$	3	—	3	—	3	—	ns	
Output buffer turn-off time	$t_{\text{OFF}}$	—	15	—	15	—	15	ns	13
Output buffer turn-off to $\overline{\text{OE}}$	$t_{\text{OEZ}}$	—	15	—	15	—	15	ns	13
$\overline{\text{CAS}}$ to Din delay time	$t_{\text{CDD}}$	15	—	18	—	20	—	ns	5

### Write Cycle

Parameter	Symbol	HM5117400B						Unit	Notes
		-6		-7		-8			
		Min	Max	Min	Max	Min	Max		
Write command setup time	$t_{\text{WCS}}$	0	—	0	—	0	—	ns	14
Write command hold time	$t_{\text{WCH}}$	10	—	15	—	15	—	ns	
Write command pulse width	$t_{\text{WP}}$	10	—	10	—	10	—	ns	
Write command to $\overline{\text{RAS}}$ lead time	$t_{\text{RWL}}$	15	—	18	—	20	—	ns	
Write command to $\overline{\text{CAS}}$ lead time	$t_{\text{CWL}}$	15	—	18	—	20	—	ns	
Data-in setup time	$t_{\text{DS}}$	0	—	0	—	0	—	ns	15
Data-in hold time	$t_{\text{DH}}$	10	—	15	—	15	—	ns	15



## HM5117400B Series

### Read-Modify-Write Cycle

		HM5117400B							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Read-modify-write cycle time	$t_{RWC}$	155	—	181	—	205	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	$t_{RWD}$	85	—	98	—	110	—	ns	14
$\overline{CAS}$ to $\overline{WE}$ delay time	$t_{CWD}$	40	—	46	—	50	—	ns	14
Column address to $\overline{WE}$ delay time	$t_{AWD}$	55	—	63	—	70	—	ns	14
$\overline{OE}$ hold time from $\overline{WE}$	$t_{OEh}$	15	—	18	—	20	—	ns	

### Refresh Cycle

		HM5117400B							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{CAS}$ setup time (CBR refresh cycle)	$t_{CSR}$	5	—	5	—	5	—	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	$t_{CHR}$	10	—	10	—	10	—	ns	
$\overline{WE}$ setup time (CBR refresh cycle)	$t_{WRP}$	0	—	0	—	0	—	ns	
$\overline{WE}$ hold time (CBR refresh cycle)	$t_{WRH}$	10	—	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	$t_{RPC}$	0	—	0	—	0	—	ns	

### Fast Page Mode Cycle

		HM5117400B							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Fast page mode cycle time	$t_{PC}$	40	—	45	—	50	—	ns	
Fast page mode $\overline{RAS}$ pulse width	$t_{RASP}$	—	100000	—	100000	—	100000	ns	16
Access time from $\overline{CAS}$ precharge	$t_{CPA}$	—	35	—	40	—	45	ns	9, 17, 20
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	$t_{CPRH}$	35	—	40	—	45	—	ns	

## HM5117400B Series

### Fast Page Mode Read-Modify-Write Cycle

		HM5117400B							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Fast page mode read-modify-write cycle time	$t_{PRWC}$	85	—	96	—	105	—	ns	
$\overline{WE}$ delay time from $\overline{CAS}$ precharge	$t_{CPW}$	60	—	68	—	75	—	ns	14

### Test Mode Cycle<sup>\*19</sup>

		HM5117400B							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Test mode $\overline{WE}$ setup time	$t_{WTS}$	0	—	0	—	0	—	ns	
Test mode $\overline{WE}$ hold time	$t_{WTH}$	10	—	10	—	10	—	ns	

### Refresh

Parameter	Symbol	Max	Unit	Note
Refresh period	$t_{REF}$	32	ms	2048 cycles
Refresh period (L-version)	$t_{REF}$	128	ms	2048 cycles

Notes: 1. AC measurements assume  $t_T = 5$  ns.

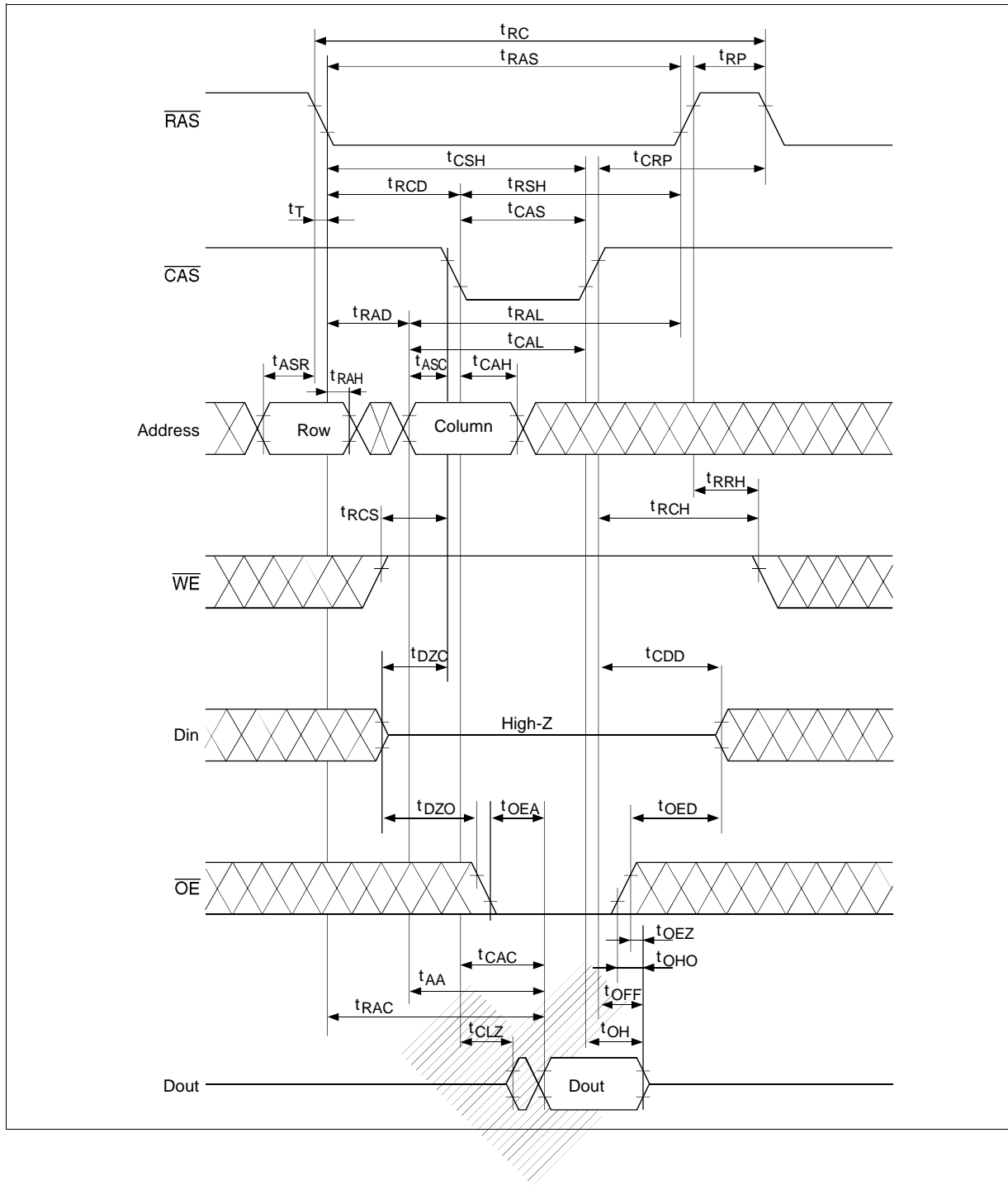
- An initial pause of 200  $\mu$ s is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing RAS-only refresh or  $\overline{CAS}$ -before-RAS refresh). If the internal refresh counter is used, a minimum of eight  $\overline{CAS}$ -before-RAS refresh cycles are required.
- Operation with the  $t_{RCD}$  (max) limit insures that  $t_{RAC}$  (max) can be met,  $t_{RCD}$  (max) is specified as a reference point only; if  $t_{RCD}$  is greater than the specified  $t_{RCD}$  (max) limit, then access time is controlled exclusively by  $t_{CAC}$ .
- Operation with the  $t_{RAD}$  (max) limit insures that  $t_{RAC}$  (max) can be met,  $t_{RAD}$  (max) is specified as a reference point only; if  $t_{RAD}$  is greater than the specified  $t_{RAD}$  (max) limit, then access time is controlled exclusively by  $t_{AA}$ .
- Either  $t_{OED}$  or  $t_{CDD}$  must be satisfied.
- Either  $t_{DZO}$  or  $t_{DZC}$  must be satisfied.
- $V_{IH}$  (min) and  $V_{IL}$  (max) are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  (min) and  $V_{IL}$  (max).
- Assumes that  $t_{RCD} \leq t_{RCD}$  (max) and  $t_{RAD} \leq t_{RAD}$  (max). If  $t_{RCD}$  or  $t_{RAD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  exceeds the value shown.
- Measured with a load circuit equivalent to 2 TTL loads and 100 pF.

10. Assumes that  $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$  and  $t_{\text{RCD}} + t_{\text{CAC}}(\text{max}) \geq t_{\text{RAD}} + t_{\text{AA}}(\text{max})$ .
11. Assumes that  $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{max})$  and  $t_{\text{RCD}} + t_{\text{CAC}}(\text{max}) \leq t_{\text{RAD}} + t_{\text{AA}}(\text{max})$ .
12. Either  $t_{\text{RCH}}$  or  $t_{\text{RRH}}$  must be satisfied for a read cycles.
13.  $t_{\text{OFF}}(\text{max})$  and  $t_{\text{OEZ}}(\text{max})$  define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
14.  $t_{\text{WCS}}$ ,  $t_{\text{RWD}}$ ,  $t_{\text{CWD}}$ ,  $t_{\text{AWD}}$  and  $t_{\text{CPW}}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if  $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$ , the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if  $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$ ,  $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$ , and  $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$ , or  $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$ ,  $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$  and  $t_{\text{CPW}} \geq t_{\text{CPW}}(\text{min})$ , the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. These parameters are referred to  $\overline{\text{CAS}}$  leading edge in early write cycles and to  $\overline{\text{WE}}$  leading edge in delayed write or read-modify-write cycles.
16.  $t_{\text{RASP}}$  defines  $\overline{\text{RAS}}$  pulse width in fast page mode cycles.
17. Access time is determined by the longest among  $t_{\text{AA}}$ ,  $t_{\text{CAC}}$  and  $t_{\text{CPA}}$ .
18. In delayed write or read-modify-write cycles,  $\overline{\text{OE}}$  must disable output buffer prior to applying data to the device. After  $\overline{\text{RAS}}$  is reset, if  $t_{\text{OEH}} \geq t_{\text{CWL}}$ , the I/O pin will remain open circuit (high impedance); if  $t_{\text{OEH}} < t_{\text{CWL}}$ , invalid data will be out at each I/O.
19. The 16M DRAM offers a 16-bit time saving parallel test mode. Address CA0 and CA1 for the 4M × 4 are don't care during test mode. Test mode is set by performing  $\overline{\text{WE}}$ -and- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  (WCBR) cycle. In 16-bit parallel test mode, data is written into 4 bits in parallel at each I/O (I/O1 to I/O4) and read out from each I/O.  
 If 4 bits of each I/O are equal (all 1s or 0s), data output pin is a high state during test mode read cycle, then the device has passed. If they are not equal, data output pin is a low state, then the device has failed.  
 Refresh during test mode operation can be performed by normal read cycles or by WCBR refresh cycles.  
 To get out of test mode and enter a normal operation mode, perform either a regular  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycle or  $\overline{\text{RAS}}$ -only refresh cycle.
20. In a test mode read cycle, the value of  $t_{\text{RAC}}$ ,  $t_{\text{AA}}$ ,  $t_{\text{CAC}}$  and  $t_{\text{CPA}}$  is delayed by 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
21. XXX: H or L (H:  $V_{\text{IH}}(\text{min}) \leq V_{\text{IN}} \leq V_{\text{IH}}(\text{max})$ , L:  $V_{\text{IL}}(\text{min}) \leq V_{\text{IN}} \leq V_{\text{IL}}(\text{max})$ )  
 /////////////// Invalid Dout

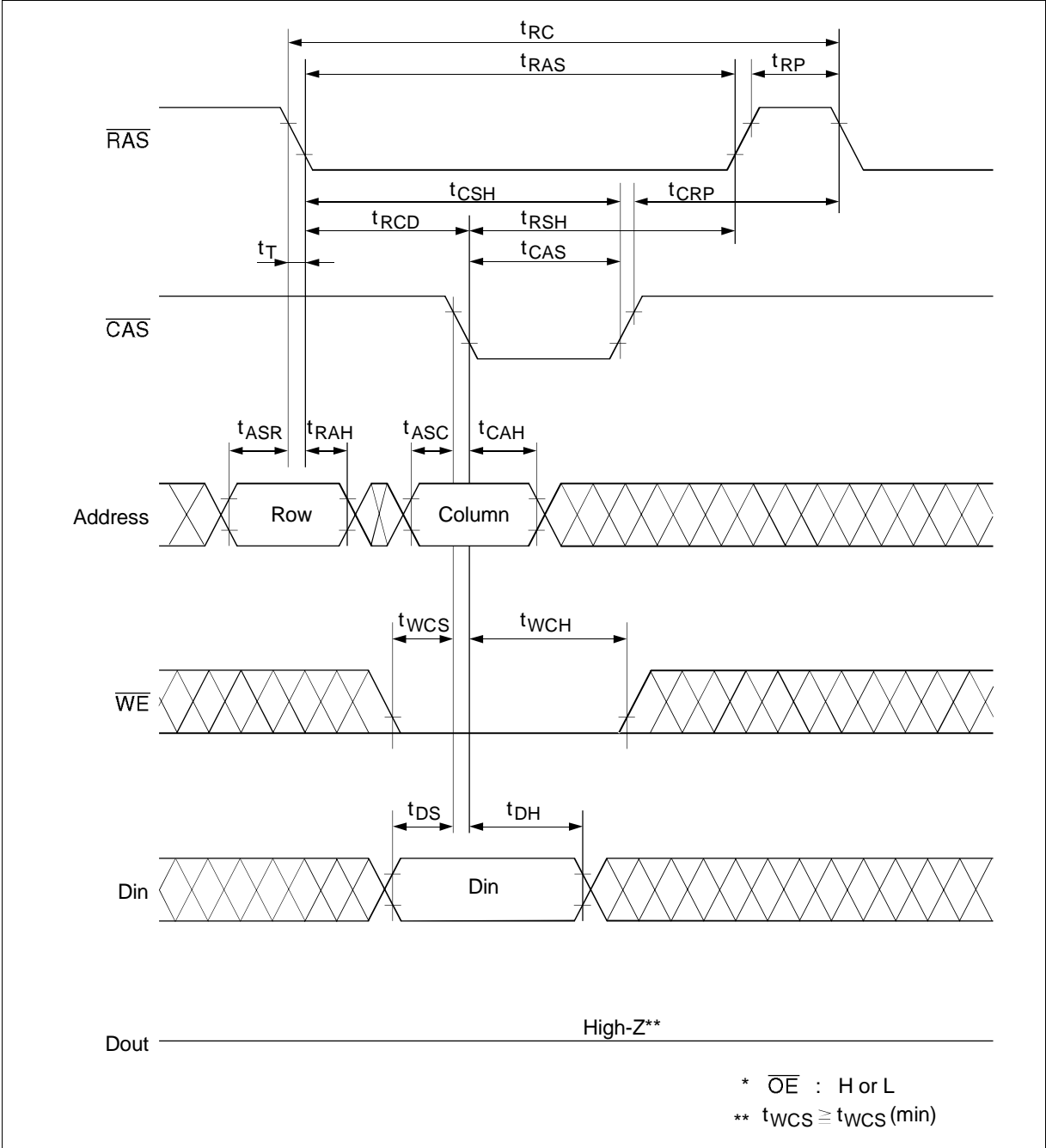
# HM5117400B Series

## Timing Waveforms<sup>\*21</sup>

### Read Cycle

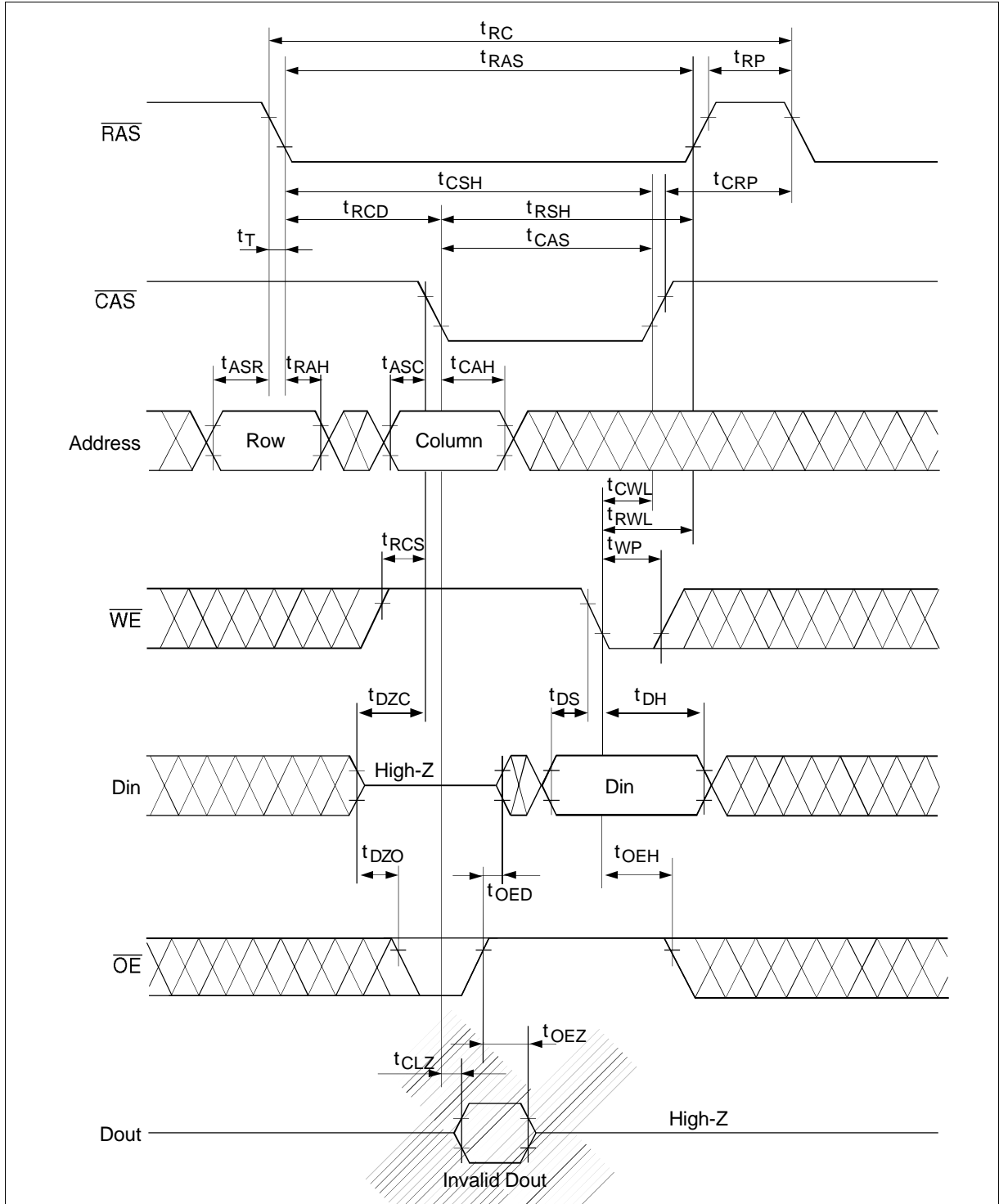


Early Write Cycle

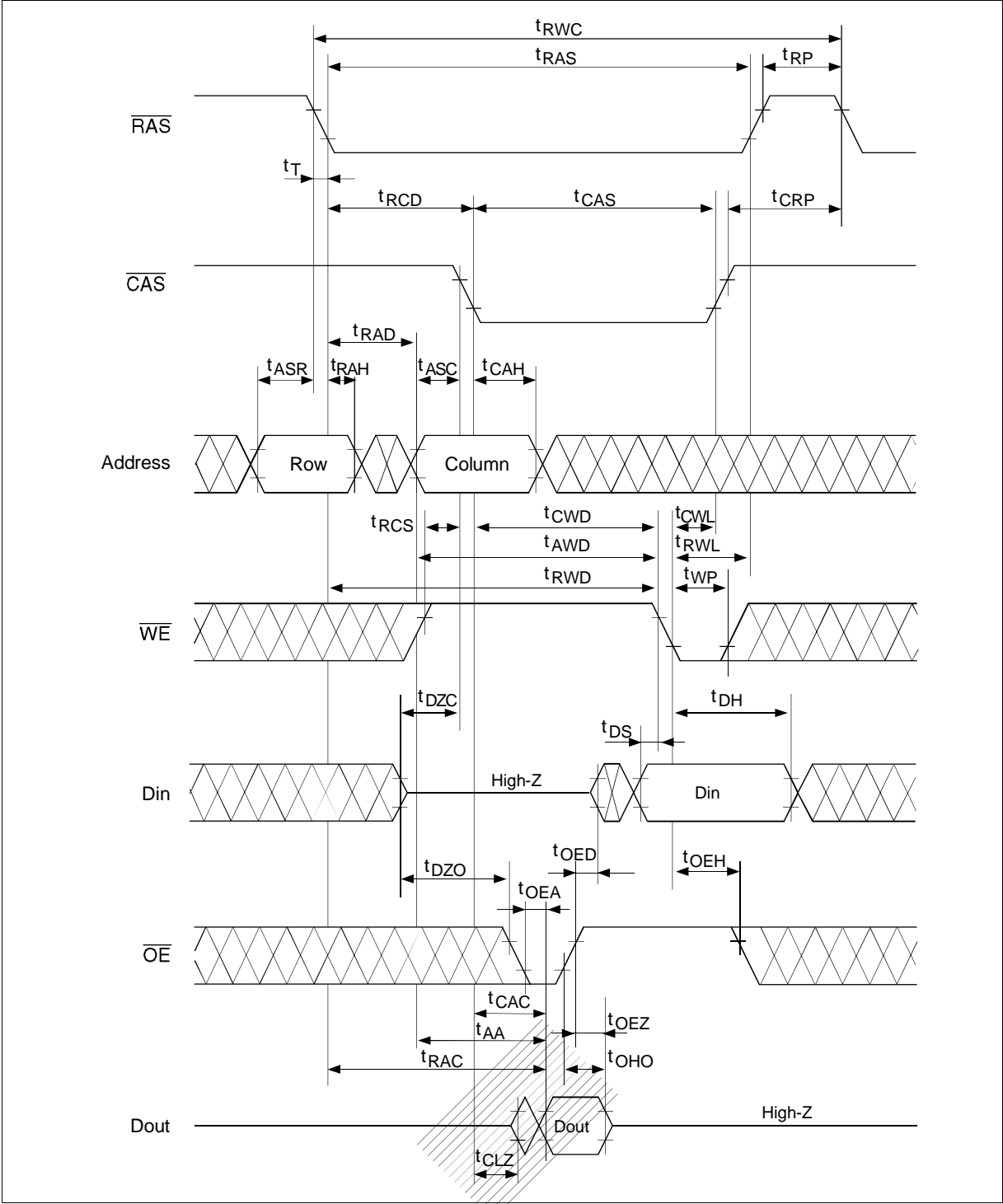


# HM5117400B Series

## Delayed Write Cycle <sup>\*18</sup>

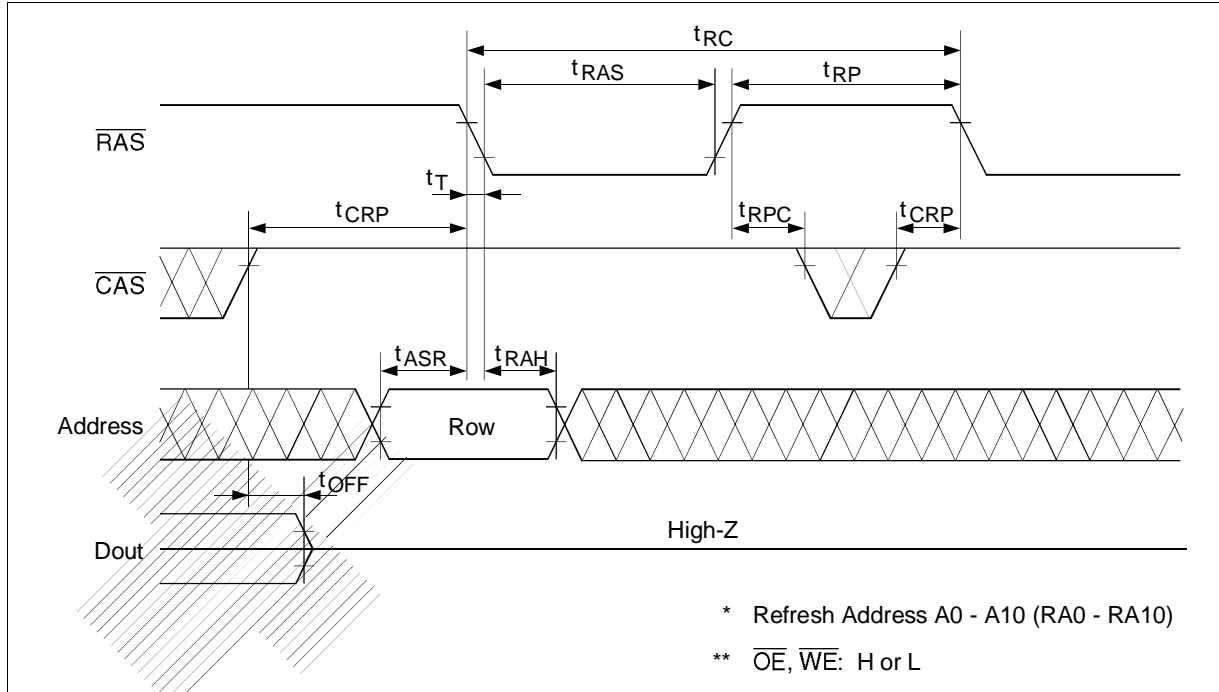


Read-Modify-Write Cycle\*18



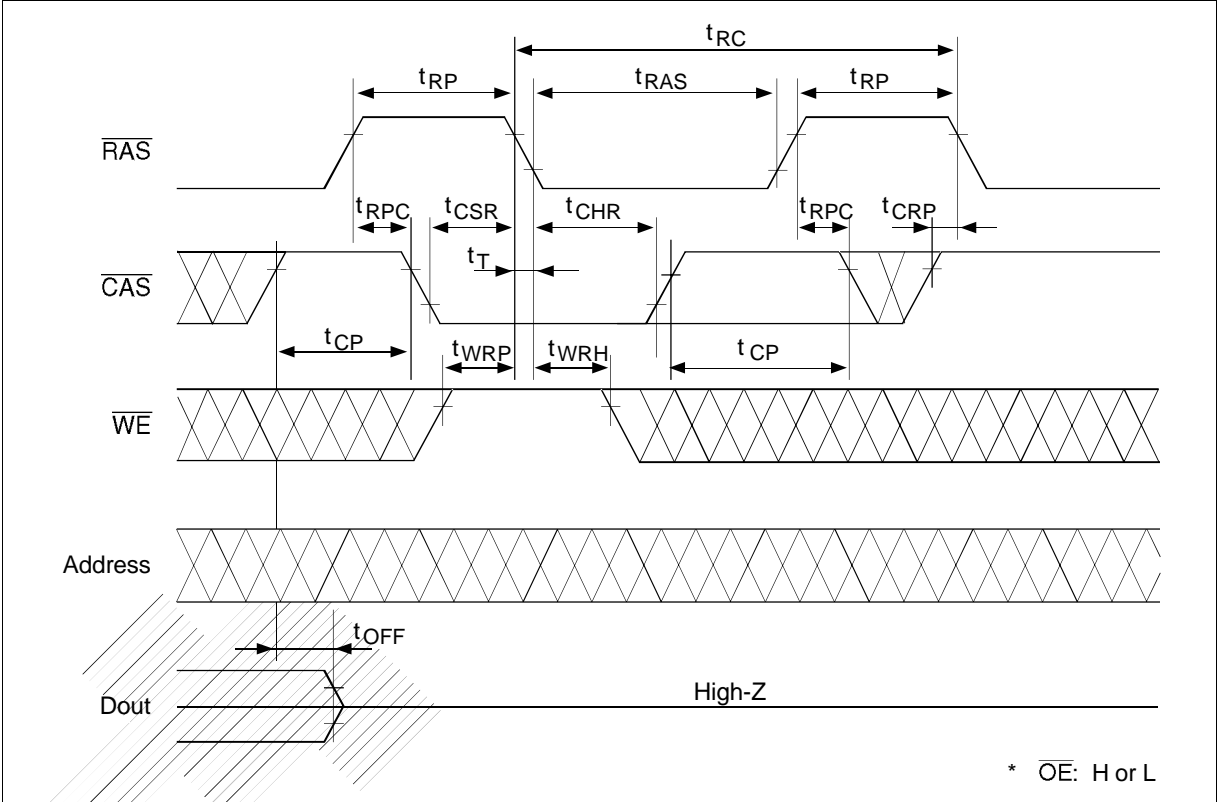
# HM5117400B Series

## RAS-Only Refresh Cycle



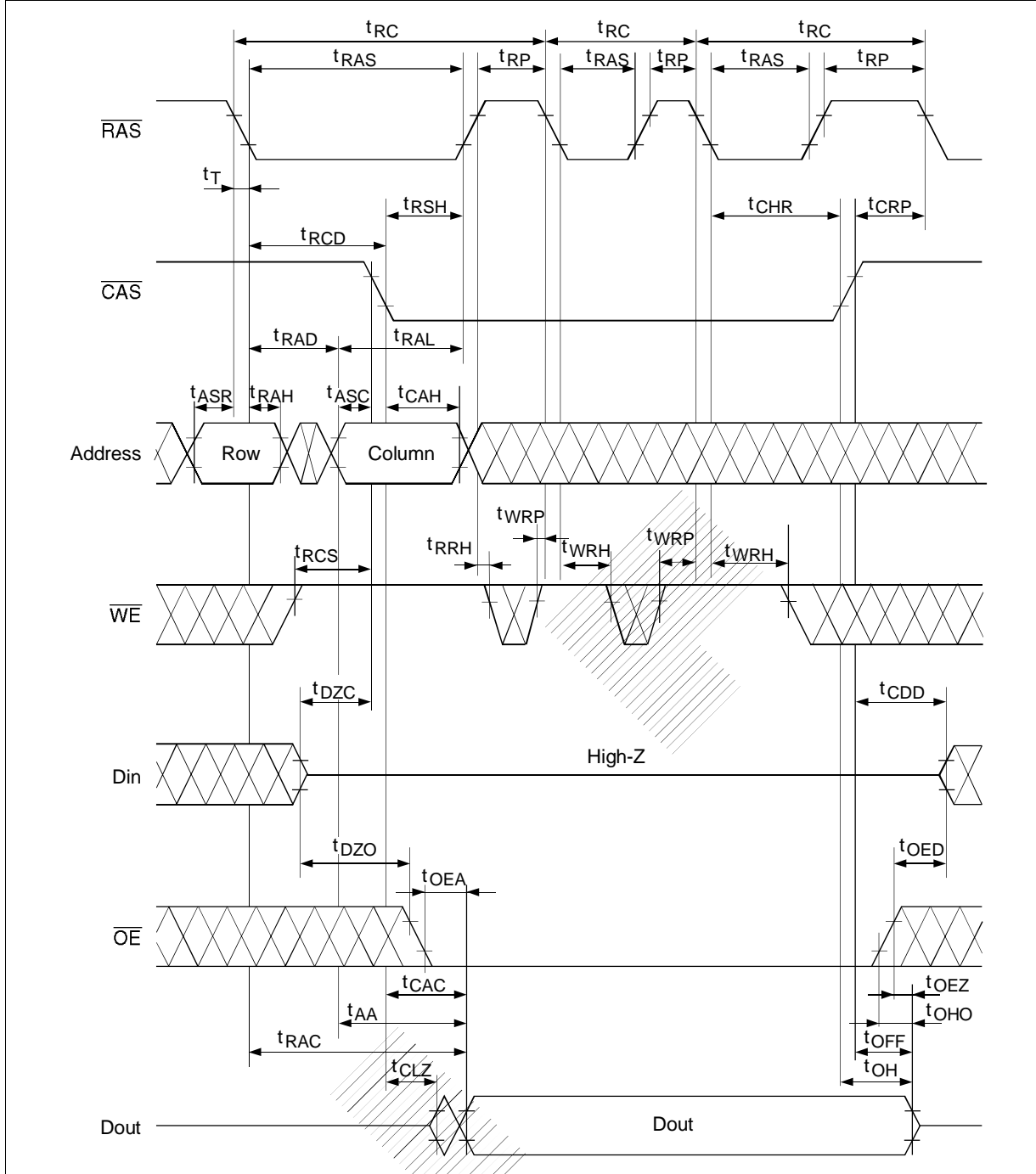


CAS-Before-RAS Refresh Cycle

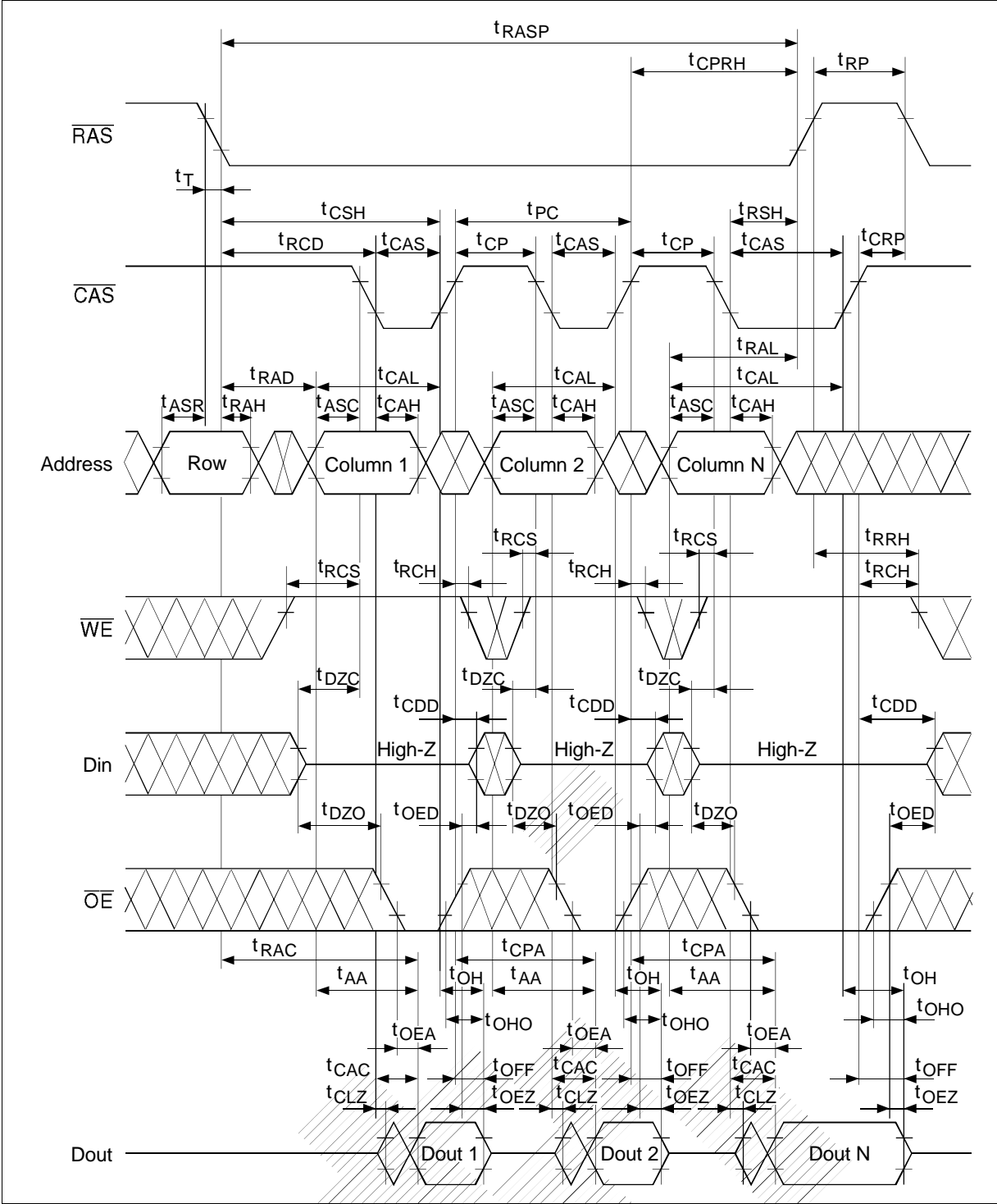


# HM5117400B Series

## Hidden Refresh Cycle

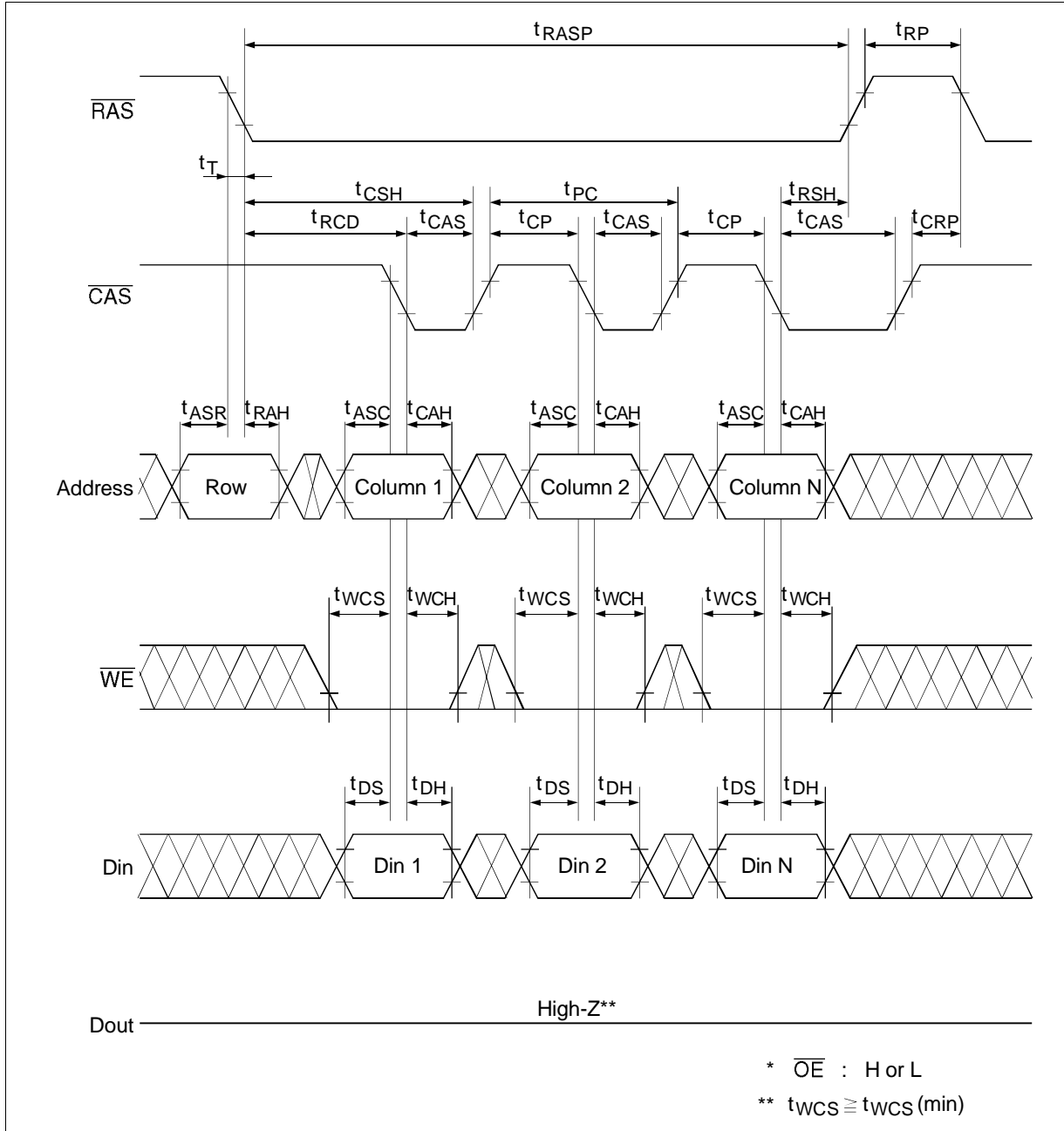


Fast Page Mode Read Cycle

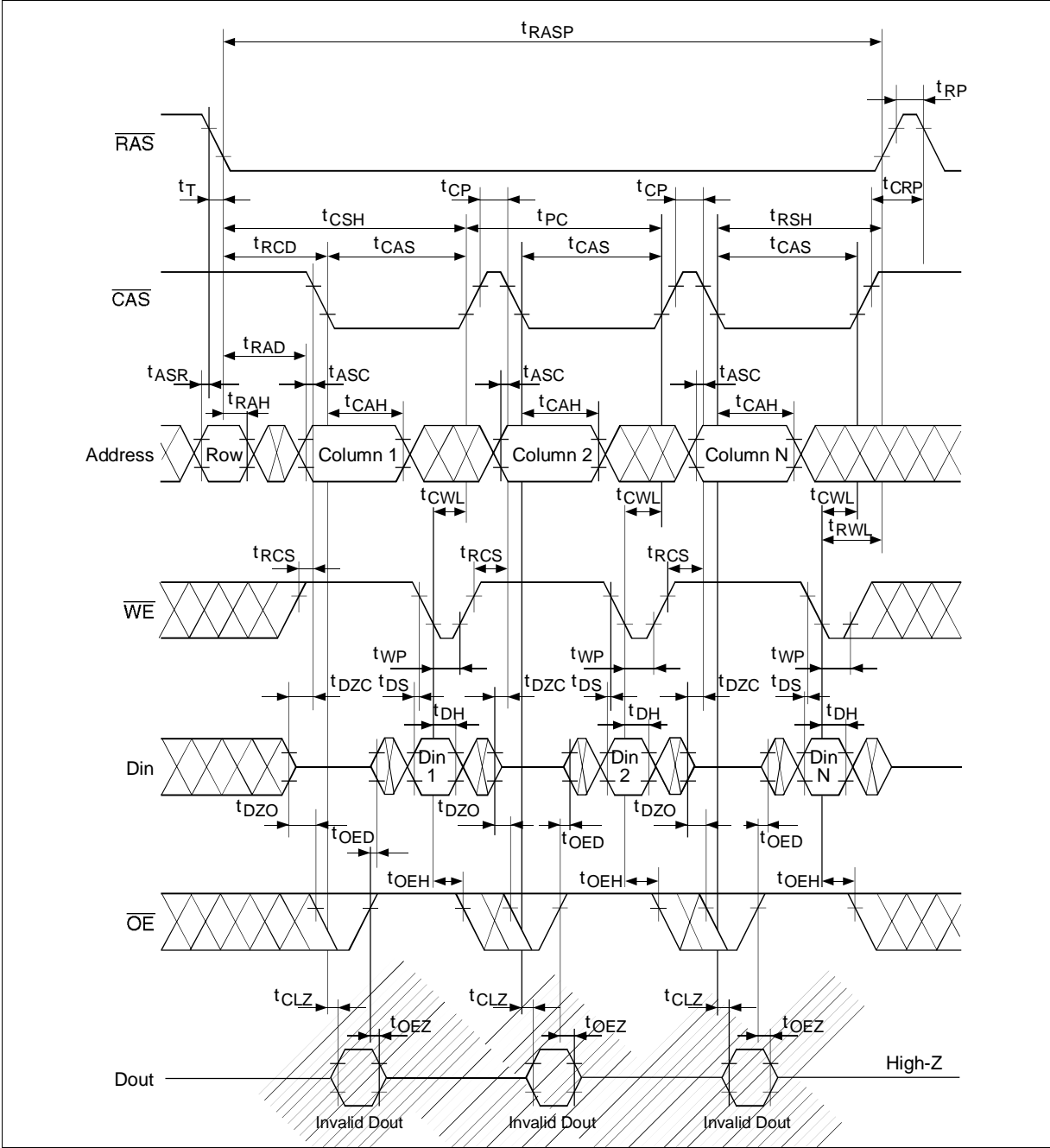


# HM5117400B Series

## Fast Page Mode Early Write Cycle

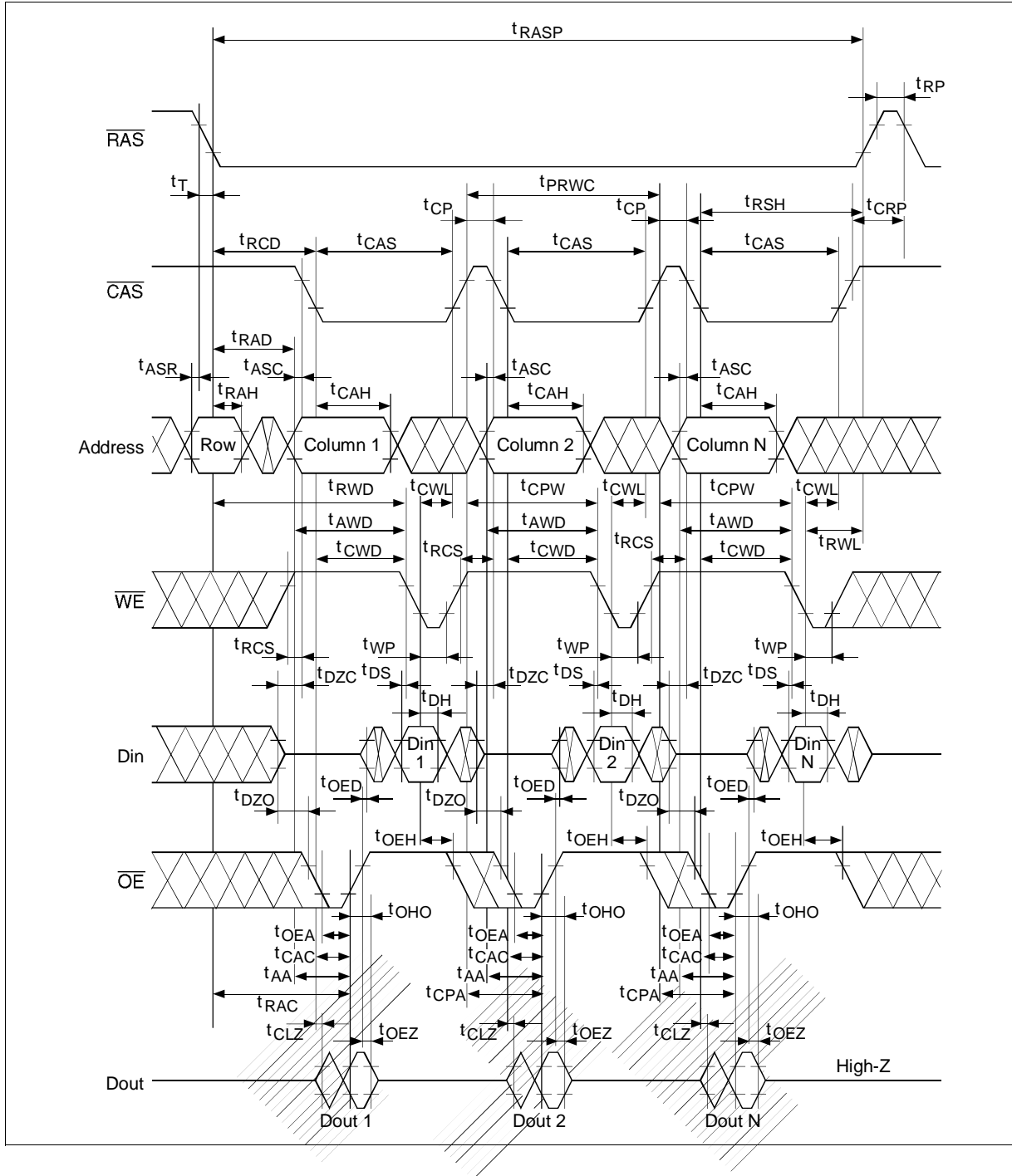


Fast Page Mode Delayed Write Cycle <sup>\*18</sup>

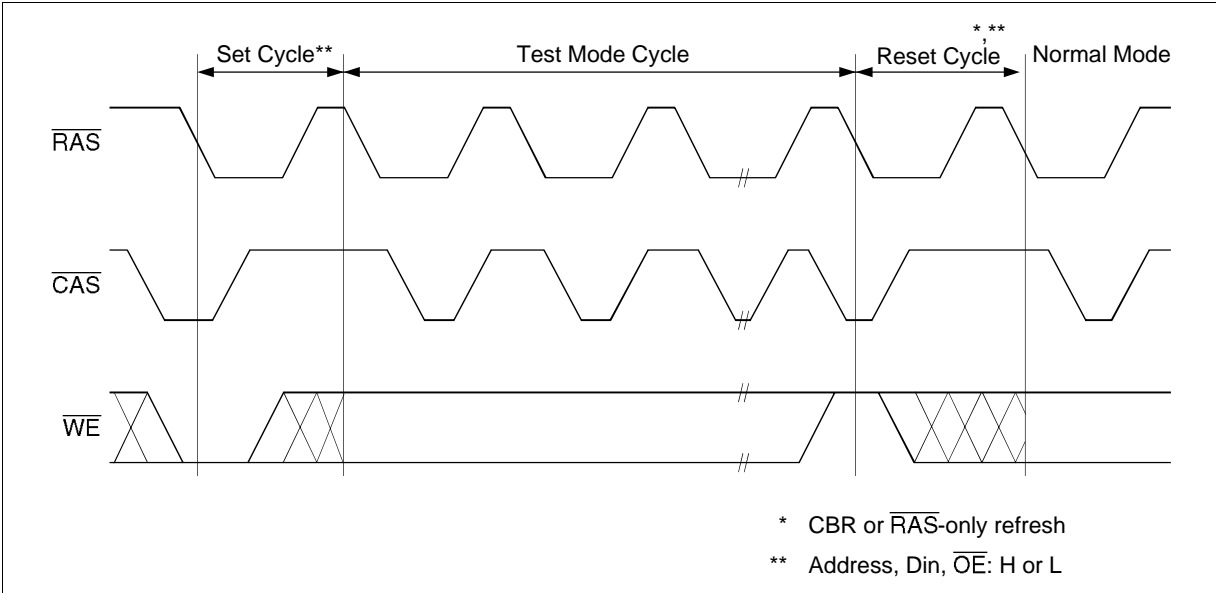


# HM5117400B Series

## Fast Page Mode Read-Modify-Write Cycle <sup>\*18</sup>

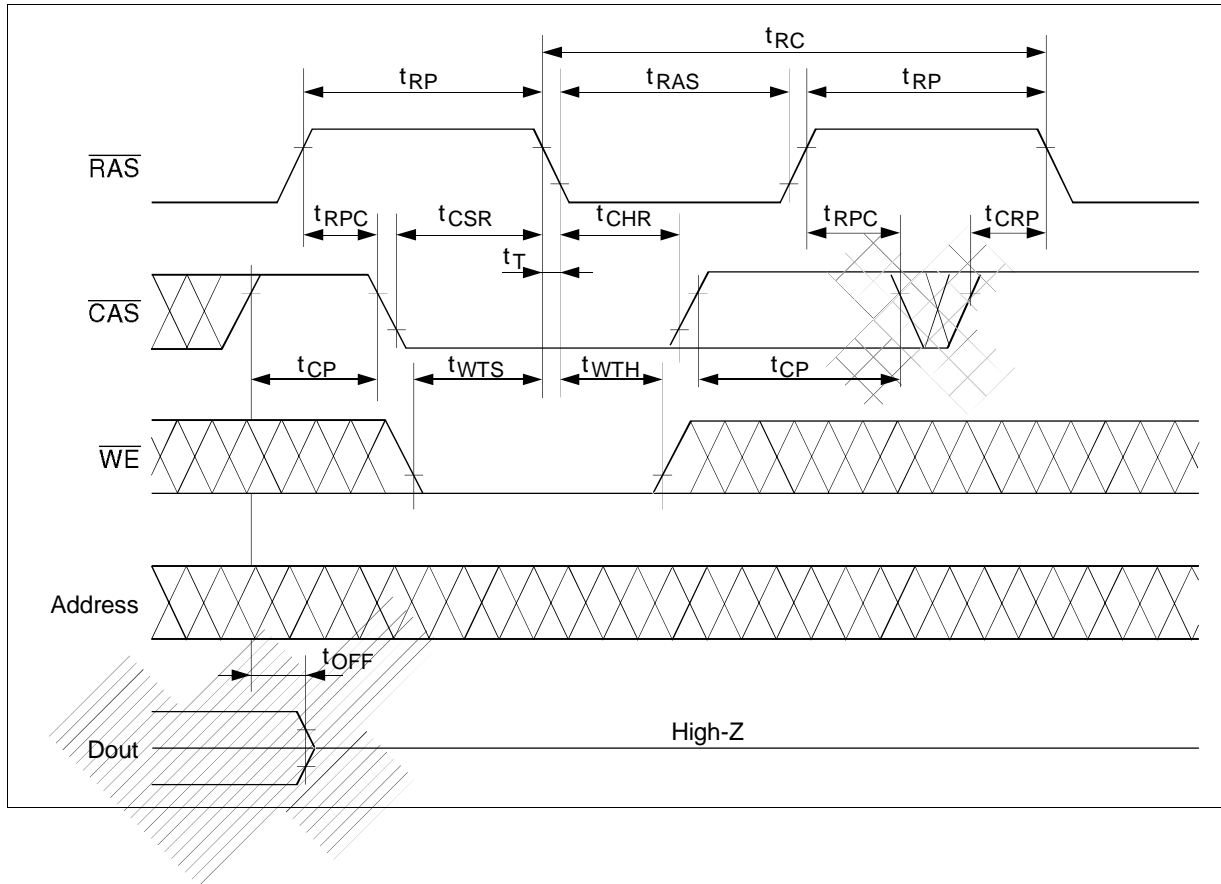


Test Mode Cycle<sup>\*19</sup>



# HM5117400B Series

## Test Mode Set Cycle



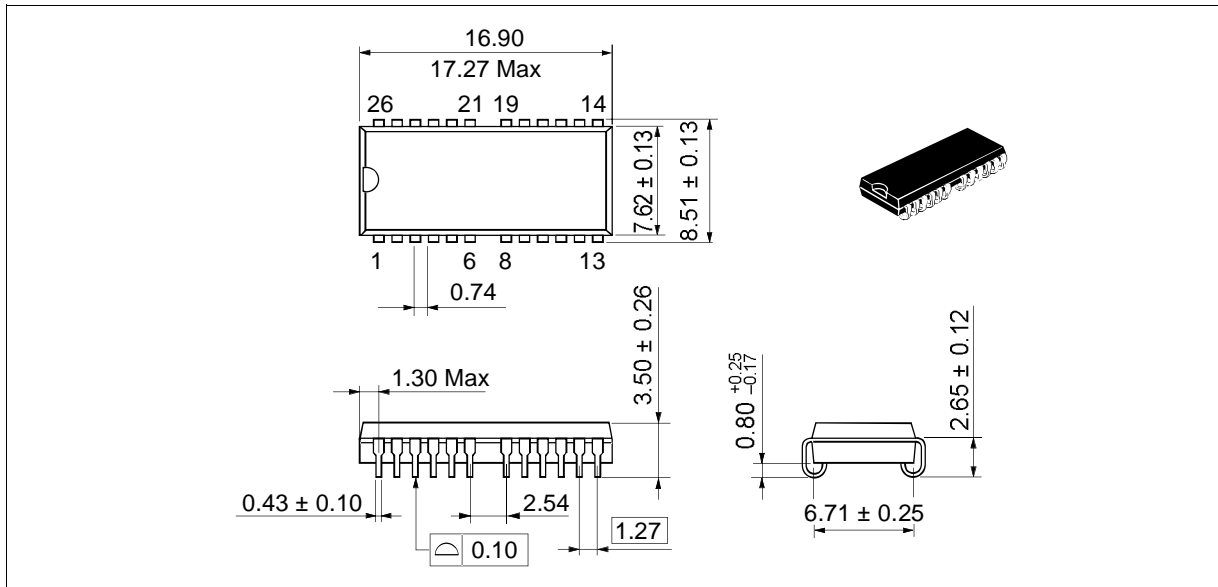


# HM5117400B Series

## Package Dimensions

HM5117400BS/BLS Series (CP-26/24DB)

Unit: mm



HM5117400BTS/BLTS Series (TTP-26/24DA)

Unit: mm

