16,384 Bit Serial Read Only Memory

FEATURES

- 2048 x 8 Bit ROM Organization
- Serial In/Parallel Out Shift Register
- Single Supply Voltage +5V
- Interfaced to SP0256
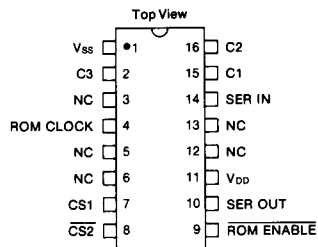- Totally Automatic Custom Programing

DESCRIPTION

The SPR016 is a serial Read Only Memory with 2048 x 8 bits of ROM. The data is addressed by an internal program counter (PC). The device also contains a serial in/parallel out shift register, which is used to assemble an address to be parallel loaded into the PC.

The device operates with a single supply (nominally +5V) which may be powered down when the system is inactive. When the SPR016 is interfaced to the SP0256 Speech Processor, the ROM enable input is used to avoid bus conflict on the serial out pin during the SPR016 power up.
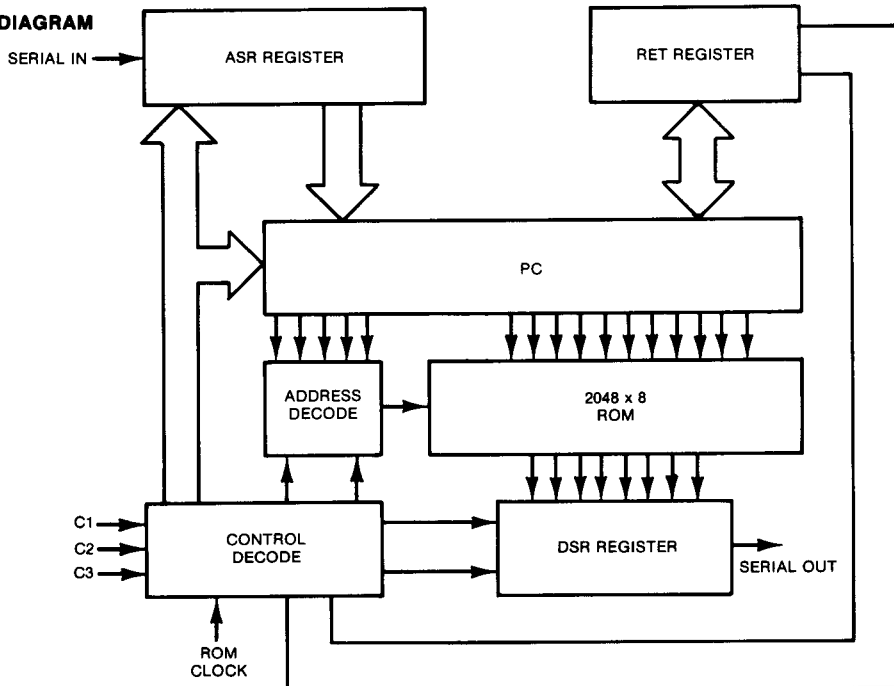
The SPR016 is constructed on a single monolithic chip utilizing the General Instrument low voltage N-Channel Ion Implant technology.

PIN CONFIGURATION
16 LEAD DUAL IN LINE

Top View

V_{SS}	1	16	C2
C3	2	15	C1
NC	3	14	SER IN
ROM CLOCK	4	13	NC
NC	5	12	NC
NC	6	11	V_{DD}
CS1	7	10	SER OUT
$\overline{CS2}$	8	9	$\overline{ROM\ ENABLE}$

BLOCK DIAGRAM

PIN ASSIGNMENTS (PRELIMINARY)

Pin Number	Name	Function
9	ROM ENABLE	Active low chip select used in system to eliminate bus conflict at system start-up. When brought high, ROM ENABLE Tri-States Serial Out.
14	SERIAL IN	Serial Input used to load 16 bit address into device.
10	SERIAL OUT	Output pin used to shift out data byte.
7	CS1	Active high chip select. Will Tri-State Serial output when low.
8	CS2	Active low chip select. Will Tri-State Serial output when high.
4	ROM CLOCK	1.56MHz clock input from SP0256 speech processor.
1	V_{SS}	Ground pin.
2 16 15	C3 C2 C1	Control pins decoded to determine device function.
11	V_{DD}	Positive supply pin (+4.6V to +7.0V).
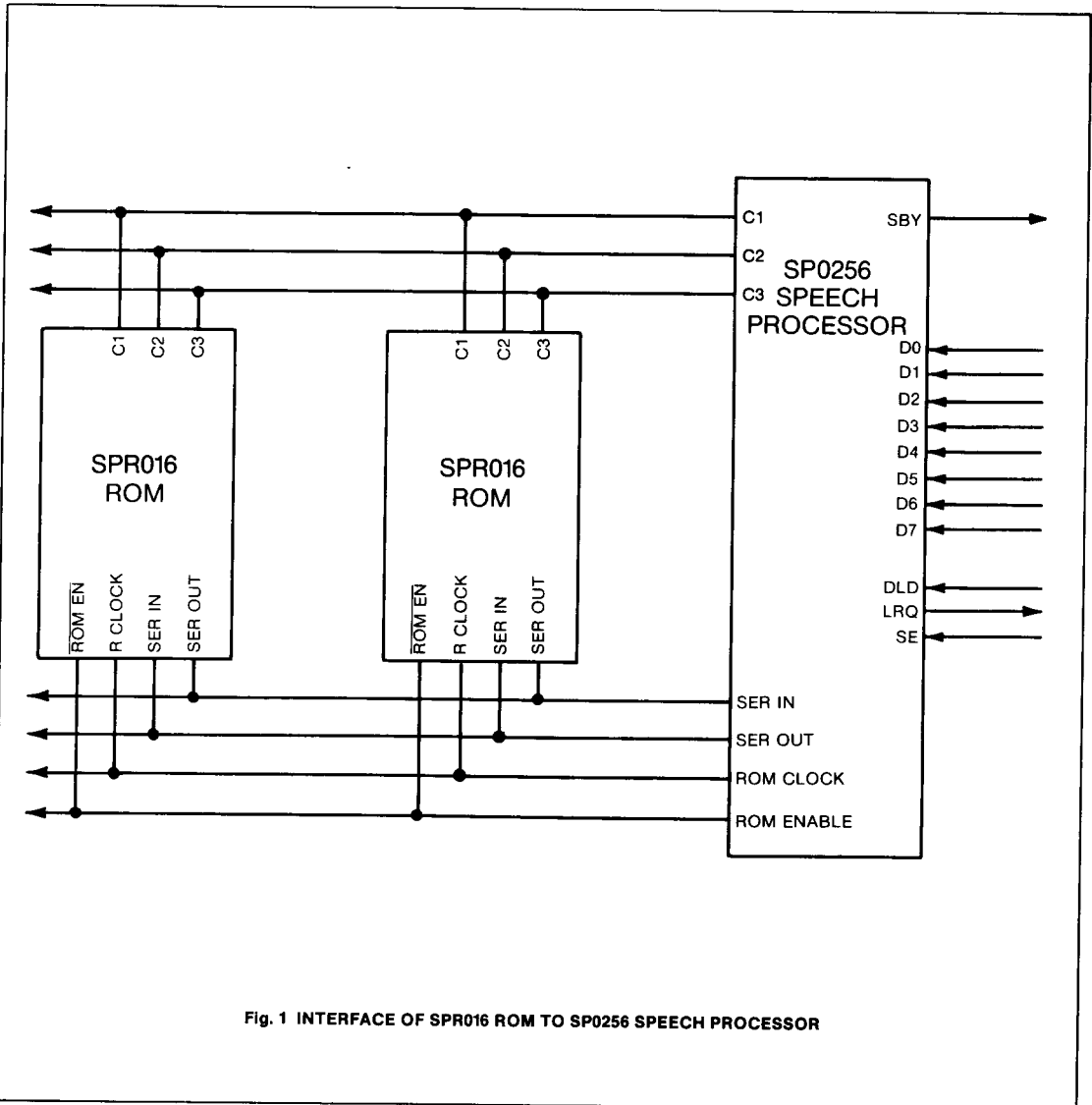
Fig. 1 INTERFACE OF SPR016 ROM TO SP0256 SPEECH PROCESSOR

TABLE 1 SPR016 CONTROL STATES

C1	C2	C3	Name	Function
0	0	0	NOP	No action taken
0	0	1	ASR Load	Accepts data from the serial input, synchronous to the externally supplied ROM clock. This data is shifted into the ASR holding register in preparation for loading into the PC. Although ASR is 16 bits long, it is not necessary to load all 16 bits of address sequentially in one ASR load.
0	1	0	PC Load	Loads the contents of the ASR register into the PC.
0	1	1	DSR Load	Loads the 8 bits of data pointed to by the present value of the least significant 11 bits of the PC into the data output shift register (DSR). At the completion of the DSR load the PC is incremented.
1	0	0	DSR Shift Out	Shifts out the contents of DSR to the serial out pin, synchronous to the ROM clock.
1	0	1	RET Register Load	Loads the return register (RET) with the current value of the PC
1	1	0	Return	Loads the PC with the contents of the RET register.
1	1	1	NOP	No Action Taken

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{DD} .... −.3 to +12V
Storage Temperature .... −25°C to +125°C
Lead Temperature (Soldering) 10 Sec .... +333°C

*Exceeding these ratings could cause permanent damage to this device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise noted):

V_{DD} = +4.6V to +7.0V
Operating Temperature = 0°C to +70°C

Supply Current

I_{DD} = 25mA V_{DD} = 7.0V   ROM clock frequency typically 1.56MHz
         V_{SS} = 0.0V T_A = 0°C

DC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Inputs ROM ENABLE, SERIAL IN, CS1, CS2, C1, C2, C3 ROM Clock						
Logic "0"	V_{IL}	0	—	0.6	V	
Logic "1"	V_{IH}	2.4	—	V_{DD}	V	
Capacitance	C_{IN}	—	—	10	pf	
Leakage	I_{LC}	—	—	10	µA	V_{PIN} = V_{DD} Volts, all others grounded
Outputs SERIAL OUT						
Logic "0"	V_{OL}	0	—	0.6	V	I_L = 1.6mA
Logic "1"	V_{OH}	2.5	—	V_{DD}	V	I_L = −50µA
Leakage	I_{LO}	—	—	10	µA	Output Tristated

AC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
ROM Clock Freq.	F	1.555	1.56	1.565	MHz	48% to 52% Duty Cycle Positive
Output Enable Delay Time from RE, CS1, CS2	t_{OE}	—	—	120	ns	Independent of ROM Clock
Output Disable Delay Time from CS1, RE, CS2	t_{OD}	—	—	120	ns	
Serial In Set Up Time	t_{SPIN}	120	—	—	ns	
Control Bus Set Up Time	t_{CIN}	180	—	—	ns	
Serial Output Access Time	t_{ACC}	—	—	360	ns	
Address Select Access Time	t_{AS}	—	—	8T + 120	ns	Note 1
Address Deselect Access Time	t_{AD}	—	—	8T + 120	ns	Note 1

NOTE:
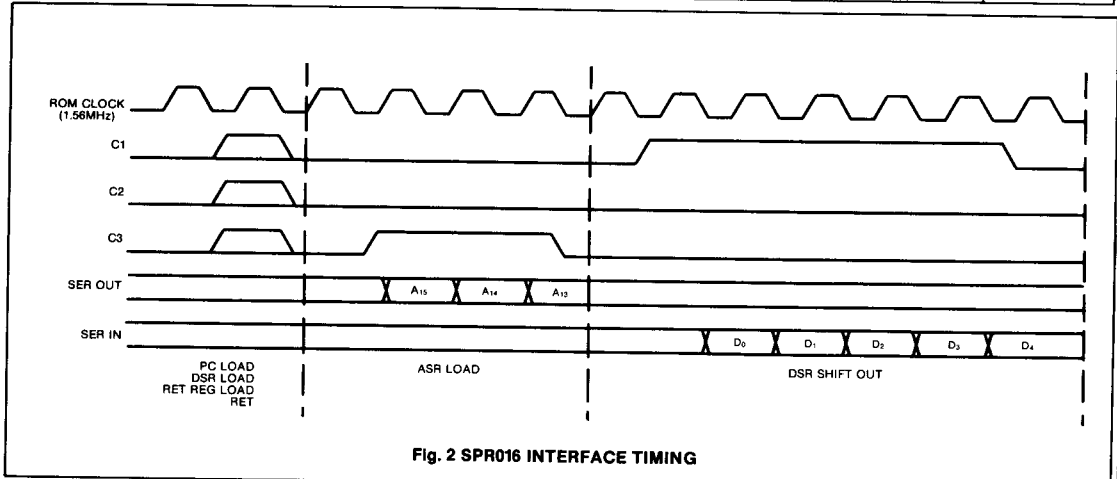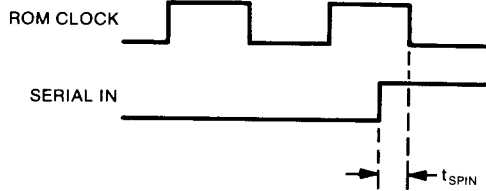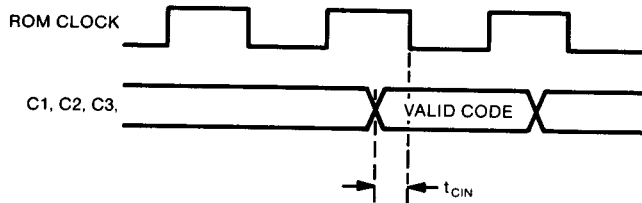1. T is the cycle time, in nanoseconds of the ROM clock input.
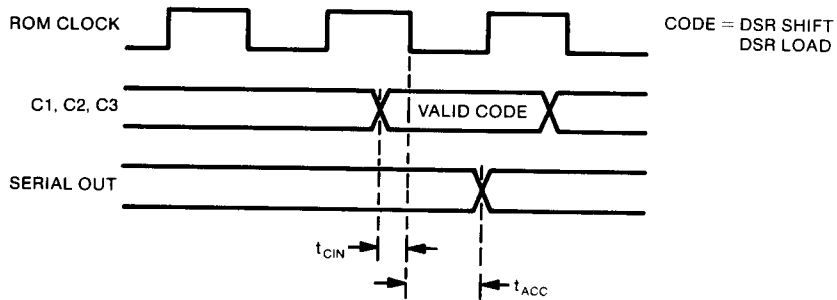
Fig. 2 SPR016 INTERFACE TIMING

SERIAL IN SETUP TIME

CONTROL BUS SETUP TIME

SERIAL OUT ACCESS TIME
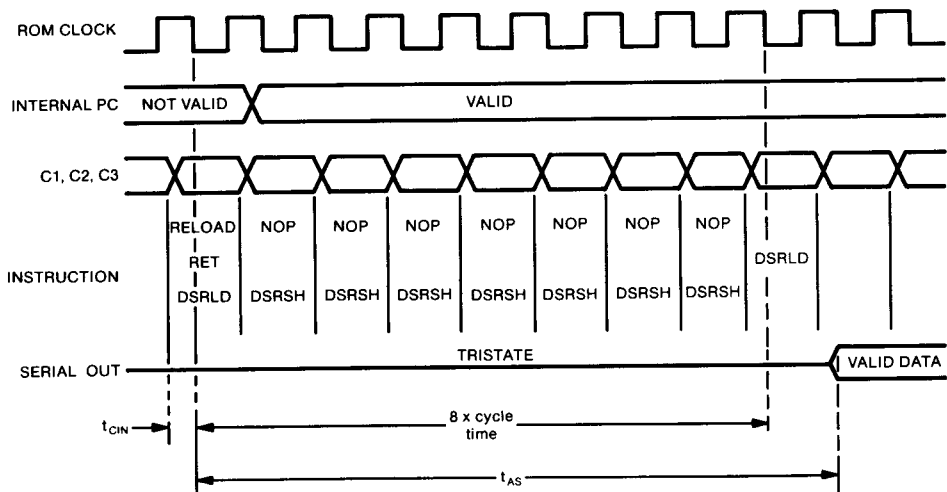
READ ONLY MEMORY

OUTPUT ENABLE RELAY TIME

ROM ENABLE, $\overline{CS2}$

CS1

SERIAL OUT

TRISTATE

VALID DATA

t_{OE}
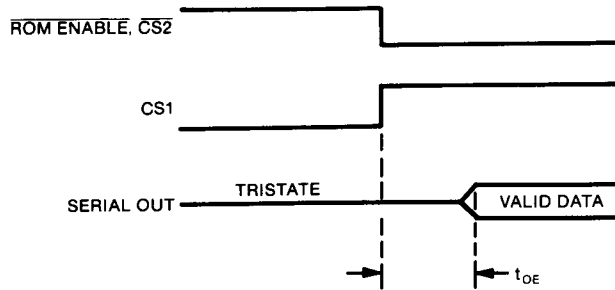
OUTPUT DISABLE RELAY TIME

ROM ENABLE, $\overline{CS2}$

CS1

SERIAL OUT

VALID DATA

TRISTATE

t_{OD}

ADDRESS SELECT ACCESS TIME

ROM CLOCK

INTERNAL PC   NOT VALID   VALID

C1, C2, C3

INSTRUCTION

RELOAD	NOP	NOP	NOP	NOP	NOP	NOP	NOP		DSRLD
RET									
DSRLD	DSRSH	DSRSH	DSRSH	DSRSH	DSRSH	DSRSH	DSRSH		

SERIAL OUT

TRISTATE

VALID DATA

t_{CIN}

8 x cycle
time
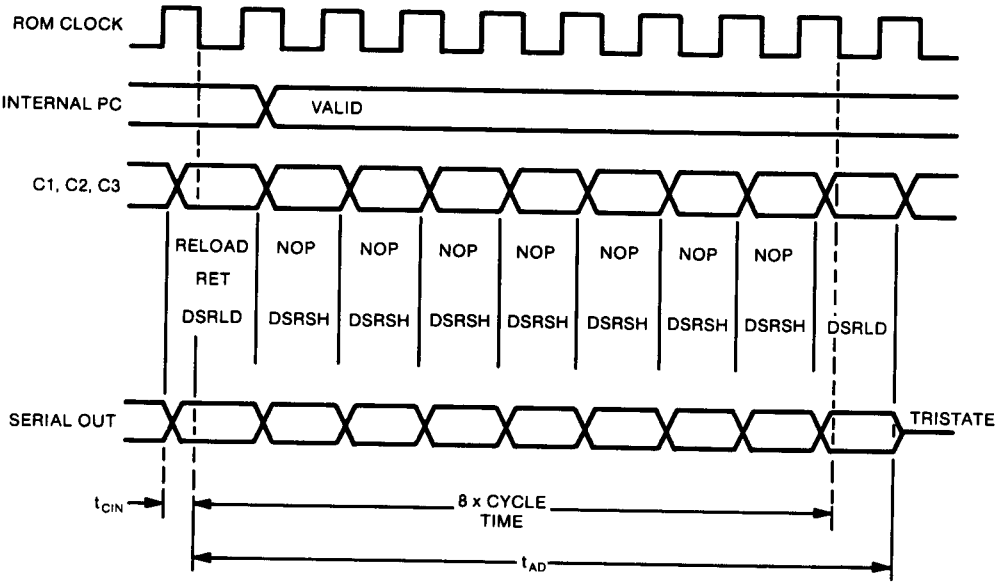
t_{AS}

ADDRESS DE-SELECT TIME

READ ONLY MEMORY