1.8V CMOS 16-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

IDT74AUC16373

FEATURES:

- **ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)**
- **1.8V Optimized**
- **0.8V to 2.7V Operating Range**
- **Inputs/outputs tolerant up to 3.6V**
- **Output drivers: ±9mA @ 2.3V**
- **Supports hot insertion**
- **Available in TSSOP, TVSOP, and VFBGA packages**

APPLICATIONS:

- **high performance, low voltage communications systems**
- **high performance, low voltage computing systems**

DESCRIPTION:

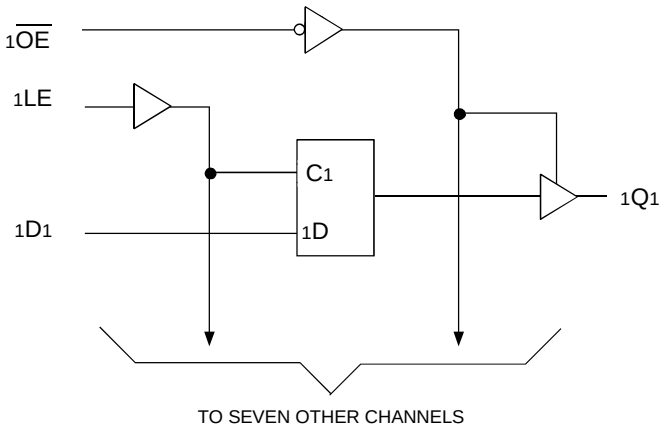
This 16-bit transparent D-type latch is built using advanced CMOS technology. The device can be used as a single 16-bit latch or as two 8-bit latches. When the latch enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

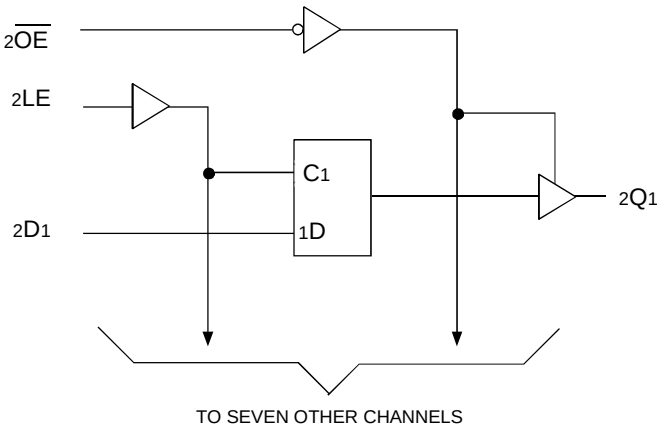
A buffered output enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The $\overline{OE}$ input does not affect the internal operation of the latch.

This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{DD} through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTIONAL BLOCK DIAGRAM





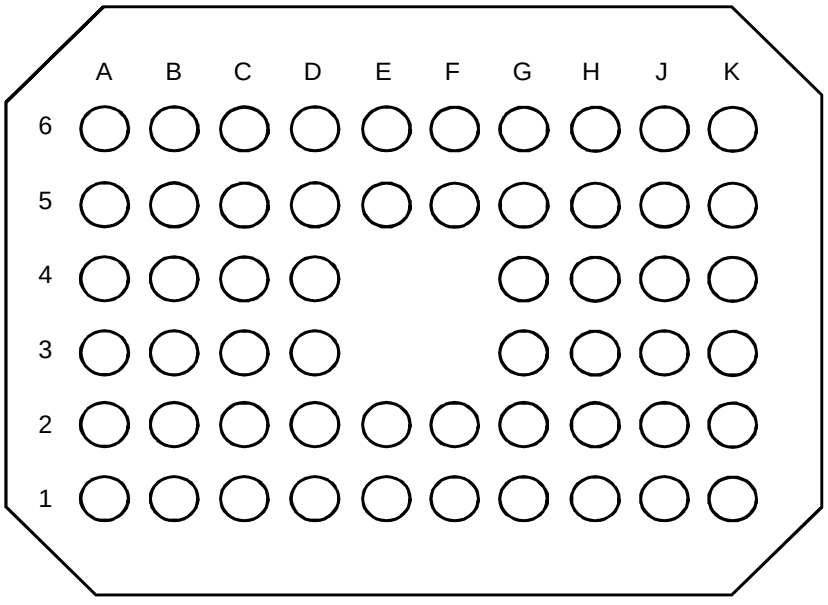
PINOUT CONFIGURATION

	A	B	C	D	E	F	G	H	J	K
6	1LE	1D2	1D4	1D6	1D8	2D1	2D3	2D5	2D7	2LE
5	NC	1D1	1D3	1D5	1D7	2D2	2D4	2D6	2D8	NC
4	NC	GND	V_{DD}	GND			GND	V_{DD}	GND	NC
3	NC	GND	V_{DD}	GND			GND	V_{DD}	GND	NC
2	NC	1Q1	1Q3	1Q5	1Q7	2Q2	2Q4	2Q6	2Q8	NC
1	$1\overline{OE}$	1Q2	1Q4	1Q6	1Q8	2Q1	2Q3	2Q5	2Q7	$2\overline{OE}$

VFBGA

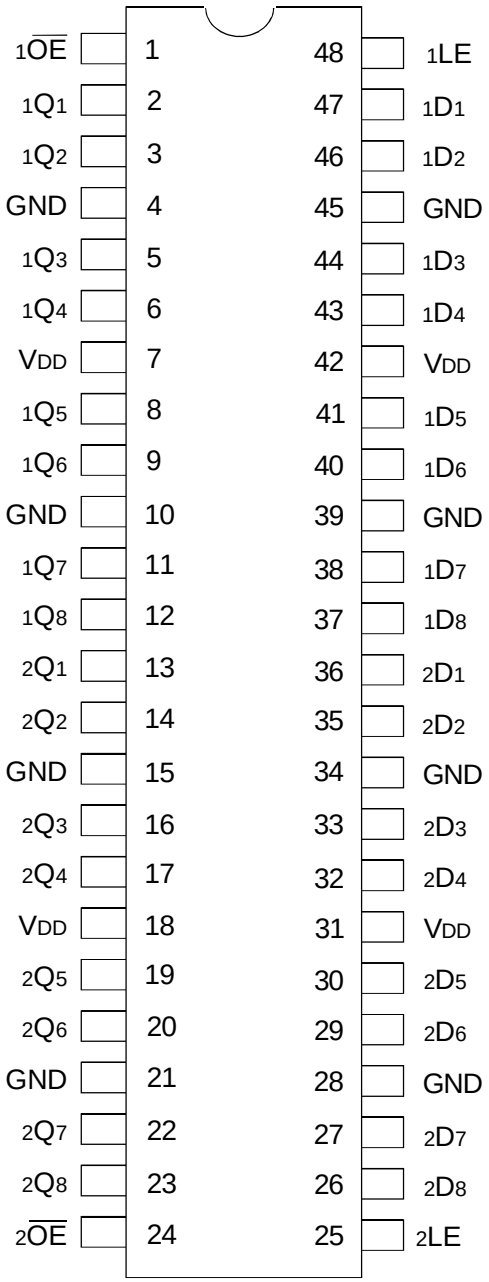
NOTE:
NC = No Internal Connection

56 BALL VFBGA PACKAGE LAYOUT



TOP VIEW

PIN CONFIGURATION



TSSOP/ TVSOP
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
xDx	Data Inputs
xLE	Latch Enable Inputs
xQx	3-State Outputs
$x\overline{OE}$	3-State Output Enable Inputs (Active LOW)

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V_{TERM}	Terminal Voltage with Respect to GND (all input and V_{DD} terminals)	–0.5 to +3.6	V
V_{TERM}	Terminal Voltage with Respect to GND (any I/O or Output terminals in high-impedance or power-off state)	–0.5 to +3.6	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	Continuous DC Output Current	±20	mA
I_{IK}	Continuous Clamp Current, $V_I < 0$, or $V_I > V_{DD}$	±50	mA
I_{OK}	Continuous Clamp Current, $V_O < 0$	–50	mA
I_{DD} I_{SS}	Continuous Current through each V_{DD} or GND	±100	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz, V_{DD} = 2.5V)

Symbol	Parameter	Conditions	Typ.	Max.	Unit
C_{IN}(1)	Input Capacitance	V_{IN} = 0V	3	4	pF
C_{OUT}(2)	Output Capacitance	V_{OUT} = 0V	5.5	6.5	pF
C_I(3)	Input Port Capacitance	V_{IN} = 0V	3	4	pF

NOTES:
1. Applies to Control Inputs.
2. Applies to Data Outputs.
3. Applies to Data Inputs.

FUNCTION TABLE (EACH 8-BIT LATCH)(1)

Inputs			Output
$x\overline{OE}$	xLE	xDx	xQx
L	H	H	H
L	H	L	L
L	L	X	Q(2)
H	X	X	Z

NOTES:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-Impedance
2. Level of Q before the indicated steady-state conditions were established.

RECOMMENDED OPERATING CHARACTERISTICS(1)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{DD}	Supply Voltage		0.8	2.7	V
V_{IH}	Input HIGH Voltage Level	V_{DD} = 0.8V	V_{DD}	—	V
		V_{DD} = 1.1V to 1.3V	0.65 x V_{DD}	—	
		V_{DD} = 1.4V to 1.6V	0.65 x V_{DD}	—	
		V_{DD} = 1.65V to 1.95V	0.65 x V_{DD}	—	
		V_{DD} = 2.3V to 2.7V	1.7	—	
V_{IL}	Input LOW Voltage Level	V_{DD} = 0.8V	—	0	V
		V_{DD} = 1.1V to 1.3V	—	0.35 x V_{DD}	
		V_{DD} = 1.4V to 1.6V	—	0.35 x V_{DD}	
		V_{DD} = 1.65V to 1.95V	—	0.35 x V_{DD}	
		V_{DD} = 2.3V to 2.7V	—	0.7	
V_I	Input Voltage		0	2.7	V
V_O	Output Voltage	Active State	0	V_{DD}	V
		3-State	0	2.7	
I_{OH}	HIGH Level Output Current	V_{DD} = 0.8V	—	–0.7	mA
		V_{DD} = 1.1V	—	–3	
		V_{DD} = 1.4V	—	–5	
		V_{DD} = 1.65V	—	–8	
		V_{DD} = 2.3V	—	–9	
I_{OL}	LOW Level Output Current	V_{DD} = 0.8V	—	0.7	mA
		V_{DD} = 1.1V	—	3	
		V_{DD} = 1.4V	—	5	
		V_{DD} = 1.65V	—	8	
		V_{DD} = 2.3V	—	9	
$\Delta t/\Delta v$	Input Transition Rise or Fall Time		—	20	ns/V
T_A	Operating Free-Air Temperature		–40	+85	°C

NOTE:
1. All unused inputs of the device must be held at V_{DD} or GND to ensure proper operation.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE(1)

Following Conditions Apply Unless Otherwise Specified:
Operating Conditions: T_A = –40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
I_{IH} I_{IL}	Input HIGH or LOW Current All Inputs	V_{DD} = 2.7V, V_I = V_{DD} or GND		—	—	±5	µA
I_{OFF}	Input/Output Power Off Leakage	V_{DD} = 0V, V_{IN} or $V_O \leq$ 2.7V		—	—	±10	µA
I_{OZH}	High Impedance Output Current	V_{DD} = 2.7V	V_O = V_{DD}	—	—	±10	µA
I_{OZL}	(3-State Output Pins)		V_O = GND	—	—	±10	
I_{DDL} I_{DDH} I_{DDZ}	Quiescent Power Supply Current	V_{DD} = 0.8V to 2.7V V_{IN} = GND or V_{DD}		—	—	20	µA

NOTE:
1. All unused inputs of the device must be held at V_{DD} or GND to ensure proper operation.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = 0.8V - 2.7V	I_{OH} = –100µA	V_{DD} - 0.1	—	—	V
		V_{DD} = 0.8V	I_{OH} = –0.7mA	—	0.55	—	
		V_{DD} = 1.1V[2]	I_{OH} = –3mA	0.8	—	—	
		V_{DD} = 1.4V[3]	I_{OH} = –5mA	1	—	—	
		V_{DD} = 1.65V[4]	I_{OH} = –8mA	1.2	—	—	
		V_{DD} = 2.3V[5]	I_{OH} = –9mA	1.8	—	—	
V_{OL}	Output LOW Voltage	V_{DD} = 0.8V - 2.7V	I_{OH} = 100µA	—	—	0.2	V
		V_{DD} = 0.8V	I_{OL} = 0.7mA	—	0.25	—	
		V_{DD} = 1.1V[2]	I_{OL} = 3mA	—	—	0.3	
		V_{DD} = 1.4V[3]	I_{OL} = 5mA	—	—	0.4	
		V_{DD} = 1.65V[4]	I_{OL} = 8mA	—	—	0.45	
		V_{DD} = 2.3V[5]	I_{OH} = 9mA	—	—	0.6	

NOTES:
1. V_{IL} and V_{IH} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS table for the appropriate V_{DD} range. T_A = -40°C to +85°C.
2. Demonstrates operation for nominal V_{DD} = 1.2V.
3. Demonstrates operation for nominal V_{DD} = 1.5V.
4. Demonstrates operation for nominal V_{DD} = 1.8V.
5. Demonstrates operation for nominal V_{DD} = 2.5V.

OPERATING CHARACTERISTICS, T_A = 25°C

Symbol	Parameter	Test Conditions	V_{DD} = 0.8V	V_{DD} = 1.2V	V_{DD} = 1.5V	V_{DD} = 1.8V	V_{DD} = 2.5V	Unit
C_{PD}	Power Dissipation Capacitance Outputs Enabled	C_L = 0pF f = 10MHz	21	22	23	25	29	pF
C_{PD}	Power Dissipation Capacitance Outputs Disabled		5	5	6	7	10	pF

SWITCHING CHARACTERISTICS[1]

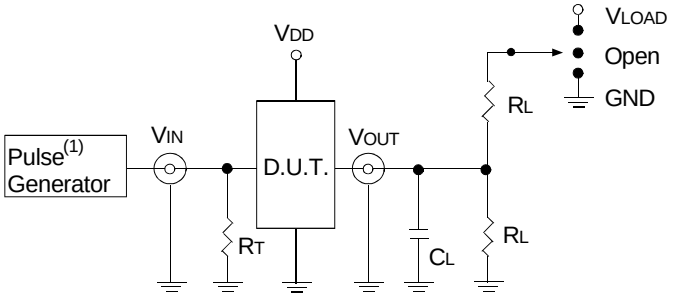
Symbol	Parameter		V_{DD} = 0.8V	V_{DD} = 1.2V±0.1V		V_{DD} = 1.5V±0.1V		V_{DD} = 1.8V±0.15V			V_{DD} = 2.5V±0.2V		Unit
			Typ.	Min.	Max.	Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay	xDx to xQx	8	1.1	3.8	0.6	2.4	0.7	1.5	2.4	0.6	1.9	ns
t_{PHL}		xLE to xQx	10.6	1.4	4.9	0.7	3.2	0.7	1.6	2.8	0.6	2.1	
t_{PZH} t_{PZL}	Output Enable Time $x\overline{OE}$ to xQx		9	1.3	4.5	0.6	2.9	0.8	1.7	2.9	0.7	2.2	ns
t_{PHZ} t_{PLZ}	Output Disable Time $x\overline{OE}$ to xQx		13	2.4	7	2.4	4.8	1.1	2.7	4.6	0.4	2.5	ns
t_{SU}	Set-up Time, Data before LE↓		1.7	0.7	—	0.5	—	0.4	—	—	0.4	—	ns
t_H	Hold Time, Data after LE↓		—	1.2	—	0.8	—	0.7	—	—	0.6	—	ns
t_W	Pulse Duration, LE HIGH		4.2	2.9	—	2.3	—	2.1	—	—	1.7	—	ns

NOTE:
1. See TEST CIRCUITS AND WAVEFORMS. T_A = -40°C to +85°C.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS(1)

Symbol	V_{DD} = 0.8V	V_{DD} = 1.2V±0.1V	V_{DD} = 1.5V±0.1V	V_{DD} = 1.8V±0.15V	V_{DD} = 2.5V±0.2V	Unit
V_{LOAD}	2xV_{DD}	2xV_{DD}	2xV_{DD}	2xV_{DD}	2xV_{DD}	V
V_T	V_{DD}/2	V_{DD}/2	V_{DD}/2	V_{DD}/2	V_{DD}/2	V
V_{LZ}	100	100	100	150	150	mV
V_{HZ}	100	100	100	150	150	mV
R_L	2	2	2	1	0.5	KΩ
C_L	15	15	15	30	30	pF

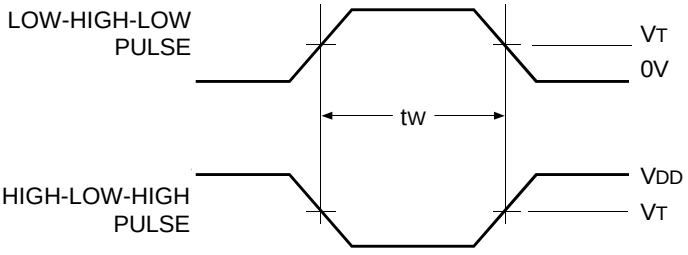


Test Circuits for All Outputs

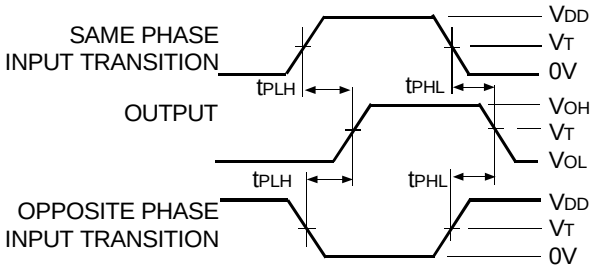
DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.
NOTE:
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; Slew Rate ≥ 1V/ns.

SWITCH POSITION

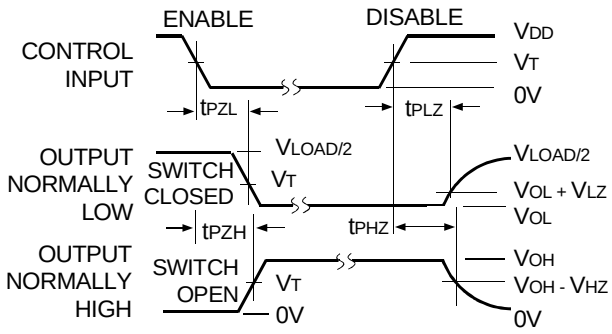
Test	Switch
Open Drain Disable Low Enable Low	V_{LOAD}
Disable High Enable High	GND
All Other Tests	Open



Pulse Width

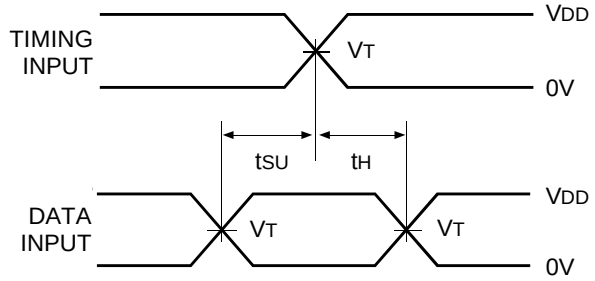


Propagation Delay



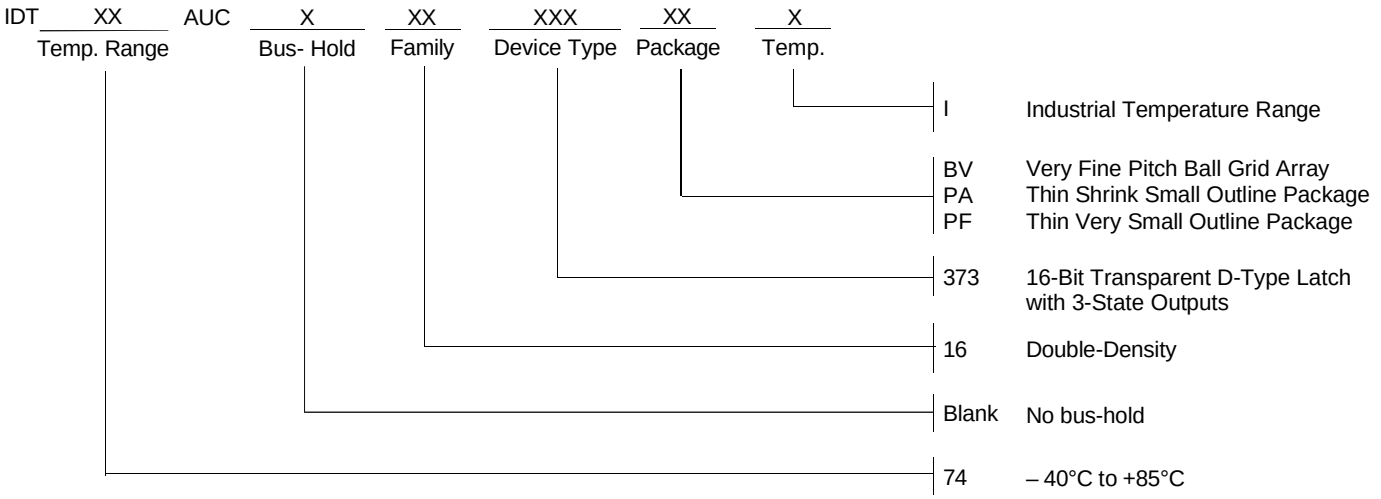
NOTE:
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

Enable and Disable Times



Setup and Hold Times

ORDERING INFORMATION



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