Preliminary

SPF-3043

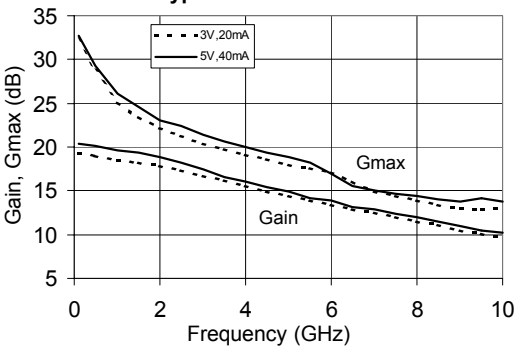
Low Noise pHEMT GaAs FET

Qualification Pending April 2001

Product Description

Stanford Microdevices' SPF-3043 is a high performance 0.25µm pHEMT Gallium Arsenide FET. This 300µm device is ideally biased at 3V,20mA for lowest noise performance and battery powered requirements. At 5V,40mA the device delivers excellent OIP3 of 32dBm. It provides ideal performance as a driver stage in many commercial and industrial LNA applications.

Typical Gain Performance



Product Features

- **DC-10 GHz Operation**
- **Ultra Low NF: 0.25 dB @ 1 GHz, 0.50 dB @ 2 GHz**
- **High Assoc. Gain: 25 dB @ 1 GHz, 22 dB @ 2 GHz**
- **Low Current Draw for NFopt (3V,20mA)**
- **+32 dBm OIP3, +20 dBm P1dB (5V,40mA)**
- **Low Cost High Performance pHEMT**

Applications

- **LNA for Wireless Infrastructure**
- **Fixed Wireless Infrastructure**
- **Wireless Data**
- **Driver Stage for Low Power Applications**

Symbol	Device Characteristics, T = 25ºC V_{DS}=3V, I_{DS}=20mA (unless otherwise noted)		Units	Min.	Typ.	Max.
G_{MAX}	Maximum Available Gain $Z_S=Z_S^*$, $Z_L=Z_L^*$	f = 0.9 GHz f = 1.9 GHz	dB		25.5 22.4	
S_{21}	Insertion Gain $Z_S=Z_L=50\Omega$	f = 0.9 GHz f = 1.9 GHz	dB		18.5 18.0	
NF_{min}	Minimum Noise Figure $Z_S=\Gamma_{OPT}$, $Z_L=Z_L^*$	f = 0.9 GHz f = 1.9 GHz	dB		0.25 0.50	
P1dB	Output 1 dB compression point $Z_S=Z_{SOPT}$, $Z_L=Z_{LOPT}$	V_{DS}=3V, I_{DS}=20 mA V_{DS}=5V, I_{DS}=40 mA	dBm		15.5 20	
OIP_3	Output Third Order Intercept Point $Z_S=Z_{SOPT}$, $Z_L=Z_{LOPT}$	V_{DS}=3V, I_{DS}=20 mA V_{DS}=5V, I_{DS}=40 mA	dBm		29 32	
V_P	Pinchoff Voltage	V_{DS}= 2V, I_{DS}= 0.1 mA	V	-1.1	-0.8	-0.5
I_{DSS}	Saturated Drain Current	V_{DS}= 2V, V_{GS} = 0V	mA	45	67.5	100
g_{mp}	Peak Transconductance	V_{DS}= 2V, V_{GS} @ g_{mp}	mS	100	150	
BV_{GSO}	Gate-to-Source Breakdown Voltage	I_G= 0.03 mA Drain Open, Source Grounded	V		-10	-8
BV_{GDO}	Gate-to-Drain Breakdown Voltage	I_G= 0.03 mA Source Open, Drain Grounded	V		-10	-8
Rth	Thermal Resistance (junction to lead)		ºC/W		150	

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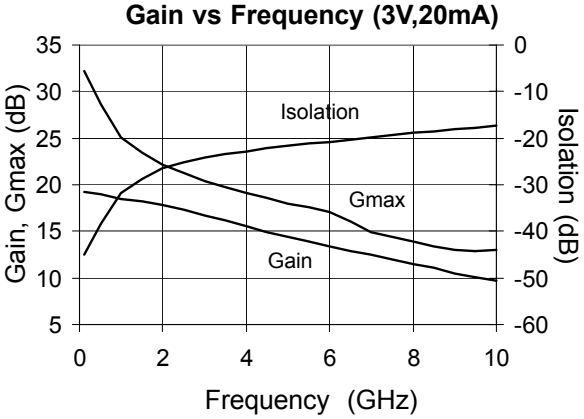
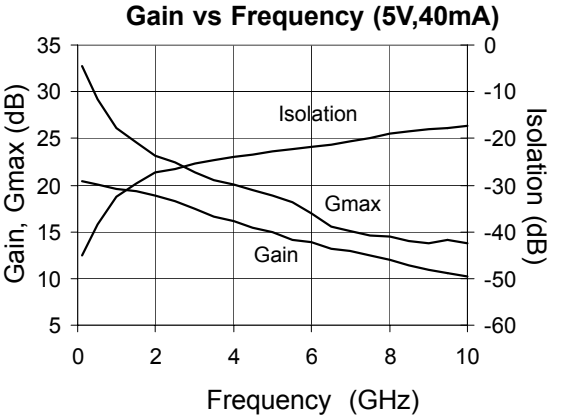
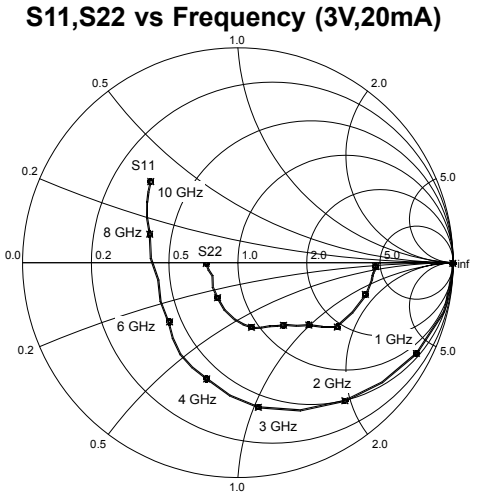
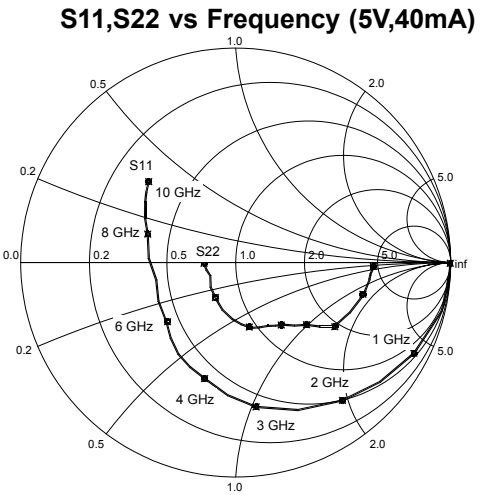
Typical Performance









Note: S-parameters are de-embedded to the device leads with $Z_S=Z_L=50\Omega$. The data represents typical performace of the device. De-embedded s-parameters can be downloaded from our website (www.stanfordmicro.com).

Typical Performance

Freq (MHz)	V_{DS} (V)	I_{DS} (mA)	Fmin (dB)	Γ_{OPT} Mag ∠ Ang	r_N	Gmax (dB)	P1dB (dBm)	OIP3 (dBm)
900	3	20	0.25	0.79 ∠ 12	0.22	25.5	15.5	29
	5	40	0.32	0.75 ∠ 12	0.25	26.5	20.0	32
1900	3	20	0.50	0.62 ∠ 34	0.19	22.4	15.5	29
	5	40	0.54	0.62 ∠ 33	0.20	23.3	20.0	32

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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain Current	I_{DS}	150	mA
Forward Gate Current	I_{GS}	2	mA
Drain-to-Source Voltage	V_{DS}	7	V
Gate-to-Source Voltage	V_{GS}	-3	V
RF Input Power	P_{IN}	15	dBm
Operating Temperature	T_{OP}	-40 to +85	C
Storage Temperature Range	T_{stor}	-40 to +150	C
Power Dissipation	P_{DISS}	430	mW
Operating Junction Temperature	T_J	+150	C

Caution: ESD sensitive
Appropriate precautions in handling, packaging and testing devices must be observed.

Part Number Ordering Information

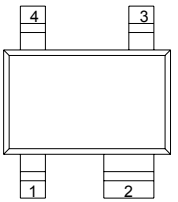
Part Number	Reel Size	Devices/Reel
SPF-3043	7"	3000

Part Symbolization

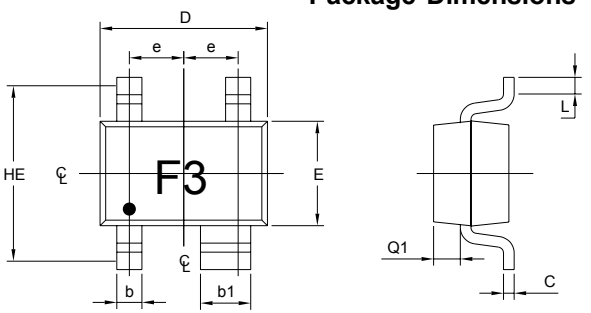
The part will be symbolized with an “F3” and a Pin 1 indicator on the top surface of the package.

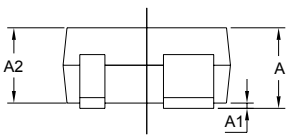
Pin Description

Pin #	Function	Description
1	Gate	RF Input
2	GND & Source	Connection to ground. Use via holes to reduce lead inductance. Place vias as close to ground leads as possible.
3	Drain	RF Output
4	GND & Source	Same as Pin 2



Package Dimensions





NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS ARE INCLUSIVE OF PLATING.
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. ALL SPECIFICATIONS COMPLY TO EIAJ SC70.
5. DIE IS FACING UP FOR MOLD AND FACING DOWN FOR TRIM/FORM. ie :REVERSE TRIM/FORM.
6. PACKAGE SURFACE TO BE MIRROR FINISH.

SYMBOL	MIN	MAX
E	1.15	1.35
D	1.85	2.25
HE	1.80	2.40
A	0.80	1.10
A2	0.80	1.00
A1	0.00	0.10
Q1	0.10	0.40
e	0.65 BSC	
b	0.25	0.40
b1	0.55	0.70
c	0.10	0.18
L	0.10	0.30

Use multiple plated-through vias holes located close to the package pins to ensure a good RF ground connection to a continuous groundplane on the backside of the board.