3.3 V 3.2 Gb/s Limiting Amplifier

PRELIMINARY TECHNICAL DATA

ADN2891

FEATURES

SFP reference design available
Input sensitivity: 4 mV p-p
80 ps rise/fall times
CML outputs: 700 mV p-p differential
Programmable LOS detector: 3mV to 40 mV
Rx signal strength indicator (RSSI):
SFF-8472 compliant average power measurement
Single-supply operation: 3.3 V
Low power dissipation: 145 mW
Available in space-saving 3 mm × 3 mm 16-lead LFCSP
Extended Temperature Range: -40°C to 95°C

APPLICATIONS

SFP/SFF/GBIC optical transceivers
OC-3/12/48, GbE, Fibre Channel receivers
10GBASE-LX4 transceivers
WDM transponders

GENERAL DESCRIPTION

The ADN2891 limiting amplifier works as a data quantizer optimized for SONET, Gigabit Ethernet (GbE), and Fibre Channel optical receivers in the range of 155Mpbs and up to 3.2Gbps . It accepts input levels of up to 2.0 V p-p differential with 4mV p-p differential input sensitivity and outputs current mode logic (CML) voltages with controlled edge speeds..

The ADN2891 measures average received power based on a direct measurement of the photodiode current with better than 1 dB of accuracy over the entire input range of the receiver. This eliminates the need for external RSSI detection circuitry in SFF-8472 compliant optical transceivers.

Additional features includes a programmable loss-of-signal (LOS) detect and output Squelch.

The ADN2891 limiting amplifier operates from a single 3.3 V supply, has low power dissipation, and is available in a 3 mm × 3 mm 16-lead lead frame chip scale package (LFCSP).

FUNCTIONAL BLOCK DIAGRAM

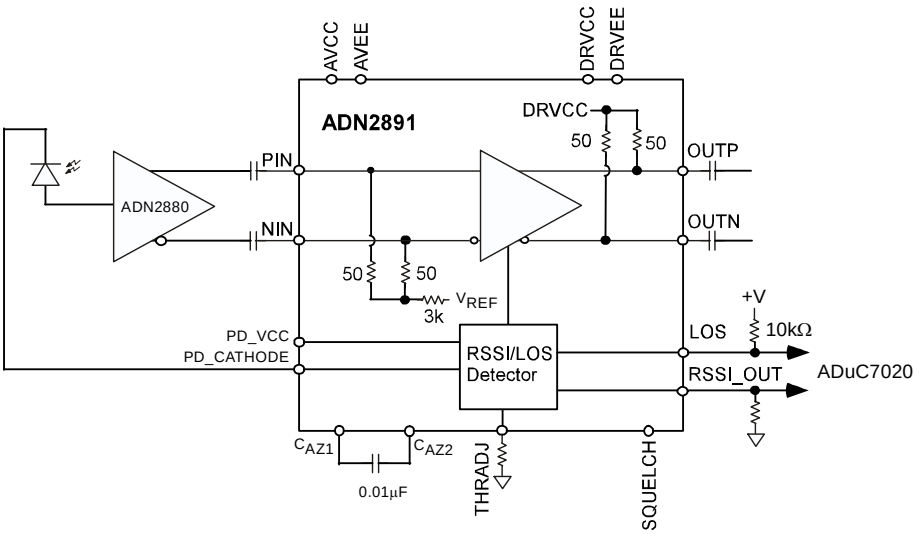

Figure 1. ADN2891 Typical Application Circuit

Rev. PrA.

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REVISION HISTORY

Revision PrA: Initial Version

SPECIFICATIONS

Table 1. Test Conditions: VCC = 3.0V to 3.6V, VEE = 0 V, T_A = -40 °C to 95 °C, unless otherwise noted.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
QUANTIZER DC CHARACTERISTICS					
Input Voltage Range	1.8		2.8	V p-p	@ PIN or NIN, dc-coupled
Input Common Mode	2.1		2.7	V	DC-coupled
Peak-to-Peak Differential Input Range			2.0	V p-p	PIN – NIN, ac-coupled
Input Sensitivity	4	3		mV p-p	PIN – NIN, BER $\leq 1 \times 10^{-10}$
Input Offset Voltage		100		µV	
Input RMS Noise		205		µV rms	
Input Resistance		50		Ω	Single-ended
Input Capacitance		0.65		pF	
QUANTIZER AC CHARACTERISTICS					
Input Data Rate	155		3200	Mb/s	
Small Signal Gain		51		dB	Differential
S11		–10		dB	Differential, f < 3.2 GHz
S22		–10		dB	Differential, f < 3.2 GHz
Random Jitter		2.4	5	ps rms	Input ≥ 10 mV p-p, OC-48, PRBS $2^{23} – 1$
Deterministic Jitter		13.7	19	ps p-p	Input ≥ 10 mV p-p, OC-48, PRBS $2^{23} – 1$
Low Frequency Cutoff		30		kHz	CAZ = Open
		1.0		kHz	CAZ = 0.0 1 µF
Power Supply Rejection		45		dB	100 kHz < f < 10 MHz
LOSS OF SIGNAL DETECTOR (LOS)					
LOS Assert Level	TBD	2.0	TBD	mV p-p	R_{THRADJ} = 1MΩ
	TBD	40	TBD	mV p-p	R_{THRADJ} = 500 Ω
Hysteresis		3.0	TBD	dB	OC-3, PRBS $2^{23} – 1$, R_{THRADJ} = 500 Ω
	TBD	3.0		dB	OC-3, PRBS $2^{23} – 1$, R_{THRADJ} = 1MΩ
		4.5	TBD	dB	OC-48, PRBS $2^{23} – 1$, R_{THRADJ} = 500 Ω
	TBD	4.5		dB	OC-48, PRBS $2^{23} – 1$, R_{THRADJ} = 1M Ω
LOS Assert Time		600		ns	DC-coupled
LOS De-Assert Time		100		ns	DC-coupled
RSSI					
Input Current Range	5		1000	µA	
RSSI Output Accuracy			15%		$I_{IN} \leq 20$ µA
			10%		$I_{IN} > 20$ µA
Gain		1.0		mA/mA	I_{RSSI}/I_{PD}
Offset		50		nA	
Compliance Voltage	V_{CC} – 0.9		V_{CC} – 0.3	V	@ PD_CATHODE
POWER SUPPLIES					
V_{CC}	3.0	3.3	3.6	V	
I_{CC}		44	60	mA	
OPERATING TEMPERATURE RANGE	–40	+25	+95	°C	T_{MIN} to T_{MAX}
CML OUTPUT CHARACTERISTICS					
Output Impedance		50		Ω	Single-ended
Output Voltage Swing	600	700	800	V p-p	Differential
Output Rise and Fall Time		80	100	ps	20% to 80%
LOGIC INPUTS (SQUELCH)					
V_{IH}, Input High Voltage	2.0			V	
V_{IL}, Input Low Voltage			0.8	V	
Input Current	–100			nA	I_{INH}, V_{IN} = 2.4 V
			100	nA	I_{INL}, V_{IN} = 0.4 V

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC OUTPUTS (LOS)					
V_{OH}, Output High Voltage	2.4			V	Open drain output, 4.7 kΩ – 10 kΩ pull-up resistor to V_{CC}
V_{OL}, Output Low Voltage			0.4	V	Open drain output, 4.7 kΩ – 10 kΩ pull-up resistor to V_{CC}

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	4.2 V
Minimum Input Voltage (All Inputs)	VEE – 0.4 V
Maximum Input Voltage (All Inputs)	VCC + 0.4 V
Storage Temperature	–65°C to +155°C
Operating Temperature Range	–40°C to +95°C
Lead Temperature Range (Soldering 10 s)	300°C
Junction Temperature	125°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for 4-layer PCB with exposed paddle soldered to GND.

Table 3.

Package Type	θ_{JA}	Unit
16-lead 3 mm × 3 mm LFCSP	28	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

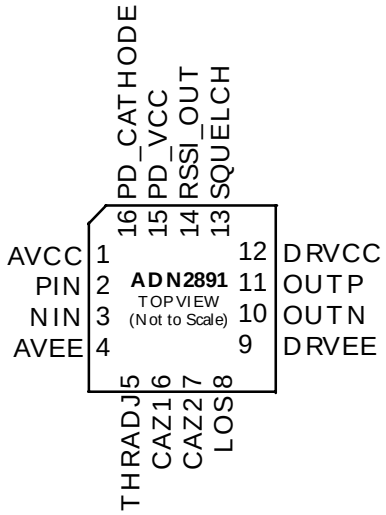

Figure 2. Pin Configuration

Note: There is an exposed pad on the bottom of the package that must be connected to the GND plane with filled vias.

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	I/O	Description
1	AVCC	Power	Analog Power
2	PIN	Input	Differential Data Input
3	NIN	Input	Differential Data Input
4	AVEE	Power	Analog Ground
5	THRADJ	Input	LOS Threshold Adjust Resistor
6	CAZ1		Offset Correction Loop Capacitor
7	CAZ2		Offset Correction Loop Capacitor
8	LOS	Output	LOS Detector Output
9	DRVEE	Power	Output Buffer Ground
10	OUTN	Output	Differential Data Output
11	OUTP	Output	Differential Data Output
12	DRVCC	Power	Output Buffer Power
13	SQUELCH	Input	Disable Outputs
14	RSSI_OUT	Output	Average Current Output
15	PD_VCC	Power	Power Input for RSSI Measurement
16	PD_CATHODE	Output	Photodiode Bias Voltage
Exposed Pad	Pad	Power	Connect to Ground

TYPICAL PERFORMANCE CHARACTERISTICS

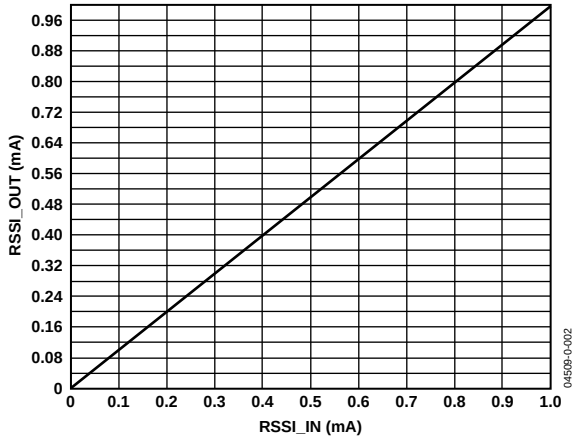

Figure 3. RSSI Output vs. Average PIN Photodiode Current

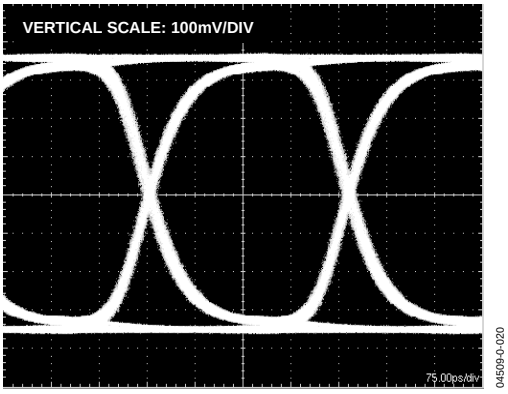

Figure 6. Eye Diagram at 3.2 Gb/s

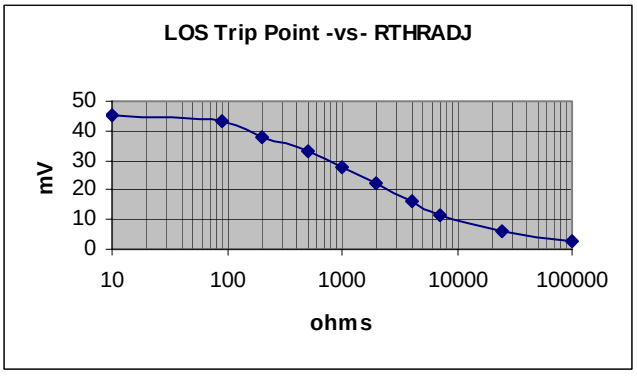

Figure 4. LOS Trip Point vs. Threshold Adjust Resistor

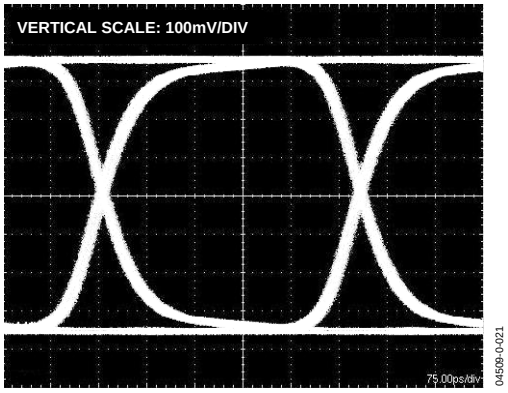

Figure 7. Eye Diagram at 2.488 Gb/s

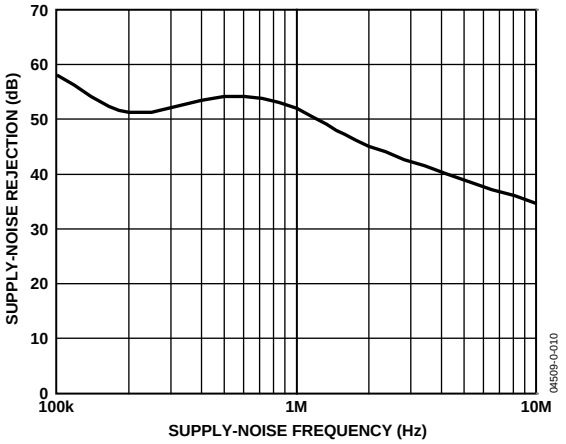

Figure 5. Typical PSRR vs. Supply-Noise Frequency

THEORY OF OPERATION

LIMAMP

Input Buffer

The ADN2891 limiting amplifier has differential inputs (PIN/NIN), with an internal 50 Ω termination. The amplifier input supports DC- or AC-coupled to TIAs. In real applications, the ROSA (receive optical sub-assembly) is typically AC-coupled to the amplifier inputs because if DC-coupled, TIA output offset degrades receiver performance.

The ADN2891 limiting amplifier is a high gain device. It is susceptible to DC offsets in the signal path. The pulse-width distortion present in a 50% duty cycle NRZ data or distortion generated from TIA appears as a DC offset to the inputs. An internal offset correction loop requires that a capacitor be connected between the CAZ1 and CAZ2 pins. For GbE and FC applications, no external capacitor is necessary, but for SONET applications, a 0.01 µF capacitor provides the data path a lower 3dB frequency cutoff of 1 kHz.

CML Output Buffer

The ADN2891 provides CML outputs, OUTP/OUTN. The outputs are internally terminated with 50 Ω to VCC.

The outputs can be kept at a static voltage by driving the SQUELCH pin to a logic high. The SQUELCH pin can be driven directly by the LOS pin, which automatically disables the amplifer outputs in situations when the input signal level drops below the programmed LOS threshold.

LOSS OF SIGNAL (LOS) DETECTOR

The receiver front-end LOS detector circuit indicates when the input signal level has fallen below the user-adjustable threshold. The threshold level can be set to anywhere from 2mVpp to 40mVpp, typically, and is set by a resistor connected between the THRADJ pin and V_{EE}. See Figure 4 for a plot of LOS Threshold -vs- THRADJ. The ADN2891 LOS circuit has a trip point down to <3.0 mV with >3 dB electrical hysteresis to prevent chatter at the LOS output. The LOS output is an open-collector output that must be pulled up externally with a 4.7 kΩ to 10 kΩ resistor.

RECEIVED SIGNAL STRENGTH INDICATOR (RSSI)

The ADN2891 has an on-chip RSSI circuit. With a photodiode biased directly by the ADN2891, a very accurate, on-chip, average power measurement is available via the RSSI circuit by monitoring the current supplied to the photodiode. The output of the RSSI is a current that is directly proportional to the average amount of PIN photodiode current. Placing a resistor between the RSSI_OUT pin and GND converts the current to a GND referenced voltage. This function eliminates the need for external RSSI circuitry in SFF-8472 compliant optical receivers.

SQUELCH MODE

Driving the SQUELCH input to a logic high disables the limiting amplifier outputs. The SQUELCH input can be connected to the LOS output to keep the limiting amplifier outputs at a static voltage level anytime the input level to the limiting amplifier drops below the programmed LOS threshold.

APPLICATIONS INFORMATION

PCB DESIGN GUIDELINES

Generic RF PCB design technique applies with special consideration implemented for the optimal performance.

Output Buffer Power Supply and Ground Planes

Pin 9 and 12 are the power supply and ground pins to provide current to differential OUTP and OUTN pins. To reduce any possible serial inductance, pin 9, which is the ground return of the output buffer, should connect to ground directly. If the ground plane is an internal plane and connections to the ground plane are vias, multiple vias in parallel to the ground can reduce the series inductance..

Similarly, to reduce the possible series inductance, pin 12, which supplies power to the high-speed differential OUTP/OUTN output buffer, should connect to power plane directly. If the power plane is an internal plane and connections to the power plane are vias, multiple vias in parallel can reduce the series inductance, especially on Pin 12. Please refer to the schematic in Figure 8 for the connection recommendation.

The exposed pad should be connected to the GND plane using filled vias so that solder does not leak through the vias during reflow. Using filled vias in parallel under the package greatly reduce the thermal resistance and enhances the reliability of the connectivity of the exposed pad to the GND plane during reflow.

To reduce power noise, a 10 µF electrolytic decoupling capacitor between VCC and VEE is at the location where the 3.3 V supply enters the PCB. The other 0.1 µF and 1 nF ceramic chip decoupling capacitors should be as close as possible to the ADN2891 VCC and VEE pins to reduce any possible current return loop.

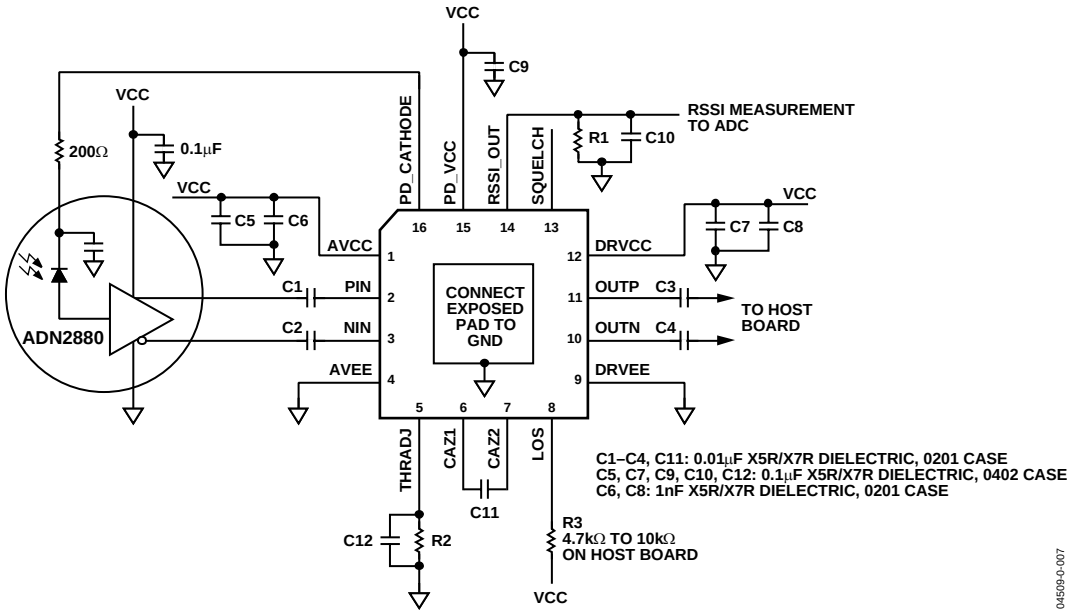

Figure 8. Typical ADN2891 Applications Circuit

PCB Layout

Figure 9 shows a recommended PC board layout. The 50 Ω transmission lines are the traces to bring the high frequency input and output signals: PIN, NIN, OUTP and OUTN to the SMA connectors with minimum reflections. To avoid a signal skew between the differential traces, each differential PIN/NIN pair and the differential OUTP/OUTN pair should have their matched trace length to the SMA connectors. C1, C2, C3, and C4 are ac-coupling capacitors in series with the high speed I/O. To minimize the possible mismatch , the AC coupling capacitor pad should be the same width as that of the 50Ω transmission line. The transmission lines should be in same width, on same signal plate, no layer changes, run from the high speed pads directly to SMA connectors. For supply decoupling, the 1 nF decoupling capacitor should be placed on the same layer as the ADN2891 as close as possible to the VCC pin. The 0.1 µF capacitor can be placed on the bottom of the PCB directly underneath the 1 nF decoupling capacitor. All high speed CML outputs have on chip, 50Ω resistors terminated between the output pin and VCC. The high speed inputs, PIN and NIN, also have the internally 50Ω terminated to an internal reference voltage.

As with any high speed mixed-signal design, make sure to keep all high speed digital traces away from sensitive analog nodes.

Soldering Guidelines for Chip Scale Package

The lands on the 16 LFCSP are rectangular. The printed circuit board pad for these should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. The land should be centered on the pad. This ensures that the solder joint size is maximized. The bottom of the chip scale package has a central exposed pad. The pad on the printed circuit board should be at least as large as this exposed pad. The user must connect the exposed pad to VEE using filled vias so that solder does not leak through the vias during reflow. This ensures a solid connection from the exposed pad to VEE.

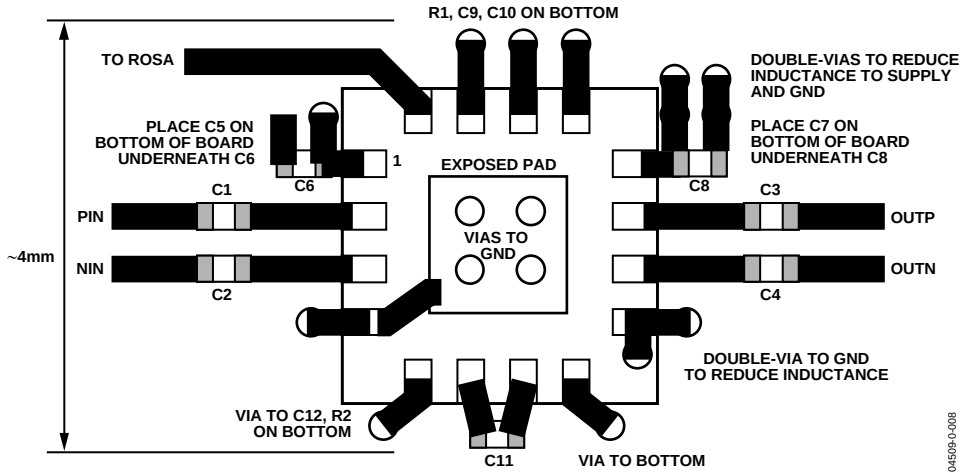

Figure 9. Recommended ADN2891 PCB Layout (TOP VIEW)

OUTLINE DIMENSIONS

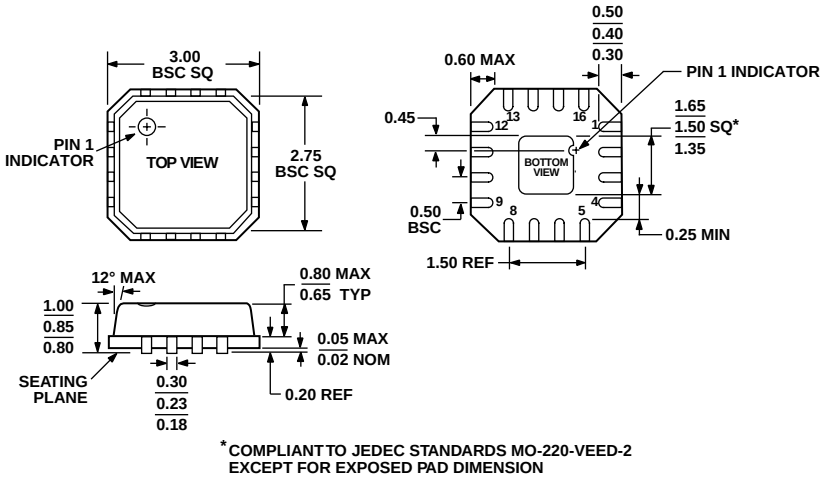

Figure 10. 16-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body
(CP-16-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
ADN2891ACP	–40°C to +95°C	16-LFCSP	CP-16-3	F02
ADN2891ACP-RL	–40°C to +95°C	16-LFCSP	CP-16-3	F02
ADN2891ACP-RL7	–40°C to +95°C	16-LFCSP	CP-16-3	F02

NOTES