Quad Low Noise, Low Cost Variable Gain Amplifier

AD8335

FEATURES

- **Low noise preamplifier (PrA)**
  - **Voltage noise = 1.3 nV/√Hz typical**
  - **Current noise = 2.4 pA/√Hz typical**
  - **NF = 7 dB ($R_S = R_{IN} = 50\ \Omega$)**
  - **Single-ended input; V_{IN} max = 625 mV p-p**
  - **Active input match**
  - **Input SNR (noise bandwidth = 20 MHz) = 92 dB**
- **VGA**
  - **Differential output**
  - **V_{OUT} max = 5 V p-p, $R_L = 500\ \Omega$ differential**
  - **Gain range (8 dB output gain step)**
  - **−10 dB to +38 dB—LO gain mode**
  - **−2 dB to +46 dB—HI gain mode**
  - **Accurate linear-in-dB gain control**
- **PrA + VGA performance**
  - **−3 dB bandwidth of 70 MHz**
  - **Excellent overload performance**
- **Supply: 5 V**
- **Power consumption**
  - **95 mW/channel (380 mW total)**
  - **65 mW/channel (PrA off; 260 mW total)**
- **Power-down**

APPLICATIONS

Medical imaging (ultrasound, gamma cameras)
Sonar
Test and measurement
Precise, stable wideband gain control

FUNCTIONAL BLOCK DIAGRAM

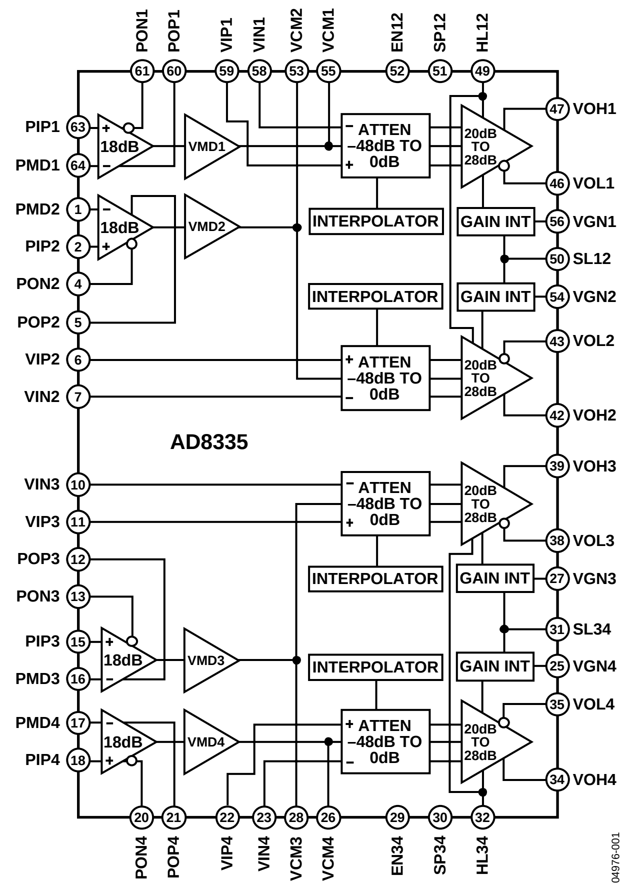

Figure 1.

GENERAL DESCRIPTION

The AD8335 is a quad variable gain amplifier (VGA) with low noise preamplifier intended for cost and power sensitive applications. Each channel features a gain range 48 dB, fully differential signal paths, active input preamplifier matching, and user-selectable maximum gains of 46 dB and 38 dB. Individual gain controls are provided for each channel.

The preamplifier (PrA) has a single-ended to differential gain of ×8 (18.06 dB) and accepts input signals ≤ 625 mV p-p. PrA noise is 1.2 nV/√Hz and the combined input referred voltage noise of the PrA and VGA is 1.3 nV/√Hz at maximum gain.

Assuming a 20 MHz noise bandwidth (NBW), the Nyquist frequency for a 40 MHz ADC, the input SNR is 92 dB. The HILO pin optimizes the output SNR for 10-bit and 12-bit ADCs with 1 V p-p or 2 V p-p full-scale (FS) inputs.

Channels 1 and 2 are enabled through the EN12 pin while Channels 3 and 4 are enabled through the EN34 pin. For VGA only applications, the PrAs can be powered down, significantly reducing power consumption.

The AD8335 is available in a 64-lead lead frame chip scale (9 mm × 9 mm) package for the industrial temperature range of −40°C to +85°C.

Rev. 0

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REVISION HISTORY

9/04—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V, T_A = 25°C, R_L = 500 Ω, f = 5 MHz, C_L = 10 pF, LO gain range (−10 dB to +38 dB), R_{FB} = 249 Ω (PrA R_{IN} = 50 Ω) and signal voltage specified differential, per channel performance, dBm (50 Ω), unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
PrA CHARACTERISTICS					
Gain	Single-ended input to differential output		18		dB
	Single-ended input to single-ended output		12		dB
Input Voltage Range	PrA output limited to 5 V p-p differential		625		mV p-p
Input Resistance	R_{FB} = 249 Ω		50		Ω
	R_{FB} = 374 Ω		75		Ω
	R_{FB} = 499 Ω		100		Ω
	R_{FB} = ∞, low frequency value into PIPx		14.7		kΩ
Input Capacitance	PIPx (Pins 2, 15, 18, 63)		1.5		pF
−3 dB Small Signal Bandwidth	With R_{FB} = 249 Ω		110		MHz
Input Voltage Noise	R_S = 0 Ω, R_{FB} = ∞		1.15		nV/√Hz
Input Current Noise			2.4		pA/√Hz
Noise Figure					
Active Termination Match	R_S = R_{IN} = 50 Ω, R_{FB} = 249 Ω		7		dB
Unterminated	R_S = 50 Ω, R_{FB} = ∞		4.4		dB
PrA + VGA CHARACTERISTICS					
−3 dB Small Signal Bandwidth	Unterminated: R_S = 50 Ω, R_{FB} = ∞		70		MHz
	Matched: R_S = R_{IN} = 50 Ω		85		MHz
Slew Rate	LO gain, VGN = 3 V, V_{OUT} = 2 V p-p		250		V/µs
	HI gain, VGN = 3 V, V_{OUT} = 2 V p-p		350		V/µs
Input Voltage Noise	Pins VGNx = 3 V, R_S = 0 Ω, R_{FB} = ∞		1.3		nV/√Hz
Noise Figure	Pins VGNx = 3 V, f = 1 MHz to 10 MHz				
Active Termination Match	R_S = R_{IN} = 50 Ω		7		dB
	R_S = R_{IN} = 100 Ω		4.5		dB
Unterminated	R_S = 50 Ω, R_{FB} = ∞		5.0		dB
	R_S = 500 Ω, R_{FB} = ∞		1.3		dB
Output Referred Noise	LO gain; VGN < 2 V		33		nV/√Hz
	HI gain; VGN < 2 V		80		nV/√Hz
Peak Output Voltage	Differential, R_L ≥ 500 Ω		5		V p-p
Output Resistance	f < 1 MHz, Pins VOHx, VOLx		1.2		Ω
Common-Mode Level	Set to midsupply for PrA and VGA		V_S/2		V
Output Offset Voltage	Differential (VOHx−VOLx) full gain range	−25	5	35	mV
	Common-mode (VOHx−VCMx, VOLx−VCMx)	−20	0	20	mV
Harmonic Distortion	V_{OUT} = 1 V p-p, LO gain, VGN = 2 V				
HD2	f = 1 MHz		−69		dBc
HD3	f = 1 MHz		−57		dBc
HD2	f = 10 MHz		−57		dBc
HD3	f = 10 MHz		−55		dBc
Harmonic Distortion	V_{OUT} = 1 V p-p, HI gain, VGN = 2 V				
HD2	f = 1 MHz		−58		dBc
HD3	f = 1 MHz		−70		dBc
HD2	f = 10 MHz		−55		dBc
HD3	f = 10 MHz		−55		dBc
Output 1 dB Compression (OP1dB)	VGN = 3 V		18		dBm
	VGN = 3 V		8		dBVpk

Parameter	Conditions	Min	Typ	Max	Unit
Two-Tone IMD3 Distortion	V_{OUT} = 1 V p-p, VGN = 3 V				
	f_1 = 1 MHz, f_2 = 1.05 MHz		−69		dBc
	f_1 = 10 MHz, f_2 = 10.05 MHz		−65		dBc
Output IP3 (OIP3)	V_{OUT} = 1 V p-p, VGN = 3 V				
	f = 1 MHz		33		dBm
	f = 10 MHz		31		dBm
Channel-to-Channel Crosstalk	V_{OUT} = 1 V p-p, f = 1 to 10 MHz		−80		dBc
Overload Recovery	Pra or VGA		10		ns
Group Delay Variation	Full gain range, f = 1 MHz to 10 MHz		3.0		ns
GAIN CONTROL INTERFACE	Pins VGNx				
Normal Operating Range		0		3	V
Maximum Range	No gain foldover	0		V_S	V
Gain Range	LO gain mode; (Pins HLxx = 0 V)		−10 to +38		dB
	HI gain mode; (Pins HLxx = V_S)		−2 to +46		dB
Scale Factor	Nominal (Pins SL12 and SL34 = 2.5 V)	19.0	20.0	21.0	dB/V
Bias Current			−0.3		µA
Response Bandwidth			5		MHz
Response Time	48 dB gain change		350		ns
GAIN ACCURACY	Pins VGNx				
Absolute Gain Error	0 ≤ VGN ≤ 0.4 V	1.25		7.5	dB
	0.4 ≤ VGN ≤ 2.6 V, 1σ	−1.25	±0.2	+1.25	dB
	2.6 ≤ VGN ≤ 3 V	−7.5		−1.25	dB
Gain Law Conformance Over Temperature	0.4 ≤ VGN ≤ 2.6 V; −40°C < T_A < +85°C		±0.75		dB
Intercept	LO gain mode; PrA matched to 50 Ω		−16.1		dB
	HI gain mode; PrA matched to 50 Ω		−8.1		dB
Channel-to-Channel Matching	0.4 ≤ V_{GN} ≤ 2.6 V		0.15		dB
LOGIC LEVEL—HILO, SHUTDOWN PREAMP, and ENABLE INTERFACES	Pins HLxx, SPxx, and ENxx				
Logic Level High		2.75		5	V
Logic Level Low		0		1	V
BIAS CURRENT—HILO, ENABLE					
Logic high			80		µA
Logic low			−12		µA
INPUT RESISTANCE—HILO, ENABLE			50		kΩ
BIAS CURRENT – SHUTDOWN PREAMP					
Logic high			20		µA
Logic low			0		µA
INPUT RESISTANCE—SHUTDOWN PREAMP			500		kΩ
HILO Response Time			0.6		µs
Enable Response Time			100		µs
POWER SUPPLY	Pins VPPx and VPVx				
Supply Voltage		4.5	5	5.5	V
Quiescent Current	Per channel—PrA and VGA enabled		19		mA
Over Temperature	−40°C < T_A < +85°C	16		22.8	mA
Quiescent Power	Per channel—PrA and VGA enabled		95		mW
Quiescent Current	Per channel—PrA disabled, VGA enabled		13		mA
Quiescent Power	Per channel—PrA disabled, VGA enabled		65		mW
Quiescent Current	All channels enabled		76		mA
Disable Current	All channels disabled		0.8		mA
PSRR	V_{GN} = 0 V, all bypass capacitors removed, 1 MHz		−60		dB

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Voltage	
Supply V_S	6 V
Preamp Input	V_S
VGA Inputs	V_S
Enable, Shutdown Preamp, and HILO Interfaces	V_S
Gain	V_S
Power Dissipation (4-layer JEDEC Board (2S2P))	2.46 W
θ_{JA}	26.4°C/W
θ_{JC}	6.8°C/W
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering 60 s)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

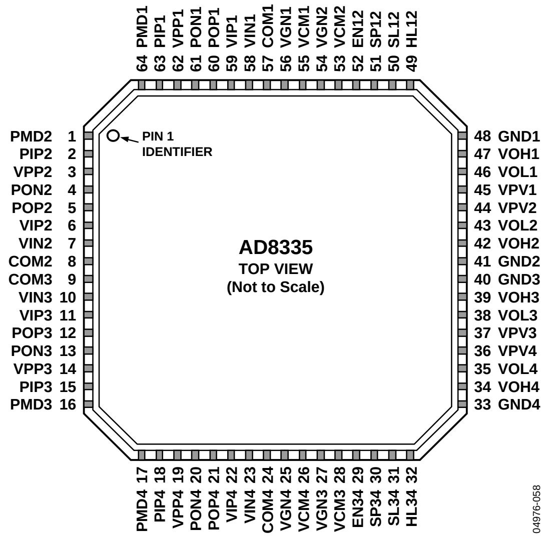


Figure 2. LFCSP Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Function
1	PMD2	Preamp input common—Ch2
2	PIP2	Preamp input—Ch2
3	VPP2	Positive supply preamp—Ch2
4	PON2	Preamp output negative—Ch2
5	POP2	Preamp output positive—Ch2
6	VIP2	VGA input positive—Ch2
7	VIN2	VGA input negative—Ch2
8	COM2	Ground preamp—Ch2
9	COM3	Ground preamp—Ch3
10	VIN3	VGA input negative—Ch3
11	VIP3	VGA input positive—Ch3
12	POP3	Preamp output positive—Ch3
13	PON3	Preamp output negative—Ch3
14	VPP3	Positive supply preamp—Ch3
15	PIP3	Preamp input—Ch3
16	PMD3	Preamp input common—Ch3
17	PMD4	Preamp input common—Ch4
18	PIP4	Preamp input—Ch4
19	VPP4	Positive supply preamp—Ch4
20	PON4	Preamp output negative—Ch4
21	POP4	Preamp output positive—Ch4
22	VIP4	VGA input positive—Ch4
23	VIN4	VGA input negative—Ch4
24	COM4	Ground preamp—Ch4
25	VGN4	Gain control—Ch4
26	VCM4	Common-mode decoupling pin—Ch4
27	VGN3	Gain control—Ch3
28	VCM3	Common-mode decoupling pin—Ch3
29	EN34	Enable—Ch3 and Ch4
30	SP34	Shutdown—preamp3 and preamp4
31	SL34	Slope decoupling pin—Ch3 and Ch4
32	HL34	HILO pin—Ch3 and Ch4
33	GND4	Ground VGA—Ch4
34	VOH4	VGA output positive—Ch4
35	VOL4	VGA output negative—Ch4
36	VPV4	Positive supply VGA—Ch4
37	VPV3	Positive supply VGA—Ch3
38	VOL3	VGA output negative—Ch3
39	VOH3	VGA output positive—Ch3
40	GND3	Ground VGA —Ch3
41	GND2	Ground VGA — Ch2
42	VOH2	VGA output positive—Ch2
43	VOL2	VGA output negative—Ch2
44	VPV2	Positive supply VGA—Ch2
45	VPV1	Positive supply VGA—Ch1
46	VOL1	VGA output negative—Ch1
47	VOH1	VGA output positive—Ch1
48	GND1	Ground VGA — Ch1
49	HL12	HILO pin—Ch1 and Ch2
50	SL12	Slope decoupling pin—Ch1 and Ch2
51	SP12	Shutdown—preamp1 and preamp2
52	EN12	Enable—Ch1 and Ch2
53	VCM2	Common-mode decoupling pin—Ch2
54	VGN2	Gain control—Ch2
55	VCM1	Common-mode decoupling pin—Ch1
56	VGN1	Gain control—Ch1
57	COM1	Ground preamp—Ch1
58	VIN1	VGA input negative—Ch1
59	VIP1	VGA input positive—Ch1
60	POP1	Preamp output positive—Ch1
61	PON1	Preamp output negative—Ch1
62	VPP1	Positive supply preamp—Ch1
63	PIP1	Preamp input—Ch1
64	PMD1	Preamp input common—Ch1

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 5 V, T_A = 25°C, R_L = 500 Ω, f = 5 MHz, C_L = 10 pF, LO gain range (−10 dB to +38 dB), R_{FB} = 249 Ω (PrA R_{IN} = 50 Ω) and signal voltage specified differential, per channel performance, unless otherwise noted.

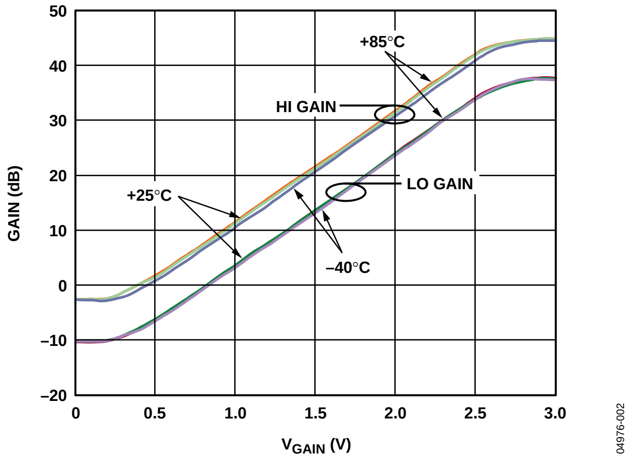


Figure 3. Gain vs. V_{GAIN} at Three Temperatures (See Figure 49)

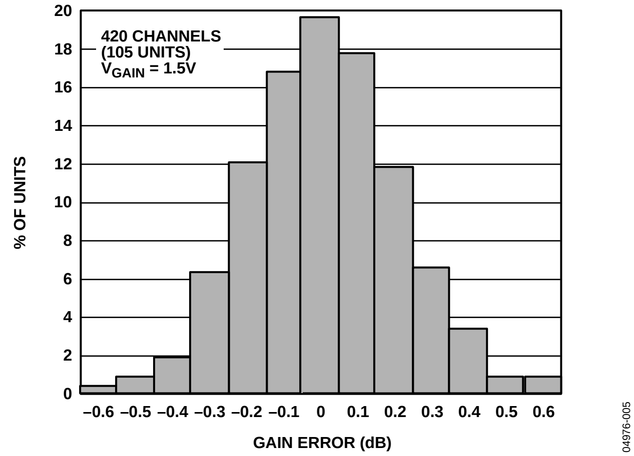


Figure 6. Gain Error Histogram

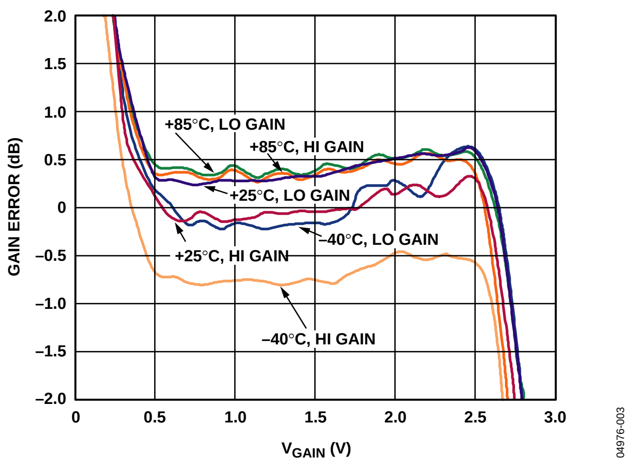


Figure 4. Gain Error vs. V_{GAIN} at Three Temperatures (See Figure 49)

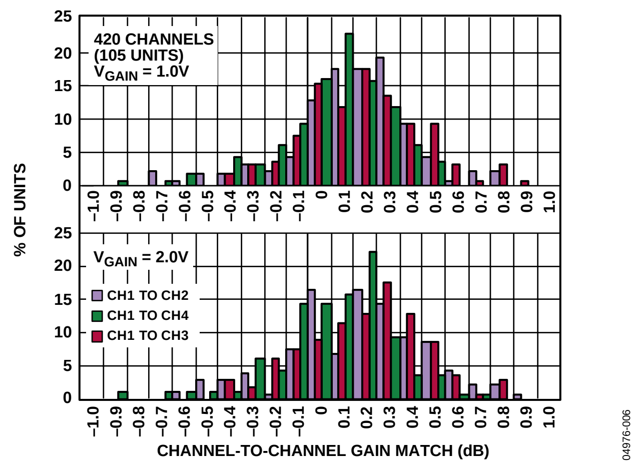


Figure 7. Gain Match Histogram for V_{GAIN} = 1 V and 2 V

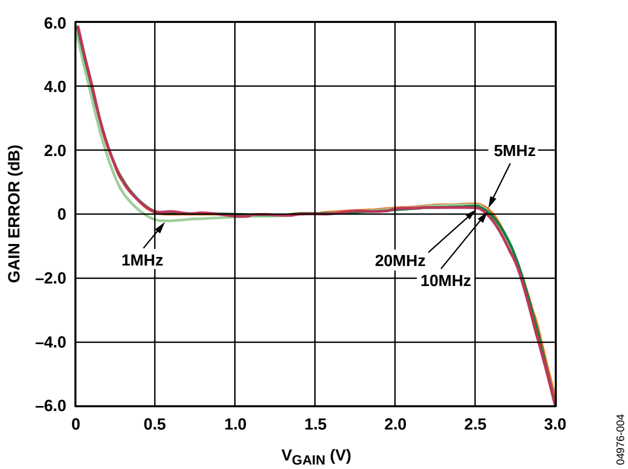


Figure 5. Gain Error vs. V_{GAIN} at Various Frequencies (See Figure 49)

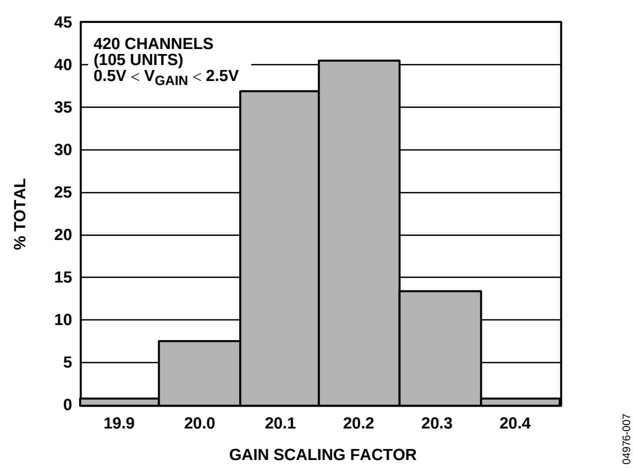


Figure 8. Gain Scaling Factor Histogram for 0.5 V < V_{GAIN} < 2.5 V

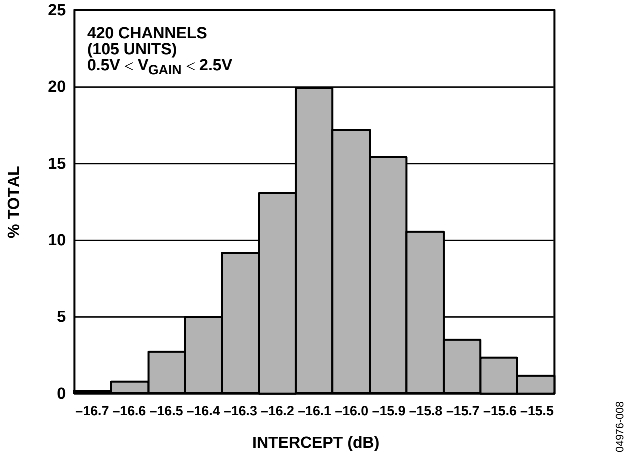


Figure 9. Intercept Histogram

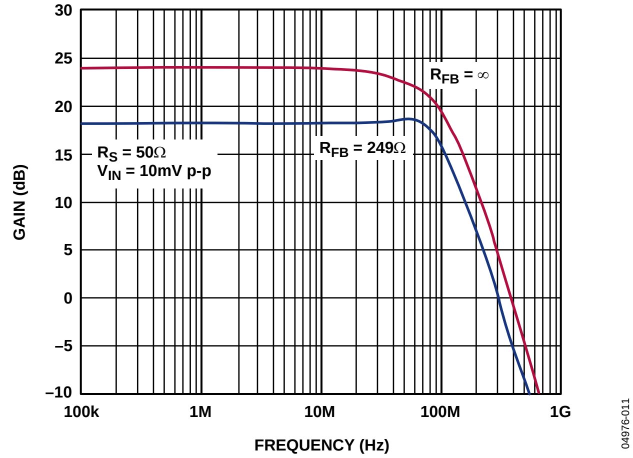


Figure 12. Frequency Response for a Terminated and Unterminated 50 Ω Source (See Figure 49)

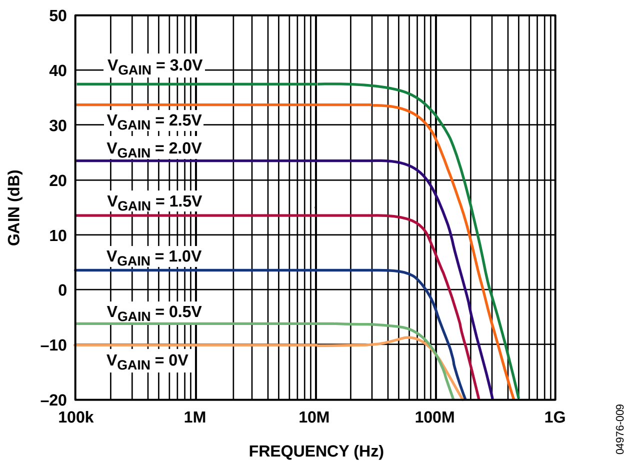


Figure 10. Frequency Response for Various Values of V_{GAIN} (See Figure 49)

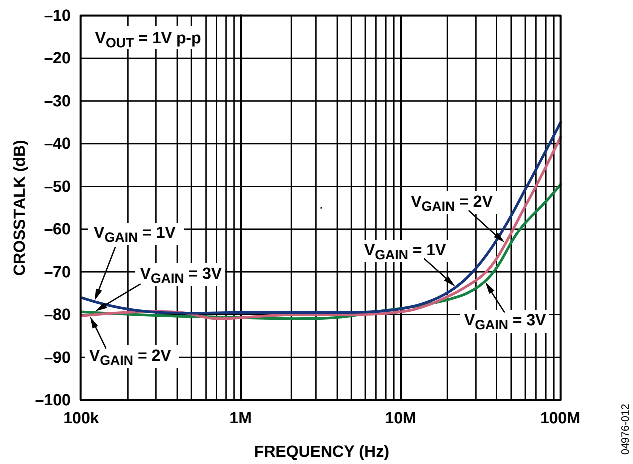


Figure 13. Channel-to-Channel Crosstalk vs. Frequency for Various Values of V_{GAIN}

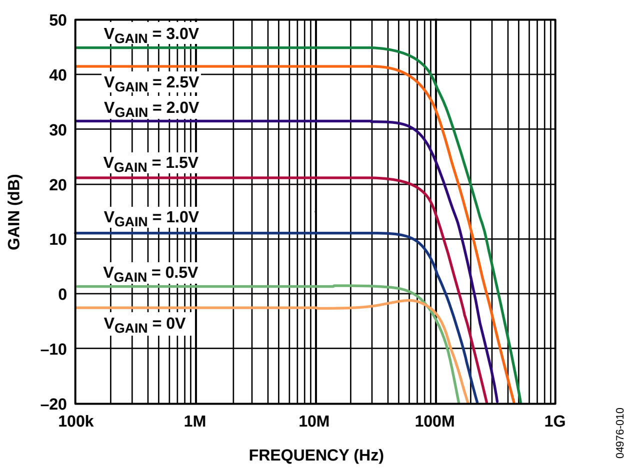


Figure 11. Frequency Response vs. Frequency for Various Values of V_{GAIN}, HILO = HI (See Figure 49)

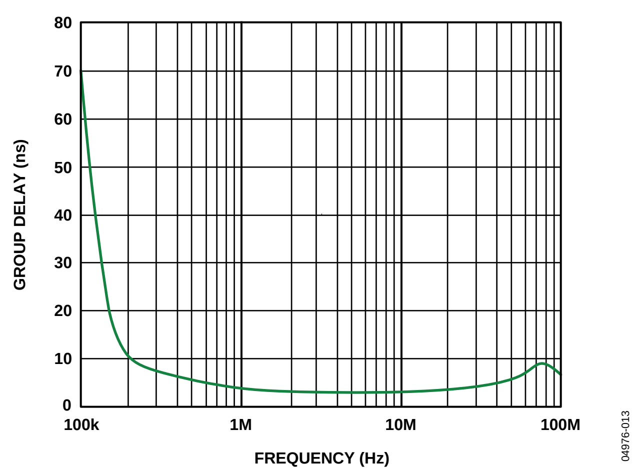


Figure 14. Group Delay vs. Frequency

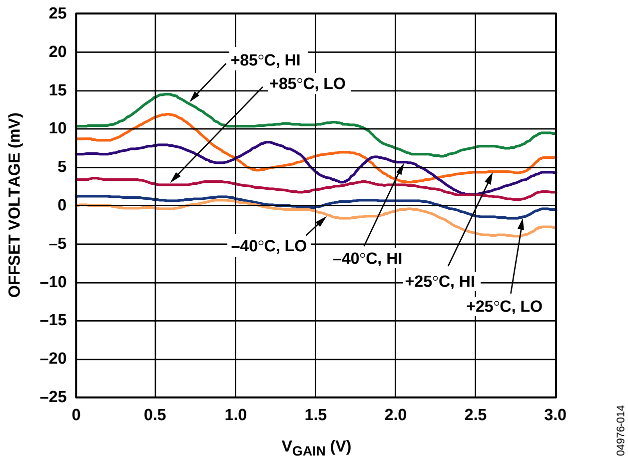


Figure 15. Differential Output Offset Voltage vs. V_{GAIN} at Three Temperatures

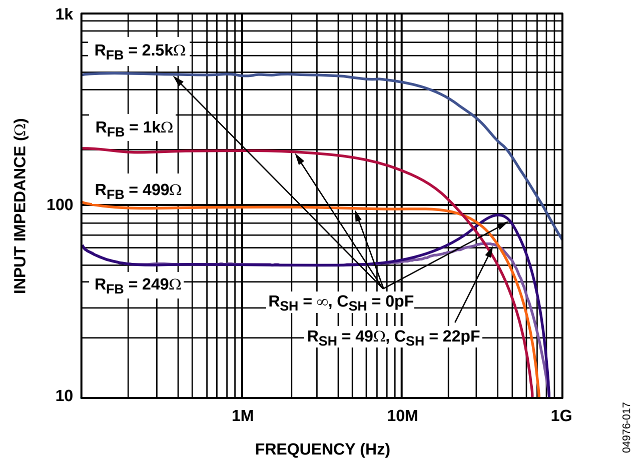


Figure 18. Preamp Input Resistance vs. Frequency for Various Values of R_{FB}

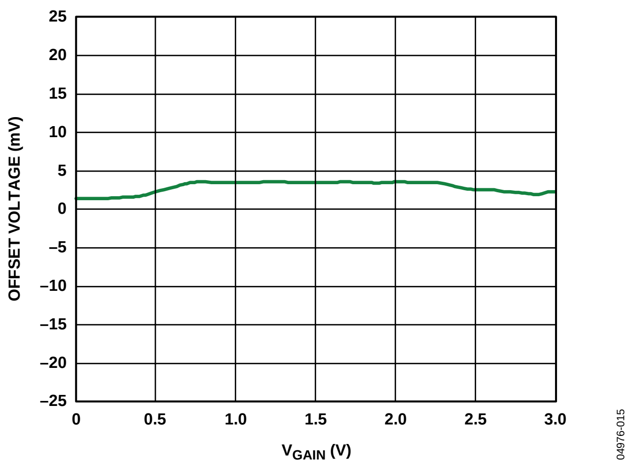


Figure 16. Absolute Offset vs. V_{GAIN} at Pins VOHx and VOLx Relative to Pins VCMx

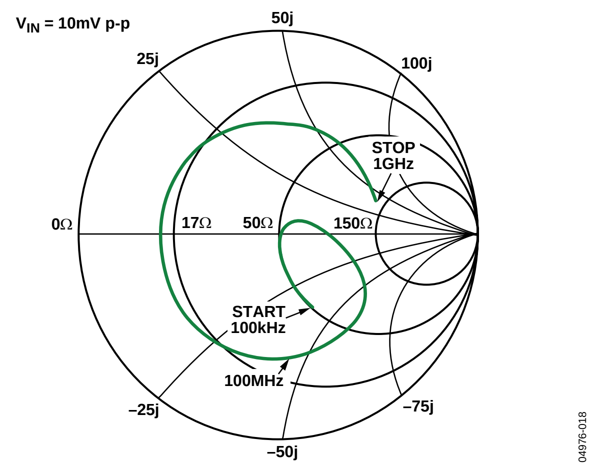


Figure 19. Smith Chart S11 vs. Frequency, 100 kHz to 1 GHz

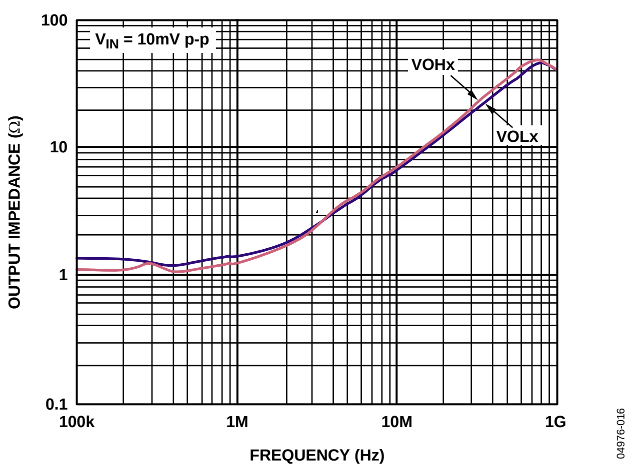


Figure 17. Output Resistance at Pins VOHx and VOLx vs. Frequency

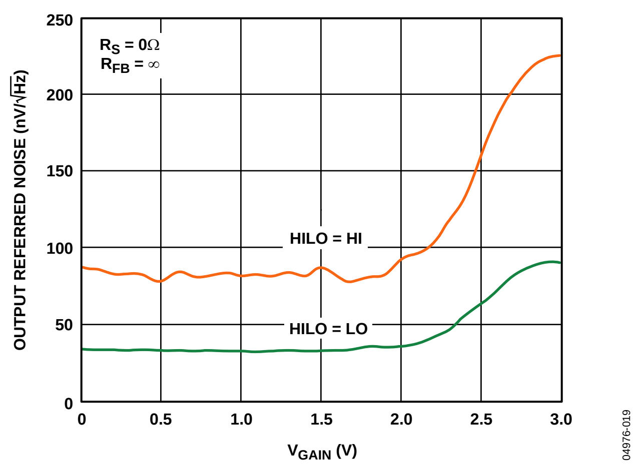


Figure 20. Output Referred Noise vs. V_{GAIN} (See Figure 50)

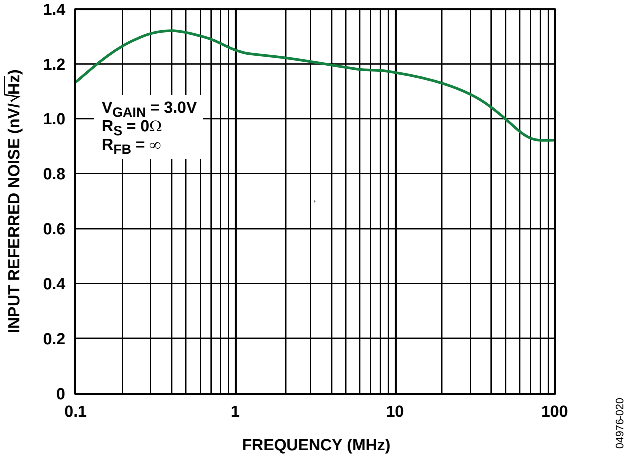


Figure 21. Short-Circuit Input Referred Noise vs. Frequency at Maximum Gain (See Figure 50)

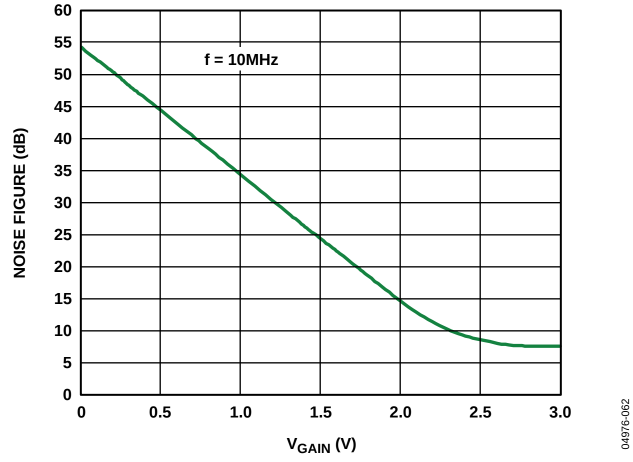


Figure 24. Noise Figure vs. V_{GAIN} for $R_S = R_{IN} = 50\ \Omega$

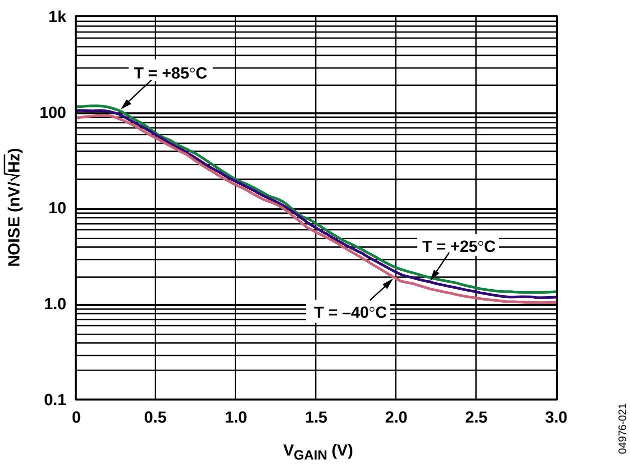


Figure 22. Input Referred Noise vs. V_{GAIN} at Three Temperatures (See Figure 50)

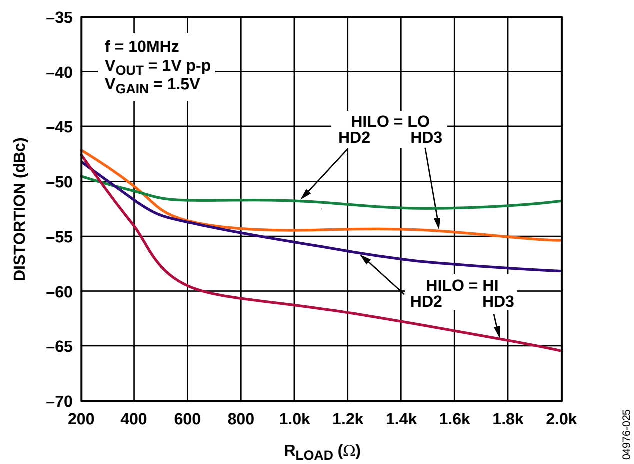


Figure 25. Harmonic Distortion vs. R_{LOAD} (See Figure 50)

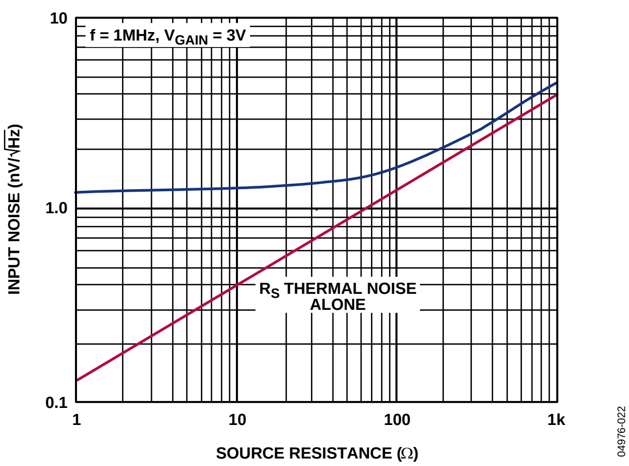


Figure 23. Input Referred Noise vs. R_S

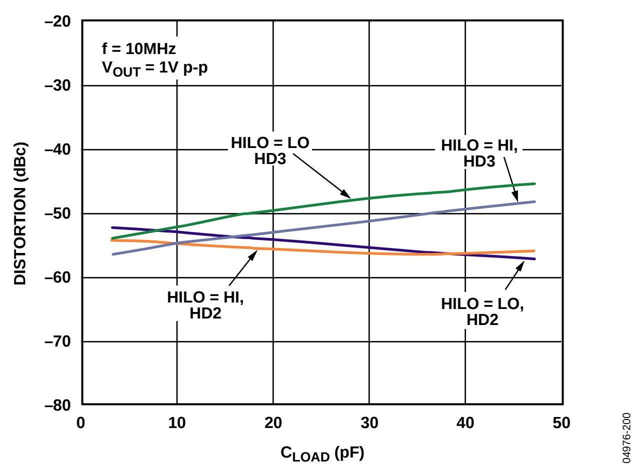


Figure 26. Harmonic Distortion vs. C_{LOAD} (See Figure 53)

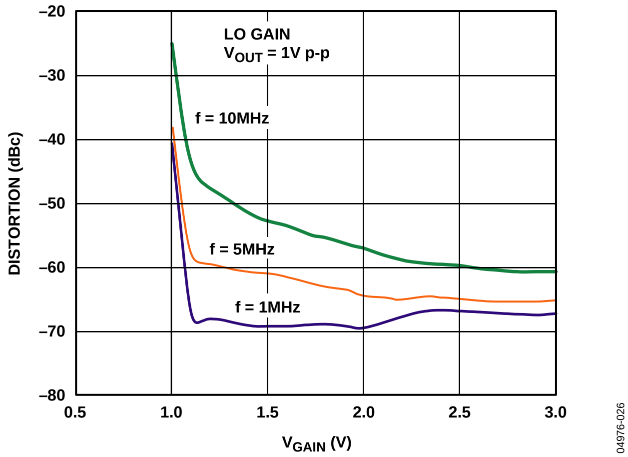


Figure 27. HD2 vs. V_{GAIN} at Three Frequencies, LO Gain (See Figure 53)

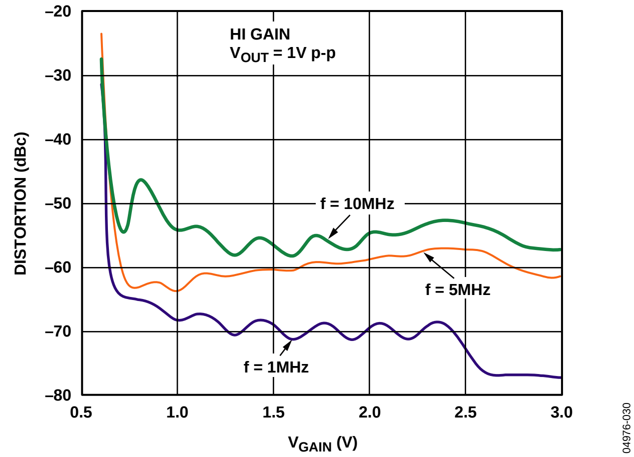


Figure 30. HD3 vs. V_{GAIN} at Three Frequencies, HI Gain (See Figure 53)

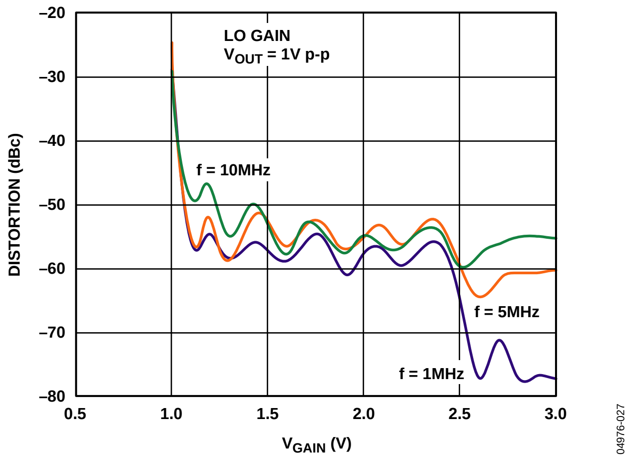


Figure 28. HD3 vs. V_{GAIN} at Three Frequencies, LO Gain (See Figure 53)

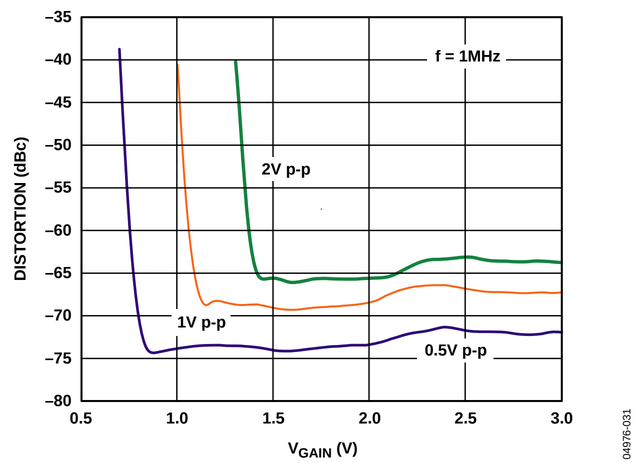


Figure 31. HD2 vs. V_{GAIN} at Three Output Voltages, LO Gain (See Figure 53)

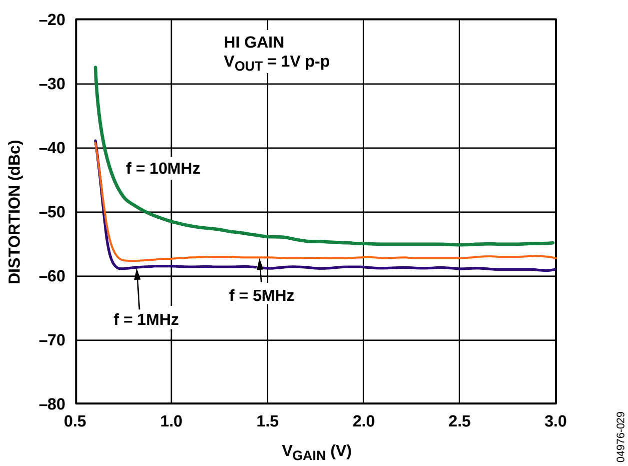


Figure 29. HD2 vs. V_{GAIN} at Three Frequencies, HI Gain (See Figure 53)

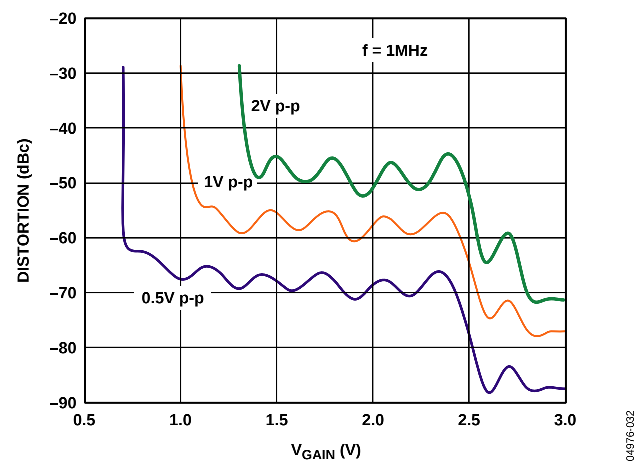


Figure 32. HD3 vs. V_{GAIN}, at Three Output Voltages, LO Gain (See Figure 53)

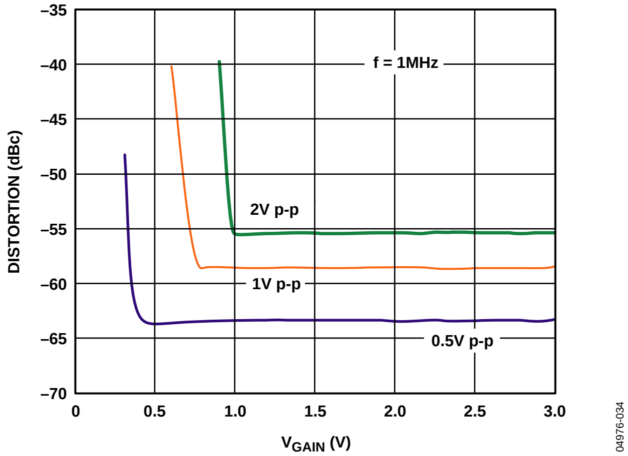


Figure 33. HD2 vs. V_{GAIN} at Three Output Voltages, HI Gain, f = 1 MHz (See Figure 53)

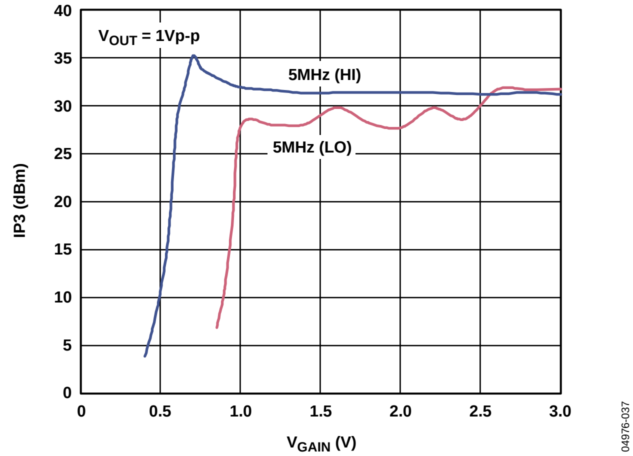


Figure 36. Output Referred IP3 (OIP3) vs. V_{GAIN}

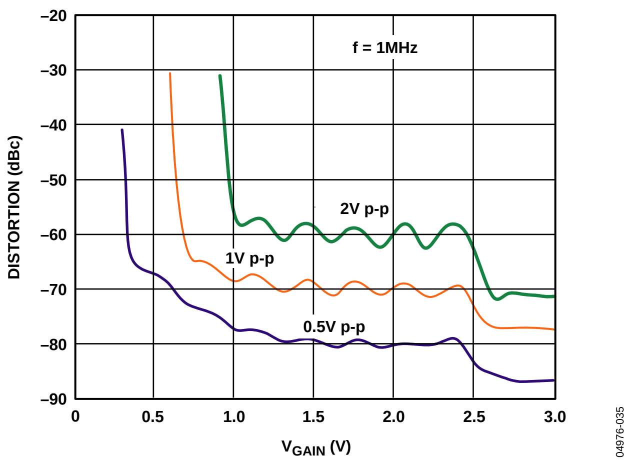


Figure 34. HD3 vs. V_{GAIN} at Three Output Voltages, HI Gain (See Figure 53)

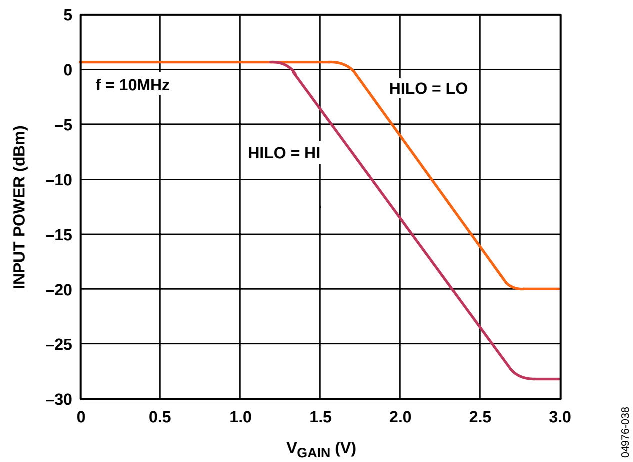


Figure 37. Input P1dB (IP1dB) vs. V_{GAIN}

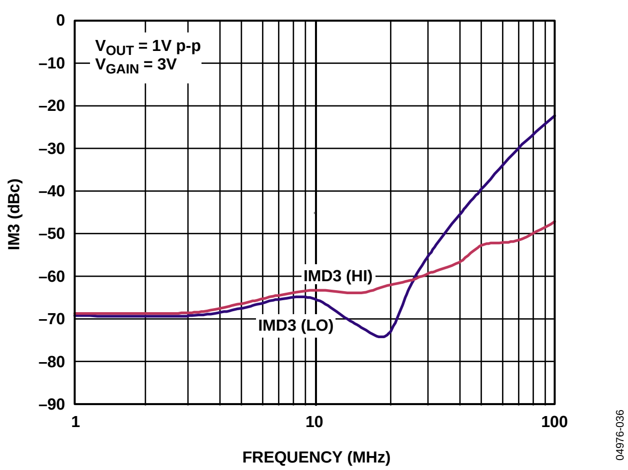


Figure 35. IMD3 vs. Frequency

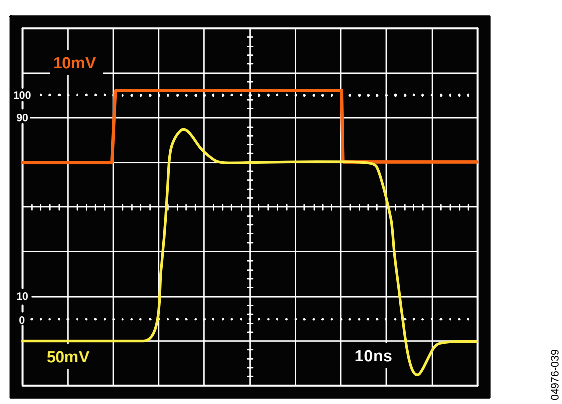


Figure 38. Small Signal Pulse Response, LO Gain (See Figure 51)

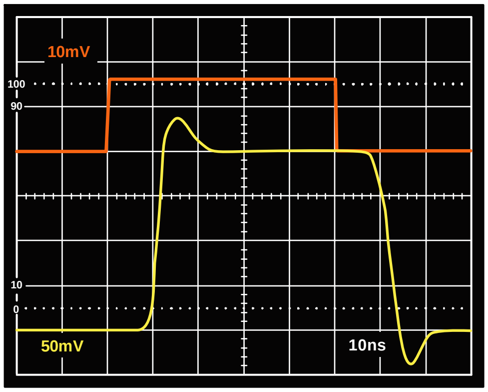


Figure 39. Large Signal Pulse Response, LO Gain (See Figure 51)

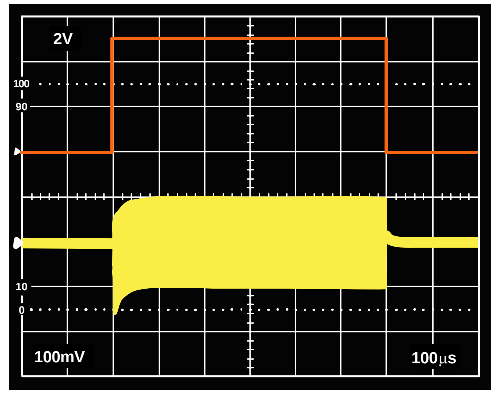


Figure 42. Small Signal Enable Response (See Figure 51)

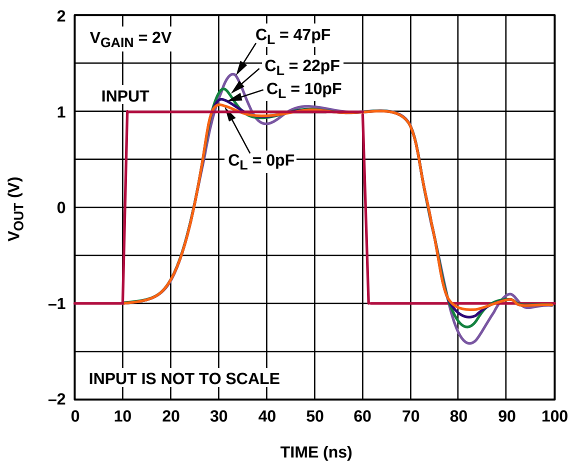


Figure 40. Large Signal Pulse Response for Various Capacitive Loads, C_L = 0 pF, 10 pF, 20 pF, 47 pF Each Output (See Figure 51)

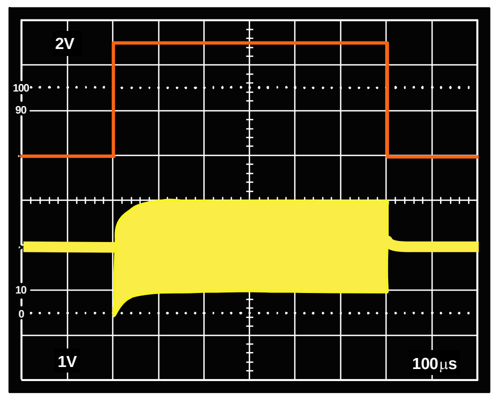


Figure 43. Large Signal Enable Response (See Figure 51)

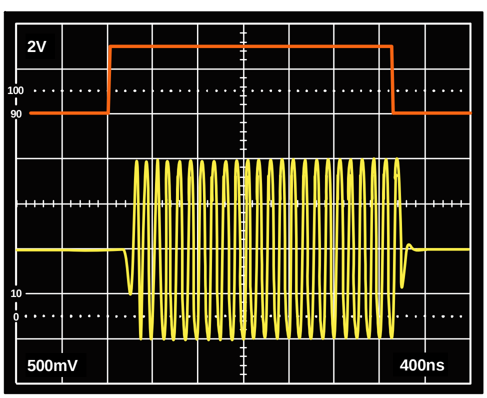


Figure 41. Gain Response, V_{GAIN} Stepped from 0 V to3 V, V_{OUT} = 2 V p-p (See Figure 51)

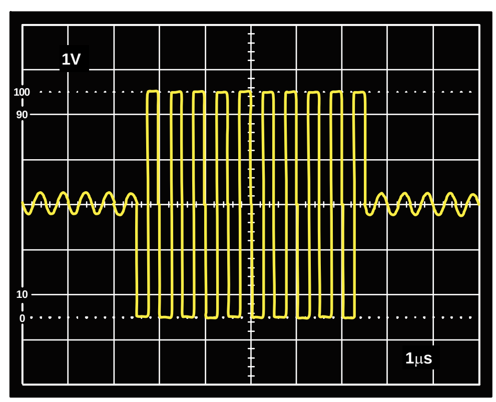


Figure 44. Preamp Overdrive Recovery, 50 mV p-p to 1.5 V p-p at Preamp Input (Measured at Preamp Output)

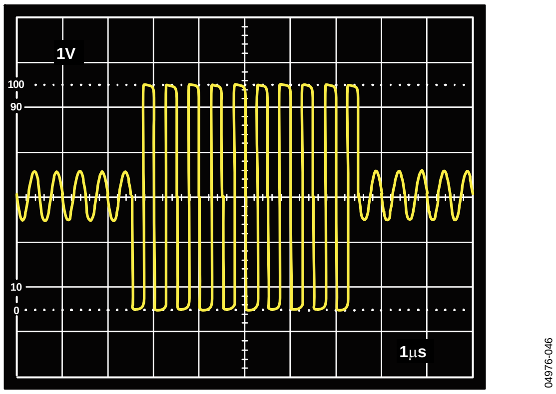


Figure 45. VGA Overdrive Recovery, 40 mV to 500 mV Input, V_{GAIN} = 2.5 V

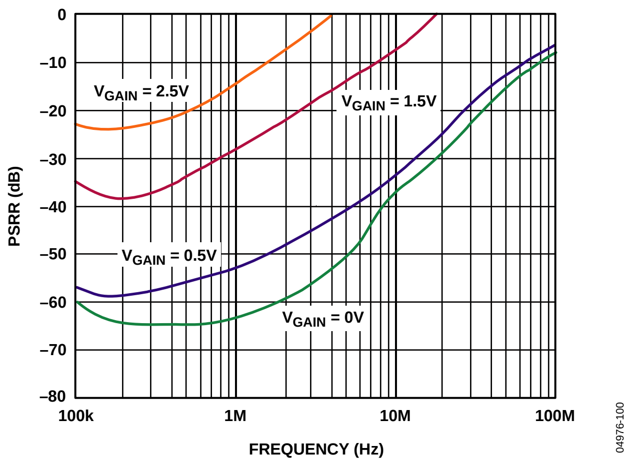


Figure 46. PSRR vs. Frequency (All Bypass Capacitors Removed)

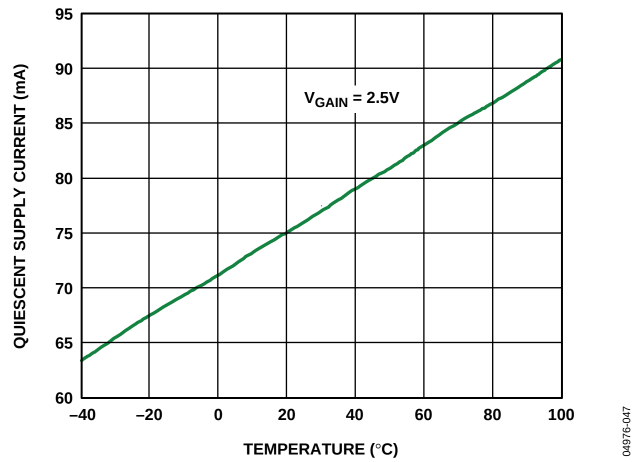


Figure 47. Quiescent Supply Current vs. Temperature

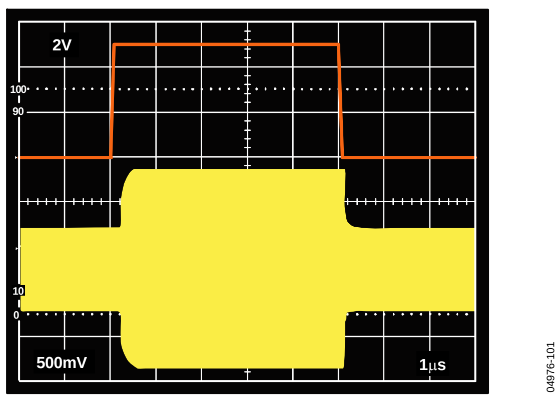


Figure 48 HILO Response Time

TEST CIRCUITS

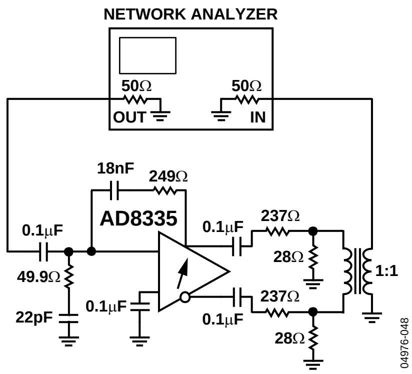


Figure 49. Test Circuit for Gain and Bandwidth Measurements

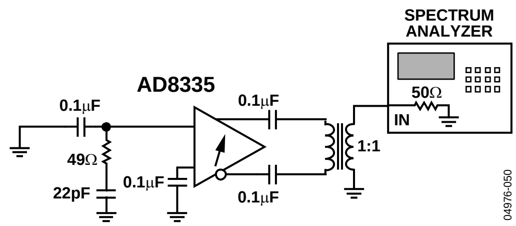


Figure 50. Test Circuit Used for Noise Measurements

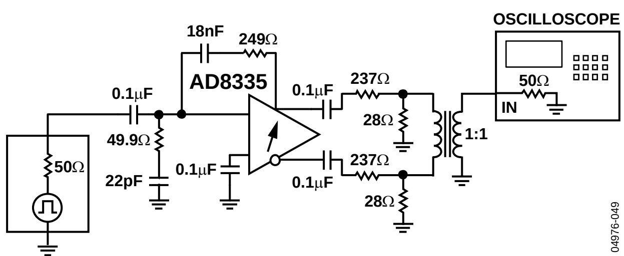


Figure 51. Test Circuit for Transient Measurements

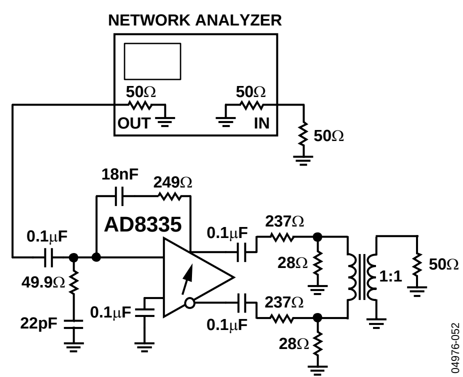


Figure 52. Test Circuit Used for S11 Measurements

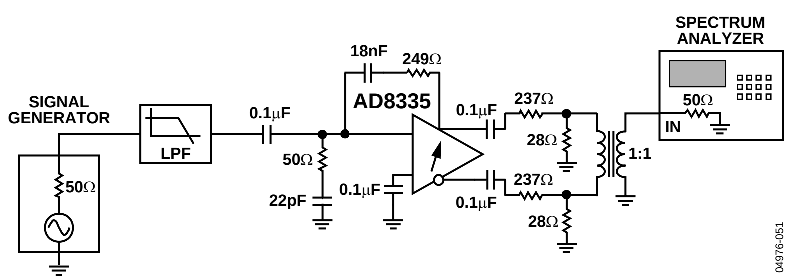


Figure 53. Test Circuit Used for Distortion Measurements

THEORY OF OPERATION

Figure 54 is a simplified block diagram of a single channel. Each channel consists of a low noise preamplifier (PrA) followed by a VGA with a user-selectable gain of 20 dB or 28 dB. Channels are enabled in pairs, Channels 1 and 2 and Channels 3 and 4. The preamps are enabled by grounding Pins SPxx and powered down by connecting them to the positive supply. The ENxx pins are connected to the positive supply to enable the VGAs and the overall channel. HILO configures VGA for a fixed gain of 20 dB or 28 dB, with 0 V or 5 V applied to the HLxx pins, respectively. Channels 1 and 2 share Pin HL12, and Channels 3 and 4 share Pin HL34. The HLxx pins are typically hardwired to adjust the VGA gain according to an ADC resolution of 12 bits for LO gain and 10 bits for HI gain.

The signal path is fully differential throughout to maximize signal swing and reduce even-order distortion; however, the preamplifiers are designed to be driven from a single-ended signal source. Gain values are referenced from the single-ended PrA input to the differential output of either the PrA or the VGA. Again referring to Figure 54, the system gain is distributed as listed in Table 4.

Table 4. Channel Gain Distribution

Section	LO Nominal Gain (dB)	HI Nominal Gain (dB)
PrA	18.06	18.06
Attenuator	0 to −48.16	0 to −48.16
Output Amp	20	27.96
Aggregate	−10.1 to +38.6	−2.14 to +46.02

In the remainder of this document, the gain values are rounded to −10 dB to +38 dB for LO gain mode and to −2 dB to +46 dB for HI gain mode. If desired, Equation 1 can be used to calculate the gain at value of V_{GAIN}:

$$Gain(dB) = 20\frac{dB}{V}V_{GN} + ICPT \qquad (1)$$

where $ICPT = -16.1$ dB for LO gain mode with the preamp input matched to 50 Ω (R_{FB} = 250 Ω) and −10.1 dB for the unmatched input case. For HI gain mode, these numbers are −8.1 dB and −2.1 dB, respectively.

Power consumption is 95 mW/channel from a 5 V supply, or 380 mW for all four channels. Power is distributed 35% for the PrA, and 65% for the remainder of the circuit. The preamps can be shut down via the SP12 and SP34 pins if a user wants to use the VGAs only. However, to avoid feedthrough around the preamp, feedback resistors should not be installed.

ENABLE SUMMARY

Table 5 summarizes the enable/shutdown logic and resulting supply current.

Table 5. Control Pin Logic and Power Consumption

EN12	SP12	EN34	SP34	PrA12	VGA12	PrA34	VGA34	IS
H	L	H	L	On	On	On	On	76 mA
H	H	H	H	Off	On	Off	On	52 mA
L	L	L	L	Off	Off	Off	Off	0.8 mA
L	H	L	H	Off	Off	Off	Off	0.8 mA

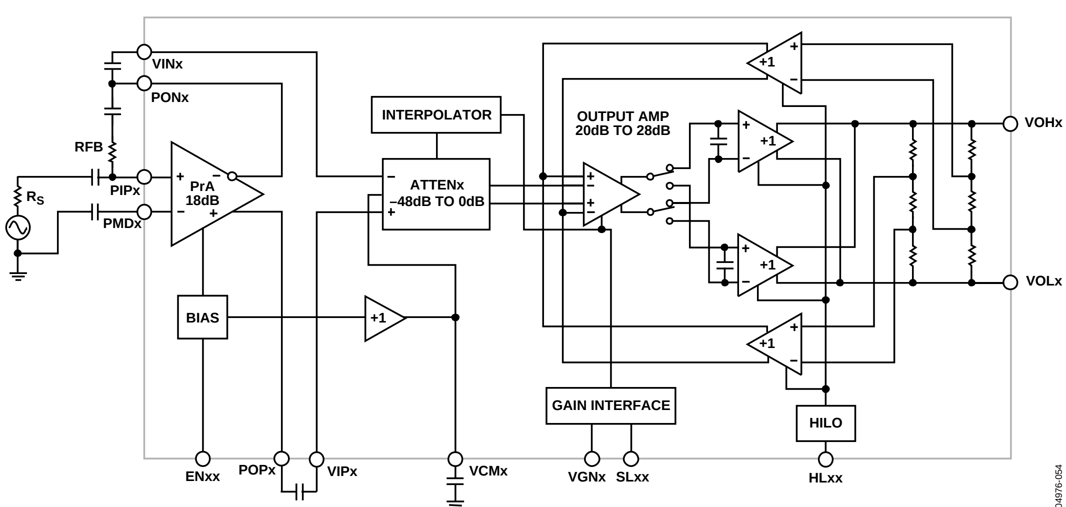


Figure 54. Simplified Block Diagram of Single Channel

PREAMP

Although the preamp signal path is fully differential, the design is optimized for single-ended input drive and signal source resistance matching. Thus, the negative input to the differential preamplifier Pins PMDx must be ac-grounded to provide a balanced differential signal at the PrA outputs. Detailed information regarding the preamplifier architecture is found in the LNA section of the AD8331/AD8332 data sheet.

The preamplifier consists of a fixed gain amplifier with differential outputs. With the negative output available and a fixed gain of 8 (18.06 dB), an active input termination is synthesized by connecting a feedback resistor between the negative output and the positive input, Pin PIPx. This technique is well known and results in the input resistance shown in Equation 2.

$$R_{IN} = \frac{R_{FB}}{(1 + A/2)} \quad (2)$$

where A/2 is the single-ended gain, or the gain from the PIPx inputs to the PONx outputs. Since the amplifier has a gain of ×8 from its input to its differential output, it is important to note that the gain A/2 is the gain from Pin PIPx to Pin PONx, which is 6 dB lower, or 12.04 dB (×4). The input resistance is reduced by an internal bias resistor of 14.7 kΩ in parallel with the source resistance connected to Pin PIPx, with Pin PMDx ac-grounded. Equation 3 can be used to calculate the needed R_{FB} for a desired R_{IN}, and is used for higher values of R_{IN}.

$$R_{IN} = \frac{R_{FB}}{(1+4)} \,||\, 14.7\,\text{k}\Omega \quad (3)$$

For example, to set R_{IN} = 200 Ω, the value of R_{FB} is 1.013 kΩ. If the simplified Equation 2 is used to calculate R_{IN}, the value is 197 Ω, resulting in a less than 0.1 dB gain error. Factors such as a widely varying source resistance might influence the absolute gain accuracy more significantly. At higher frequencies, the input capacitance of the PrA needs to be considered. The user must determine the level of matching accuracy and adjust R_{FB} accordingly.

The bandwidths (BW) of the preamplifier and VGA are approximately 110 MHz each, resulting in a cascaded BW of approximately 80 MHz. Ultimately the BW of the PrA limits the accuracy of the synthesized R_{IN}. For $R_{IN} = R_S$ up to approximately 200 Ω, the best match is between 100 kHz and 10 MHz, where the lower frequency limit is determined by the size of the ac-coupling capacitors, and the upper limit is determined by the preamplifier BW. Furthermore, the input capacitance and R_S limits the BW at higher frequencies.

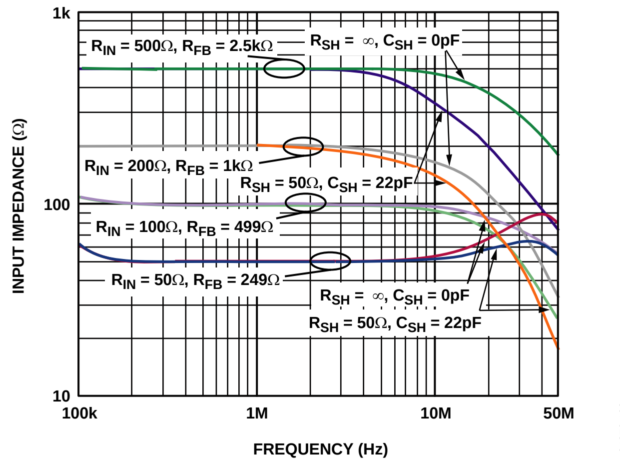


Figure 55. R_{IN} vs. Frequency for Various Values of R_{FB}. Effects of R_{SH} and C_{SH} are also shown.

Figure 55 shows R_{IN} vs. frequency for various values of R_{FB}. Note that at the lowest value, 50 Ω, R_{IN} peaks at frequencies greater than 10 MHz. This is due to the BW roll-off of the PrA as mentioned earlier. The R_{SH} and C_{SH} network shown in Figure 58 reduces this peaking.

However, as can be seen for larger R_{IN} values, parasitic capacitance starts rolling off the signal BW before the PrA can produce peaking and the R_{SH}/C_{SH} network further degrades the match. Therefore R_{SH} and C_{SH} should not be used for values of R_{IN} greater than 50 Ω.

Noise

The total input referred noise (IRN) is approximately 1.3 nV/√Hz. Allowing for a gain of ×8 in the preamp, the VGA noise is 0.46 nV/√Hz referred to the PrA input. The preamp noise is 1.2 nV/√Hz. It is important to note that these noise values include all amplifier noise sources, including the VGA and the preamplifier gain resistors. Frequently, manufacturer noise specifications exclude gain setting resistors, and the voltage noise spectral density of an op amp might be presented as 1 nV/√Hz. Including the gain resistors results in a much higher noise specification.

Figure 56 shows the simulated noise figure (NF) vs. source resistance, and various values of preamplifier R_{IN} from 50 Ω, to 14.7 kΩ, the value seen looking into Pins PIPx when $R_{FB} = \infty$. As shown in the figure, the minimum NF for R_{IN} = 50 Ω is slightly less than 7 dB. Note that, for this preamplifier, the NF is optimized for the R_{IN} from 50 Ω to 200 Ω; for $R_{FB} = \infty$, the minimum NF is at approximately 480 Ω. This optimum noise resistance can also be calculated by dividing the input referred voltage noise by the current noise.

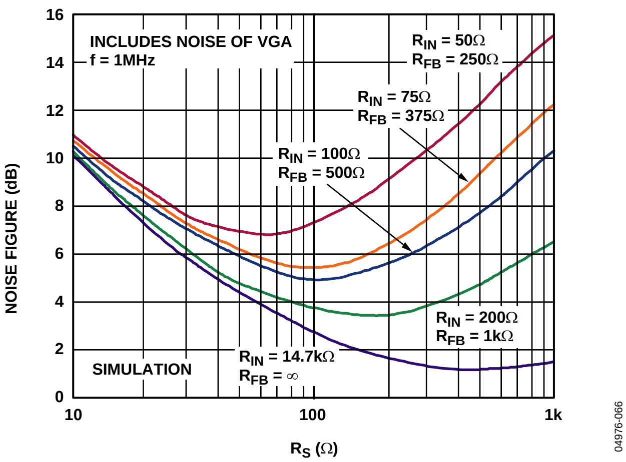


Figure 56. Simulated Noise Figure vs. R_S for Various Fixed Values of R_{IN}, Actively Matched

VGA

As seen in Figure 54, the basic architecture, an X-AMP™, consists of a ladder attenuator, followed by a fixed-gain amplifier with selectable input stages. Earlier examples of this architecture are to be found in the AD60x series, AD8331/AD8332, and AD8367 VGAs. Through a proprietary, temperature-compensated interpolator design, the bias currents to the input g_m stages are continuously steered from right to left (decreasing attenuation) resulting in increasing gain.

The HILO (HL12 and HL34) gain pins select one of two output amplifier networks consisting of the feedback resistors, amplifier stages, and buffers.

Optimizing the System Dynamic Range

The VGA output gain switch of 8 dB (×2.5) optimizes the VGA noise floor for a 10-bit or 12-bit ADC, assuming a full-scale ADC input voltage of 1 V p-p.

At low gain the ADC SNR should limit the system noise performance, while at high gains the noise is defined by the source and preamplifier. The maximum voltage swing is bounded by the full-scale peak-to-peak ADC input voltage (typically 1 V p-p to 2 V p-p). The noise performance is optimized by adjusting the noise floor of the VGA according to the ADC resolution. The SNR of a 12-bit converter is theoretically 12 dB better than a 10-bit; however, approximately 8 dB is typical in practice, accounting for the 8 dB gain option of the AD8335. The IRN and the power consumption of the VGA are unaffected by either gain setting; therefore, only the output referred noise (ORN) changes (by 8 dB) without affecting any other parameters.

Attenuator

The attenuator is an 8-stage differential R-2R ladder with a total attenuation of 48.16 dB – 6.02 dB per tap. The effective input resistance per side is 320 Ω nominally for a total differential resistance of 640 Ω. The common-mode voltage of the attenuator and the VGA is controlled by an amplifier that uses the same midsupply voltage derived in the preamplifier, permitting dc coupling of the PrA to the VGA without introducing large offsets due to common-mode differences. However, when dc coupling between the PrA and VGA, any offset from the PrA are amplified as the gain is increased, producing an exponentially increasing VGA output offset. When the PrA and the VGA are ac-coupled, the output offset is unchanged with changes in gain (see Figure 15). As a result, ac coupling is recommended for most applications. As can be seen from Figure 54, Pins VCMx connect to the respective midpoints on each channel and are used to ac decouple the common-mode node at high frequencies. It is very important that at least a 0.1 μF capacitor be used, with better decoupling at higher frequencies when another smaller capacitor (10 nF) is connected in parallel. The internal +1 buffer provides correct common-mode bias levels and any dynamic currents have to be absorbed by the external decoupling capacitors.

Gain Control

The gain control interface has two inputs, V_{GAIN} (Pins VGNx) and VSLP (Pins SLxx). The slope input is intended only as a decoupling pin, and the only guaranteed gain slope is the 20 dB/V default. However, if a voltage is applied to the VSLP inputs, the gain slope can be increased by reducing the slope voltage. For example, if a voltage of 1.67 V is applied to Pins SLxx, the gain slope changes to 30 dB/V. Use Equation 4 to calculate the gain slope.

$$VSLP = \frac{2.5\ \text{V} \times 20\ \text{dB/V}}{Slope} \quad (4)$$

V_{GAIN} varies the gain of the VGA through the interpolator by selecting the appropriate input stages connected to the input attenuator. The nominal V_{GAIN} range for 20 dB/V is 0 V to 3 V, with the best gain-linearity from approximately 0.5 V to 2.5 V, where the error is typically less than ±0.2 dB. For V_{GAIN} voltages above 2.5 V and less than 0.5 V, the error increases (see Figure 4). The value of the V_{GAIN} voltage can be increased to that of the supply voltage, without gain foldover.

Each channel has separate gain control pins that can be connected to a common voltage-source such as found in most ultrasound applications. For control of individual channels, connect the appropriate gain control signal to each channel.

Output Stage

Duplicate output stages of the VGA provide an 8 dB (×2.5) gain switch. The gain switch is intended to optimize the output noise floor for either a 10-bit or 12-bit ADC. The VGA gain is 20 dB (×10) in LO gain mode and 28 dB (×25) in HI gain mode. The logic setting of the HILO (Pins HLxx) selects between output amplifiers including the gain resistors and feedback buffers.

100 MHz bandwidth is maintained between the amplifiers by changing the compensation capacitance as the gain switches gain settings. Power consumption is the same for either level of gain.

In certain applications, power consumption can be reduced by lowering the supply voltage as much as possible; however, the output dynamic range is affected by the more limited swing. The fully differential signal path of the AD8335 restores 6 dB of dynamic range, and the common-mode level is maintained automatically at half the supply voltage for maximum signal swing. The differential signal has the added benefit of suppressing the even order harmonics.

The output amplifier is designed to drive a nominal differential load of 500 Ω or greater; the signal swing can be as large as 5 V p-p differential before clipping occurs. However, that distortion increases before reaching the clipping level. Distortion is shown in Figure 25 through Figure 34 for typical values of 1 V p-p or 2 V p-p (full-scale inputs for many ADCs). The output is ac-coupled to a differential anti-alias filter driving a differential ADC. Most modern ADCs have differential inputs and achieve optimum performance when driven differentially. For more information, see the Applications section.

VGA Noise

As with all X-AMPs, the output noise of the VGA is constant with gain. This causes the input referred noise to increase as the gain is decreased. This characteristic is desirable in receiver applications where wide dynamic range input signals are compressed with a fixed ceiling and noise floor into an ADC. The VGA output noise is approximately 33 nV/√Hz in LO gain mode and 2.5 times higher than this, 83 nV/√Hz, in HI gain mode. As the gain increases, the noise of the preamplifier prevails and, at the maximum VGA gain, the output noise is approximately 90 nV/√Hz and 225 nV/√Hz for LO and HI gain modes, respectively.

The output SNR is determined by the noise floor and the largest signal level, typically limited by the FS of the ADC. Modulation noise, essentially the noise introduced by the gain control input, can be troublesome. Normally one tends to look at the main amplifier signal path for noise, but a VGA is really a multiplier with the following function

$$V_{OUT} = \frac{V_{GAIN} \times V_{IN}}{V_{REF}} \quad (4)$$

where V_{REF} (bias) and V_{GAIN} (gain control interface) are both noise contributors under certain conditions. It is therefore important that the gain control signals be kept clean, especially at higher gain control slopes.

APPLICATIONS

ULTRASOUND

The primary application for the AD8335 is medical ultrasound. Figure 57 shows a simplified block diagram of an ultrasound system. The most critical function of an ultrasound system is the time gain control (TGC) compensation for physiological signal attenuation. Because the attenuation of ultrasound signals is exponential with respect to distance (time), a linear-in-dB VGA is the optimal solution.

Key requirements in an ultrasound signal chain are very low noise, active input termination, fast overload recovery, low power, and differential drive to an ADC. Because ultrasound machines use beamforming techniques requiring large binary weighted numbers (for example, 32 to 512) of channels, the lowest power at the lowest possible noise is of key importance.

Most modern machines use digital beamforming. In this technique, the signal is converted to digital format immediately following the TGC amplifier; beamforming is done digitally.

Typical ADC resolution in general purpose machines is 10 bits with sampling rates greater than 40 MSPS, while high end systems use 12 bits.

Power consumption and low cost are of primary importance in low-end and portable ultrasound machines, and the AD8335 is designed for these criteria.

For additional information regarding ultrasound systems, refer to “How Ultrasound System Considerations Influence Front-End Component Choice”, Analog Dialogue, Vol. 36, No. 3, May–July 2003. (http://www.analog.com/library/analogDialogue/archives/36-03/ultrasound/index.html)

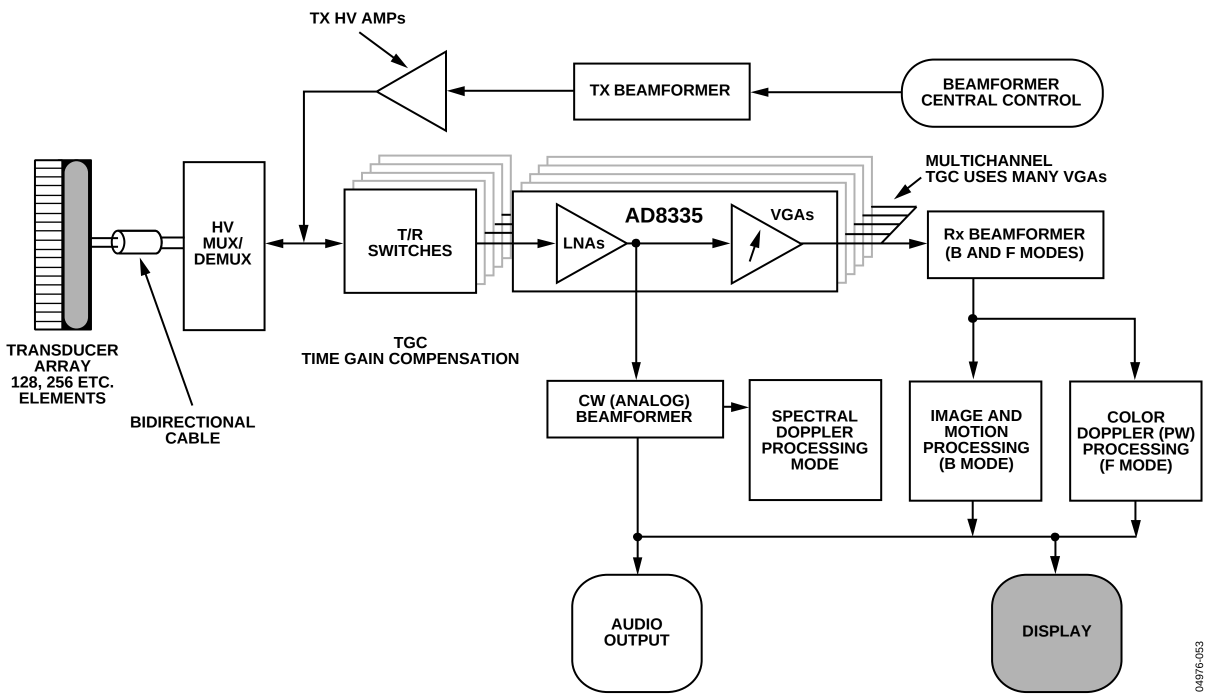


Figure 57. Simplified Ultrasound System Block Diagram

BASIC CONNECTIONS

Figure 58 shows the basic connections for the AD8335. Input signals enter from the left and output signals exit from the right, providing straight-line signal paths. Of course, a device with four differential VGAs such as this requires a multilayer printed circuit board. Power supply isolation is shown for the preamps, and for the VGA sections. If components are mounted to both sides of the board, those in the signal path should be located on the top, with power-supply decoupling components on the wiring side.

PREAMP CONNECTIONS

To configure the AD8335 for input matching a feedback resistor (R_{FB}) is ac-coupled between Pin PONx and Pin PIPx. AC coupling accommodates dissimilar common-mode voltages at the input and output ports. For values of R_{SOURCE} between 50 Ω and 200 Ω, R_{FB} is simply 5 × R_{SOURCE}. Table 6 lists a few larger values of source resistor (or R_{IN}), along with the exact value and nearest standard 1% feedback resistor. For values other those than listed in Table 6, R_{FB} can be calculated using Equation 5. For values larger than 1 kΩ, it may be advantageous to simply remove R_{FB}.

Table 6. Feedback Resistor Values for Various Input Resistances

R_{IN} (Ω)	Exact R_{FB} Value (Ω)	Nearest Standard 1% Value (Ω)
200	1014	1.02k
500	2588	2.61k
1000	5365	5.36k

$$R_{FB}\ (\Omega) = \frac{5 \times R_{IN}}{1 - \dfrac{R_{IN}}{14.7\,\mathrm{k}}} \tag{5}$$

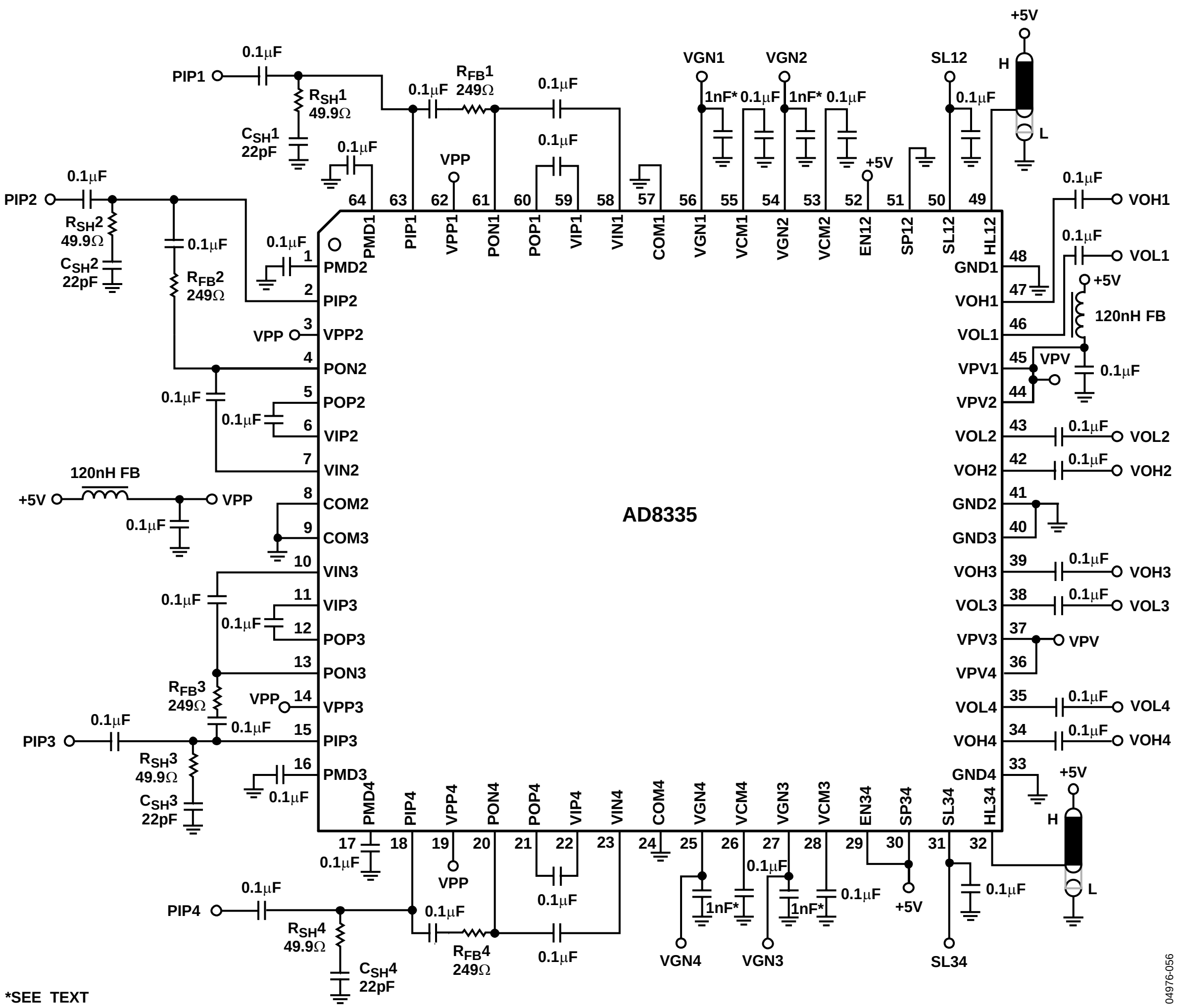


Figure 58. Basic Connections for R_{IN} = 50 Ω

The preamp PMD pins must be capacitively coupled to ground. Although the preamplifier is a differential design, the PMD pins are the internal input bias nodes and are made available for bypassing only. These pins may not be used as signal inputs.

The PIPx inputs must be capacitively coupled from the signal source because they have a nominal dc level of more than half the supply voltage. AC coupling capacitors throughout the circuit should be as large as possible for the application. Although 0.1 µF capacitors are shown in Figure 58 (and used in most positions in the evaluation board), values of these capacitors should be determined by the application. Capacitors used for coupling PMDx and PIPx pins should be the same value.

When synthesizing low values of R_{IN}, the bandwidth of the preamplifier produces some peaking at the high end of the frequency response. The optional series R_{SH}x/C_{SH}x network shown in Figure 58 flattens the response (see Figure 55). With a 50 Ω source, the resistor and capacitor values should be 49.9 Ω and 22 pF. For R_S values greater than 100 Ω, the network is not needed. The circuit is stable in either scenario.

The starred capacitors in Figure 58 (*) on the VGNx pins may be removed when faster gain control signals are required.

INPUT OVERDRIVE

Excellent overload behavior is of primary importance in ultrasound. Both the preamplifier and VGA have built-in overdrive protection and quickly recover after an overload event.

Input Overload Protection

As with any amplifier, voltage clamping prior to the inputs is highly recommended if the application is subject to high transient voltages.

A block diagram of a simplified ultrasound transducer interface is shown in Figure 59. A common transducer element serves the dual functions of transmit and receive of ultrasound energy. During the transmit phase, high voltage pulses are applied to the ceramic elements. A typical T/R (transmit/receive) switch may consist of four high voltage diodes in a bridge configuration. Although they ideally block transmit pulses from the sensitive receiver input, diode characteristics are not ideal, and resulting leakage transients impinging on the PIPx inputs can be problematic.

Since ultrasound is a pulse system, and time-of-flight is used to determine depth, quick recovery from input overloads is essential. Overload can occur in the preamp and the VGA. Immediately following a transmit pulse, the typical VGA gains are low, and the PrA is subject to overload from T/R switch leakage. With increasing gain, the VGA can become overloaded from strong echoes that occur with near field echoes and acoustically dense materials, such as bone.

Figure 59 illustrates an external overload protection scheme. A pair of back-to-back Schottky diodes is installed prior to installing the ac-coupling capacitors. Although the BAS40 is shown, many types are available and merit investigation by the user. With such diodes, clamping levels of ±0.5 V or less greatly enhance the system overload performance.

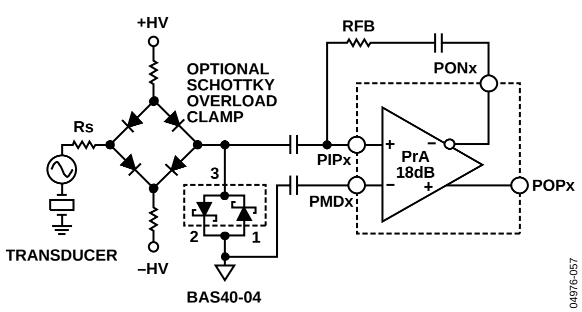


Figure 59. Input Overload Protection

LOGIC INPUTS

The enable Pins EN12 and EN34, the preamp shutdown Pins SP12 and SP34, and the HILO Pins HL12 and HL34 are all logic inputs of the AD8335. The enable inputs turn on and off each of the corresponding pairs of channels; the preamp shutdown pins do the same for the preamplifiers only; inputs HL12 and HL34 set the HILO gain for Channels 1 and 2, and Channels 3 and 4, respectively.

Shutting down the preamplifiers allows use of the VGAs alone, while reducing power consumption. The VGAs cannot be shut down independently. The SPxx (shutdown preamp) pins are logic high; thus the pins are grounded to enable the preamplifiers.

The pins can be enabled by connecting to the supply or to ground for fixed enable or disable, or to the output of a logic device. Be sure to check the data sheet of the device for voltage and current requirements.

COMMON-MODE PINS

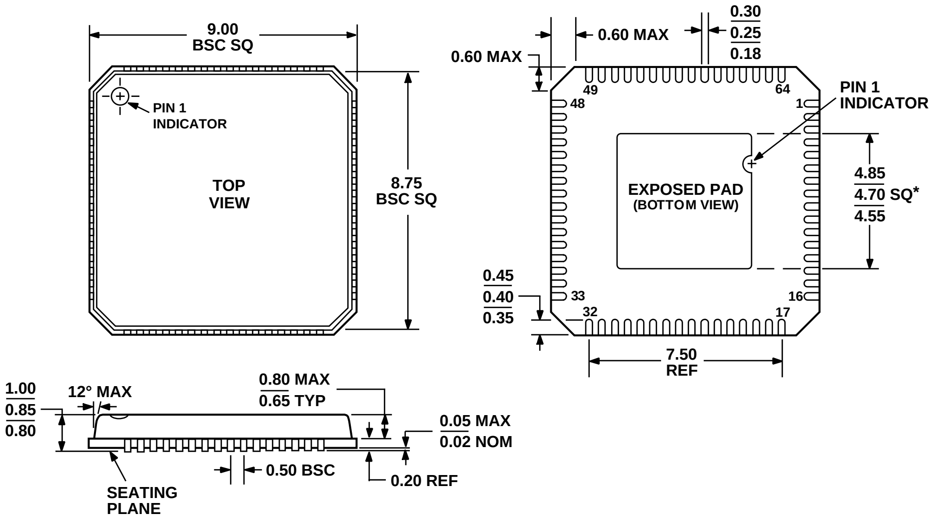
The common-mode Pins VCMx are provided for bypassing the internal common-mode reference for each channel to ground. They require a capacitor at each of the four pins and can neither be connected together nor driven by an external source.

DRIVING ADCs

The AD8335 VGA is designed to drive 10-bit and 12-bit ADCs with minimal extra components. Because the AD8335 is a single supply 5 V part and many of the newest ADCs operate from a 3 V supply, dissimilar common-mode voltages exist between the VGA output and the ADC input. This level shift is most easily accommodated by ac coupling, especially if the signal is filtered, as is the case in most ultrasound and communications applications.

When an anti-aliasing filter (AAF) is called for, it is advantageous to implement a differential configuration. A fully differential AAF requires approximately 1.5 times the number of components than a single-ended filter, because the components that in the single-ended case are tied to ground, now connect across the differential signal path. Although the series components double, the component count for the differential filter is more economical when compared to simply building a pair of single-ended filters requiring twice as many components.

OUTLINE DIMENSIONS



*COMPLIANT TO JEDEC STANDARDS MO-220-VMMD
EXCEPT FOR EXPOSED PAD DIMENSION

Figure 60. 64-Lead Lead Frame Chip Scale Package [LFCSP]
(CP-64)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8335ACPZ[1]	−40°C to +85°C	Lead Frame Chip Scale Package (LFCSP)	CP-64
AD8335ACPZ-REEL[1]	−40°C to +85°C	Lead Frame Chip Scale Package (LFCSP)	CP-64
AD8335ACPZ-REEL7[1]	−40°C to +85°C	Lead Frame Chip Scale Package (LFCSP)	CP-64
AD8335-EVAL		Evaluation Board with AD8335ACP	

[1] Z = Pb-free part.