Data Sheet | December 21, 2006 | FN9287.0

4-Channel Integrated LCD Supply with Dual V_{COM} Amplifiers

The ISL97652 represents a high power, integrated LCD supply IC targeted at large panel LCD displays. The ISL97652 integrates a high power, boost converter for A_{VDD} generation, delay switch, regulated V_{ON} and V_{OFF} charge pumps, V_{ON} slicing circuitry, a buck regulator for logic supply generation and dual high power V_{COM} amplifiers.

Operating at 650kHz or 1.3MHz, the A_{VDD} boost converter features a 2.8A boost FET. A short circuit protected A_{VDD} delay switch is integrated to provide sequencing of the A_{VDD} output. Feedback is taken from the far side of the delay FET for improved regulation and an OVP circuit protects output side components. The boost features programmable soft-start.

The asynchronous buck converter features an integrated 2.5A FET. It also operates from the 650kHz or 1.3MHz internal clock and features separate enable and soft-start control.

The dual charge pump controllers used for V_{ON} and V_{OFF} generation uses the full F_{OSC} switching frequency to allow the use of small output components for board space efficiency. V_{ON} is further processed through an integrated $V_{ON-SLICE}$ circuit for reduced flicker.

The integrated amplifiers feature high slew-rate and high output current capability. They are permanently enabled when AVIN is present.

Available in the 48 Ld 7mmx7mm QFN package, the ISL97652 is specified for ambient operation over the -40°C to +85°C temperature range.

Ordering Information

PART NUMBER (Note)	PART MARKING	TAPE & REEL	PACKAGE (Pb-Free)	PKG. DWG. #
ISL97652IRZ	ISL97652IRZ	-	48 Ld 7x7 QFN	L48.7x7
ISL97652IRZ-T	ISL97652IRZ	13” (4k pcs)	48 Ld 7x7 QFN	L48.7x7
ISL97652IRZ-TK	ISL97652IRZ	13” (1k pcs)	48 Ld 7x7 QFN	L48.7x7

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

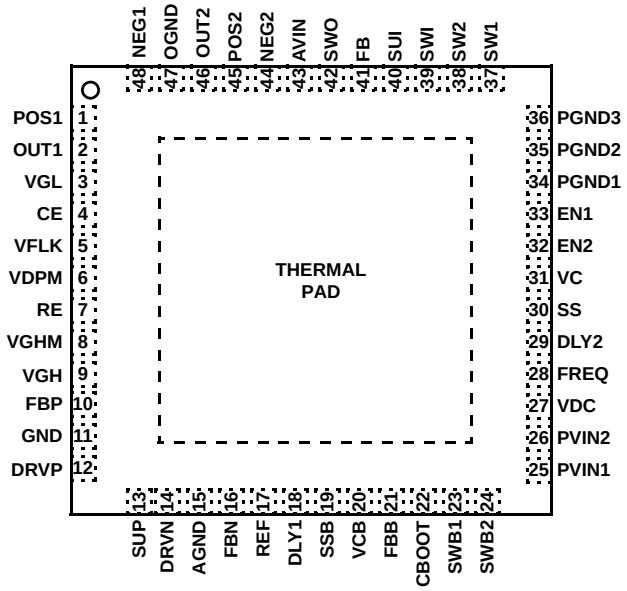
- 8V to 15V input supply
- A_{VDD} boost up to 19.5V (OVP threshold), with integrated 2.8A_{PEAK} FET
- Overvoltage protection (OVP)
- 2A integrated A_{VDD} delay FET, with short circuit protection
- Dual charge pump controllers for V_{ON} and V_{OFF}
- V_{LOGIC} buck with integrated 2.5A_{PEAK} FET
- V_{ON} slicing
- Dual high speed V_{COM} amplifiers
- 650kHz/1.3MHz switching frequency
- Integrated sequencing
- UVLO and OTP protection
- Thermally enhanced 7x7 QFN package
- Pb-free plus anneal available (RoHS compliant)

Applications

- LCD-TVs (up to 40”)
- Industrial/medical LCD displays

Pinout

ISL97652
(48 LD QFN)
TOP VIEW



Absolute Maximum Ratings (T_A = +25°C)

Maximum Pin Voltages, All Pins Except Below . . . . . -0.3 to 6.5V
SW, SUP, DRVP, DRVN, SUI, SWO, AVIN, POS1, NEG1, OUT1, POS2, NEG2, OUT2, VGL . . . . . -0.3 to 22V
SWI,SW2 . . . . . -0.3 to 24V
SUI . . . . . V(SWI) - 6.5V to V(SWI) +0.3V
PVIN, SWB, VFLK, VDPM, EN1, EN2, FREQ . . . . . -0.3 to 15.5V
VGH, VGHM. . . . . -0.3 to 36V

Recommended Operating Conditions

Input Voltage Range, V_{IN}. . . . . 8V to 15V
Boost Output Voltage, A_{VDD} . . . . . +15V
V_{ON} Output Range, V_{ON} . . . . . +15V to +32V
V_{OFF} Output Range, V_{OFF} . . . . . -15V to -5V
Logic Output Voltage Range, V_{LOGIC} . . . . . +1.5V to +3.3V
Input Capacitance, C_{IN} 2x10µF
Boost Inductor, L1 . . . . . 3.3µH-10µH
Output Capacitance, C_{OUT} 2x22µF
Buck Inductor, L2 . . . . . 3.3µH-10µH
Operating Ambient Temperature Range . . . . . -40°C to +85°C
Operating Junction Temperature Range . . . . . -40°C to +125°C

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
7x7 QFN Package (Notes 1, 2)	26	1.5

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C
Power Dissipation
$T_A \leq +25°C$ 3.7W
T_A = +70°C 2.0W
T_A = +85°C 1.4W

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

+150°C max junction temperature is intended for short periods of time to prevent shortening the lifetime. Operation close to +150°C junction may trigger the shutdown of the device even before +150°C, since this number is specified as typical.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
2. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

V_{IN} = 12V, V_{BOOST} = V_{SUP} = 15V, V_{ON} = 25V, V_{OFF} = -8V, over temperature from -40°C to +85°C, unless otherwise stated.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY PINS						
PV_{IN}	Supply Voltage		8	12	15	V
V_{SUP}	Charge Pumps Positive Supply		8		20	V
VGH	$V_{ON-SLICE}$ Positive Supply		8		30	V
AVIN	Op-AmpV Positive Supply		4.5		20	V
PI_{VIN}	Quiescent Current into PV_{IN}	Enabled, no switching		3	6	mA
		Disabled		0.5	5	µA
I_{SUP}	V_{SUP} Supply Current	Enabled, no switching and VP_{OUT} = V_{SUP}			0.5	mA
		Disabled			5	µA
I_{AVIN}	A_{VIN} Supply Current	For AVIN range			7	mA
V_{REF}	Reference Voltage	T_A = +25°C	1.252	1.265	1.278	V
			1.240	1.265	1.290	V
F_{OSC}	Oscillator Frequency for Buck, Boost, V_{ON} and V_{OFF} Functions	FREQ = V_{IN}	1100	1300	1500	kHz
		FREQ = GND	550	650	750	kHz
A_{VDD} BOOST						
I_{BOOST}	Boost Switch Peak Current	Boost Peak Current limit	2.8			A
EFF_{BOOST}	Peak Efficiency	See graphs and component recommendations		91		%

Electrical Specifications V_{IN} = 12V, V_{BOOST} = V_{SUP} = 15V, V_{ON} = 25V, V_{OFF} = -8V, over temperature from -40°C to +85°C, unless otherwise stated. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
$r_{DS(ON)}$	Switch On Resistance			125	200	mΩ
$\Delta V_{BOOST}/\Delta V_{IN}$	Line Regulation	Vin = 8V to 12V at Iload=200mA, see “Typical Performance Curves” on page 6		0.08		%
$\Delta V_{BOOST}/\Delta I_{OUT}$	Load Regulation	100mA to 500mA, see “Typical Performance Curves” on page 6		0.5		%
V_{FB}	Boost Feedback Voltage	T_A = +25°C	1.252	1.265	1.278	V
			1.240	1.265	1.290	V
Dmax_boost	Boost Maximum Duty Cycle	FOSC = 650kHz		90		%
		FOSC = 1.3MHz		85		%
Dmin_boost	Boost Minimum Duty Cycle	FOSC = 650kHz		10		%
		FOSC = 1.3MHz		20		%
A_{VDD} DELAY SWITCH						
R_{PD}	$R_{DS(ON)}$			180	240	mΩ
SWI_{MAX}	Maximum SWI Voltage		21			V
IdelayFET	Delay FET RMS Current Limit		1.5	2		A
FETtimeout	Delay FET Fault Timeout	I(SWO) > IdelayFET		100		µs
Ipull-Down	Pull-down Current Applied to FET Gate and SUI			65		µA
V_{GATE}	SUI Voltage When Switch is Fully Switched On			V(SWI) - 5		V
SWI_{LEAK}	SWI Leakage Current When Disabled	V_{IN} = 15V, SWI = 21V, SWO = 0V, EN1 = EN2 = 0V			1	µA
VDS_{OK}	Drain Source Voltage When Boost is Enabled	SWI =16.5V		15.7		V
VDS_{HYS}	Hysteresis on VDS_{OK} Spec	SWI =16.5V		1.4		V
V_{LOGIC} BUCK						
I_{BUCK}	Buck Switch Current	Current limit	2.5			A
EFF_{BUCK}	Peak Efficiency	See graphs and component recommendations		85		%
$R_{DS(ON)\ BK}$	Switch On Resistance			170	250	mΩ
$\Delta V_{BUCK}/\Delta V_{IN}$	Line Regulation	Vin = 8V to 12V at Iload = 200mA, see “Typical Performance Curves” on page 6		0.05		%
$\Delta V_{BUCK}/\Delta I_{OUT}$	Load Regulation	200mA to 1000mA, see “Typical Performance Curves” on page 6		0.1		%
V_{FBB}	FBL Regulation Voltage	T_A = +25°C	1.252	1.265	1.278	V
			1.240	1.265	1.290	V
Dmax_buck	Buck Maximum Duty Cycle	F_{OSC} = 650kHz		90		%
		F_{OSC} = 1.3MHz		85		%
Dmin_buck	Buck Minimum Duty Cycle	F_{OSC} = 650kHz		10		%
		F_{OSC} = 1.3MHz		20		%
NEGATIVE (V_{OFF}) CHARGE PUMP						
V_{OFF}	V_{OFF} Output Voltage Range	1X Charge Pump	V_{SUP} + 1.4V		0	V
ILoad_NCP_min	External Load Driving Capability	V_{SUP} >5V	30			mA

Electrical Specifications V_{IN} = 12V, V_{BOOST} = V_{SUP} = 15V, V_{ON} = 25V, V_{OFF} = -8V, over temperature from -40°C to +85°C, unless otherwise stated. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
Ron(DRVN)H	High-Side Driver ON Resistance at DRVN	I(DRVN) = +60mA			11	Ω
RON(DRVN)L	Low-Side Driver ON Resistance at DRVN	I(DRVN) = -60mA			10	Ω
Ipu(DRVN)lim	Pull-Up Current Limit in DRVN	V(DRVN) = 0V to V(SUP)-0.5V	60	270		mA
Ipd(DRVN)lim	Pull-Down Current Limit in DRVN	V(DRVN) = 0.36V to V(VSUP)		-200	-60	mA
I(DRVN)leak	Leakage Current in DRVN	V(FBN) < 0 or EN1 = LOW	-2		2	µA
V_{FBN}	FBN Regulation Voltage	T_A = +25°C	0.48	0.5	0.52	V
			0.47	0.5	0.53	V
D_NCP_max	Max Duty Cycle of the Negative Charge Pump			50		%
Rpd(FBN)off	Pull-Down Resistance, Not Active	I(FBN) = 500µA	2.5	3.5	4.5	kΩ
POSITIVE (V_{ON}) CHARGE PUMP						
V_{ON}	V_{ON} Output Voltage Range	2X or 3X charge pump	V_{SUP} + 2V		34	V
ILoad_PCP_min	External Load Driving Capability		30			mA
Ron(DRVP)H	High-Side Driver ON Resistance at DRVP	I(DRVP) = +60mA			11	Ω
Ron(DRVP)L	Low-Side Driver ON Resistance at DRVP	I(DRVP) = -60mA			10	Ω
Ipu(DRVP)lim	Pull-Up Current Limit in DRVP	V(DRVP) = 0V to V(SUP)-0.5V	60	270		mA
Ipd(DRVP)lim	Pull-Down Current Limit in DRVP	V(DRVP) = 0.36V to V(VSUP)		-200	-60	mA
I(DRVP)leak	Leakage Current in DRVP	VFBP > VREF or EN1 or EN2 = low	-2		2	µA
V_{FBP}	FBP Regulation Voltage	T_A = +25°C	1.225	1.25	1.275	V
			1.22	1.25	1.28	V
D_PCP_max	Max Duty Cycle of the Positive Charge Pump			50		%
LOGIC INPUTS						
VHI	Logic “HIGH”	EN1, EN2, VFLK, VDPM	2.0			V
VLO	Logic “LOW”	EN1, EN2, VFLK, VDPM			0.8	V
IL_pd	Logic Pin Pull-Down Current	V_{LOGIC} > VLO			25	µA
V_{ON} SLICE						
VGH	VGH Voltage		8		30	V
I_{VGH}	VGH Input Current	VFLK = 0, RE=33K		300		µA
		VFLK = 5V, RE=33K		40		µA
VGL	VGL Voltage		3		VGH - 2	V
I_{VGL}	VGL Input Current		-2	0.1	2	µA
R_{ONVGH}	VGH to VGH_M On Resistance			15	30	Ω
T_{DEL}	DELAY Time	CE = 470pF		10		µs
VCOM AMPLIFIERS						
Icont	Maximum Continuous Current Per Amplifier		50			mA
V_{SAMP}	Supply Voltage		4.5		20	V
I_{SAMP}	Supply Current per amplifier			3		mA
V_{OS}	Offset Voltage			3	20	mV
I_B	Noninverting Input Bias Current per amplifier			0	150	nA
CMIR	Common Mode Input Voltage Range		0		AVIN	V

Electrical Specifications V_{IN} = 12V, V_{BOOST} = V_{SUP} = 15V, V_{ON} = 25V, V_{OFF} = -8V, over temperature from -40°C to +85°C, unless otherwise stated. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
CMRR	Common-Mode Rejection Ratio		50	70		dB
PSRR	Power Supply Rejection Ratio		70	85		dB
VOH	Output Voltage Swing High	$I_{OUT(SOURCE)}$ = 5mA		AVIN - 50		mV
VOH	Output Voltage Swing High	$I_{OUT(SOURCE)}$ = 50mA		AVIN - 450		mV
VOL	Output Voltage Swing Low	$I_{OUT(SINK)}$ = 5mA		50		mV
VOL	Output Voltage Swing Low	$I_{OUT(SINK)}$ = 50mA		450		mV
I_{SC}	Output Short Circuit Current per amplifier		300	400		mA
SR	Slew Rate			50		V/µs
BW	Gain Bandwidth	-3dB gain point		30		MHz
FAULT DETECTION THRESHOLDS						
OVP	Overvoltage Protection Threshold	AVDD rising	18.8	19.5	20	V
OVP_{HYS}	Overvoltage Protection Threshold Hysteresis			0.8		V
VLOR	Undervoltage Lockout Threshold	PV_{IN} rising		7.8	8.0	V
VLOF	Undervoltage Lockout Threshold	PV_{IN} falling	7.4	7.6		V
T_{OFF}	Thermal Shut-Down	Temperature rising		150		°C
T_{ON}	Reset after Thermal Shut-Down	Temperature falling		100		°C
Vth_A_{VDD}(FB)	A_{VDD} Boost Short Detection	V(FBFBB) falling less than		1.14		V
Vth_V_{LOGIC}(FBB)	V_{LOGIC} Buck Short Detection	V(FBB) falling less than		1.14		V
Vth_POUT(FBP)	P_{OUT} Charge Pump Short Detection	V(FBP) falling less than		1.14		V
Vth_NOUT(FBN)	N_{OUT} Charge Pump Short Detection	V(FBN) rising more than		0.525		V
TFD	Fault Delay Time to Chip Turns Off			64		µs
START-UP SEQUENCING						
ISS	SS, SSB Current	SS, SSB ≤1.5V		6		µA
IDLY	DLY1, DLY2 Current	DLY1, DLY2 <1.5V		6		µA
SSTH1	SS, SSB Voltage to Give Max Current Limit			1.27		V
SSTH2	SS, SSB Voltage to Enable Fault Checking			2.05		V
DELTH1	DEL1, DEL2 Voltage to Give Max Current Limit			1.27		V
DELTH2	DEL1, DEL2 Voltage to Enable Fault Checking			2.05		V

Typical Performance Curves

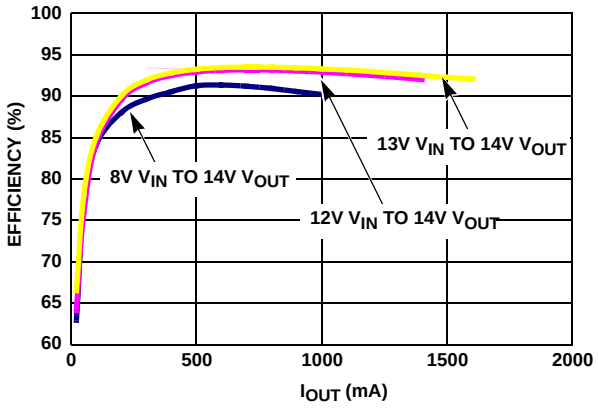


FIGURE 1. BOOST EFFICIENCY @ 650kHz

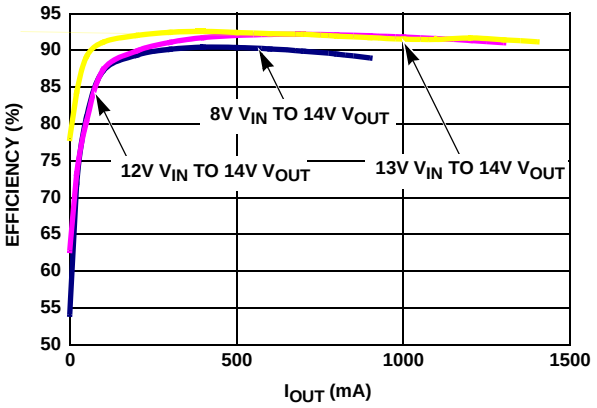


FIGURE 2. BOOST EFFICIENCY @ 1.3MHz

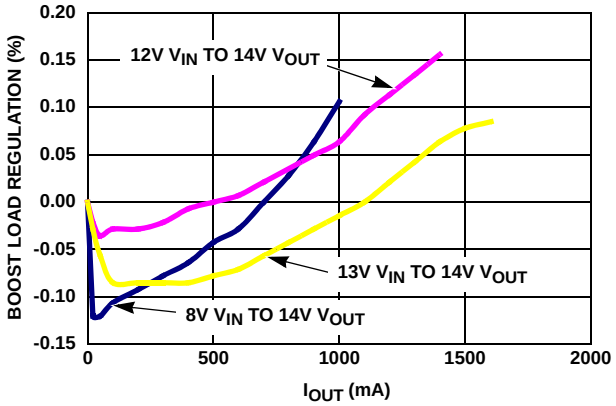


FIGURE 3. BOOST LOAD REGULATION @ 650kHz

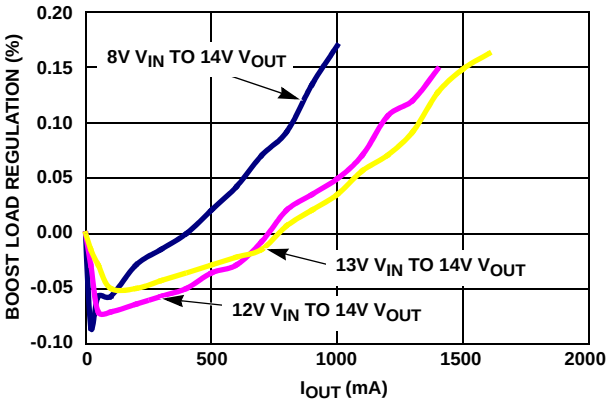


FIGURE 4. BOOST LOAD REGULATION @ 1.3MHz

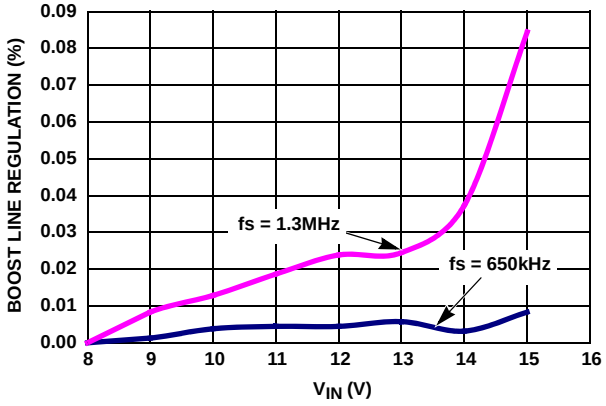


FIGURE 5. BOOST LINE REGULATION

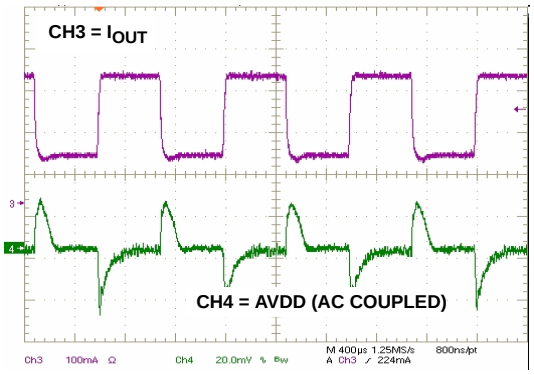


FIGURE 6. BOOST TRANSIENT RESPONSE @ 650kHz

Typical Performance Curves (Continued)

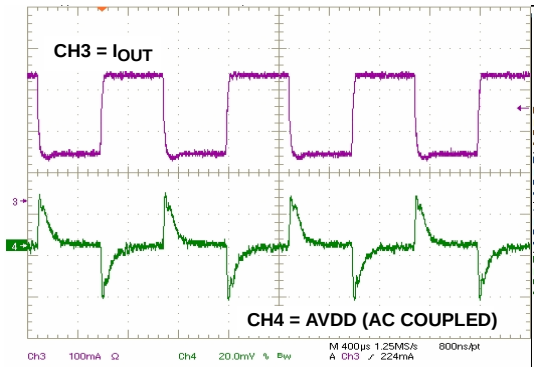


FIGURE 7. BOOST TRANSIENT RESPONSE @ 1.3MHz

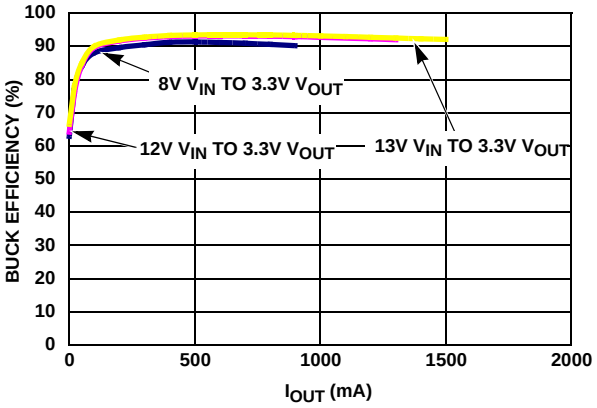


FIGURE 8. BUCK EFFICIENCY @ 650kHz

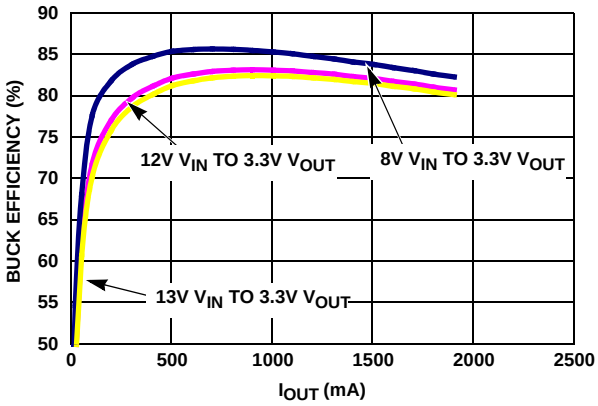


FIGURE 9. BUCK EFFICIENCY @ 1.3MHz

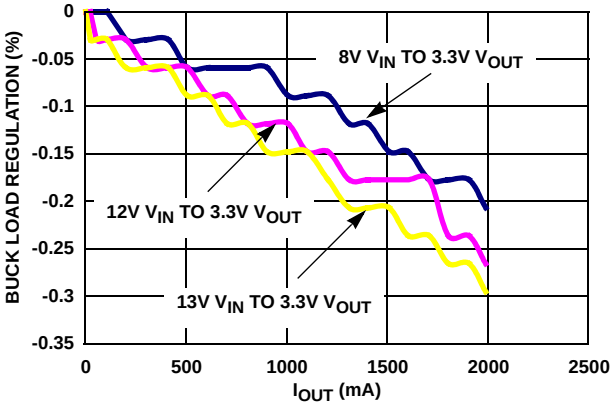


FIGURE 10. BUCK LOAD REGULATION @ 650kHz

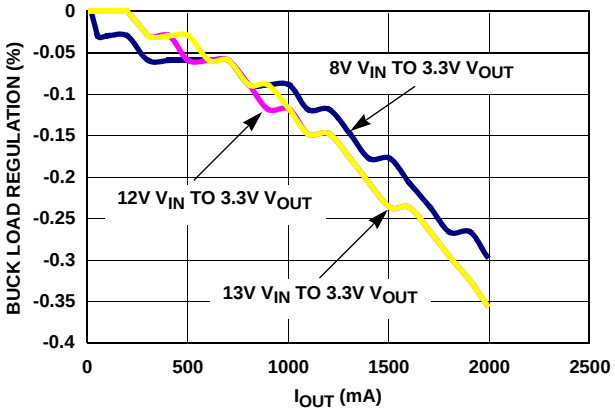


FIGURE 11. BUCK LOAD REGULATION @ 1.3MHz

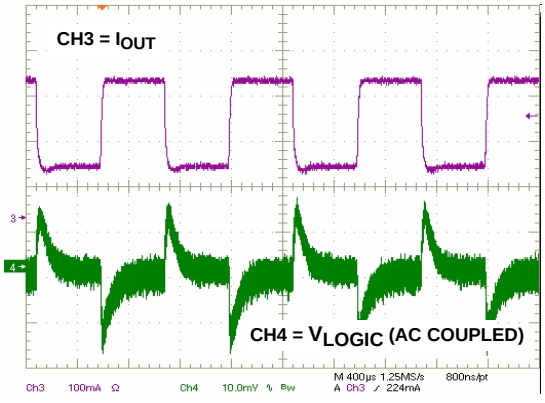


FIGURE 12. BUCK TRANSIENT RESPONSE @ 650kHz

Typical Performance Curves (Continued)

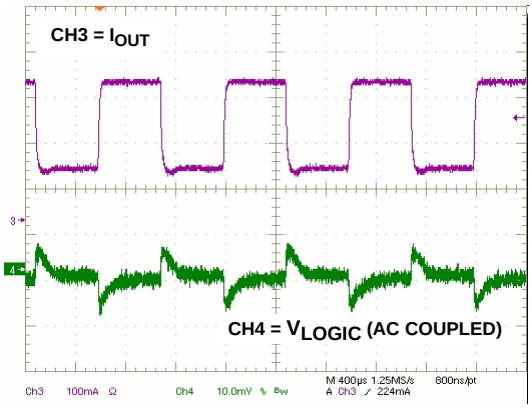


FIGURE 13. BUCK TRANSIENT RESPONSE @ 1.3MHz

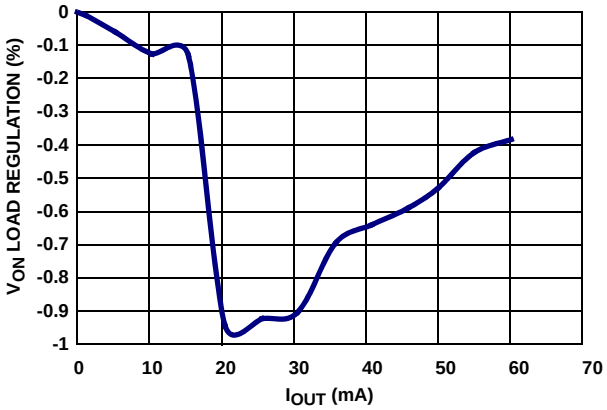


FIGURE 14. V_{ON} LOAD REGULATION

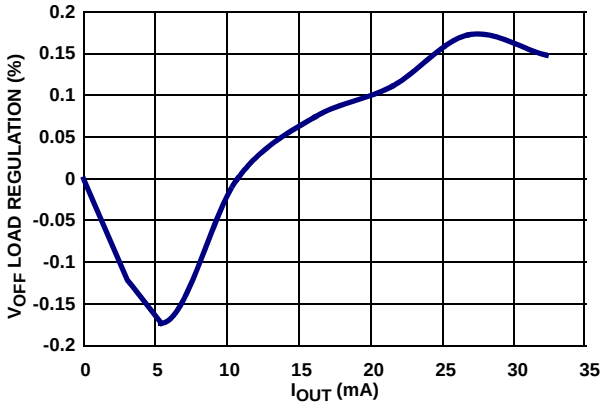


FIGURE 15. V_{OFF} LOAD REGULATION

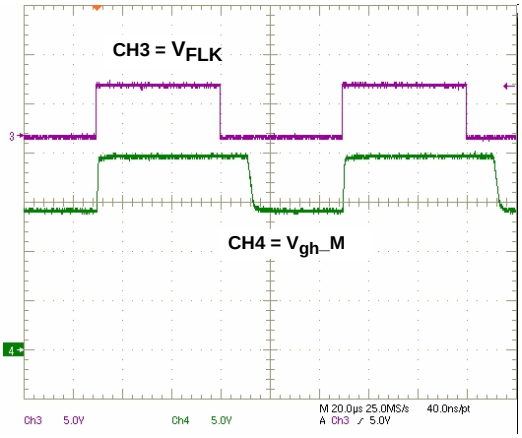


FIGURE 16. GPM WAVEFORM

+

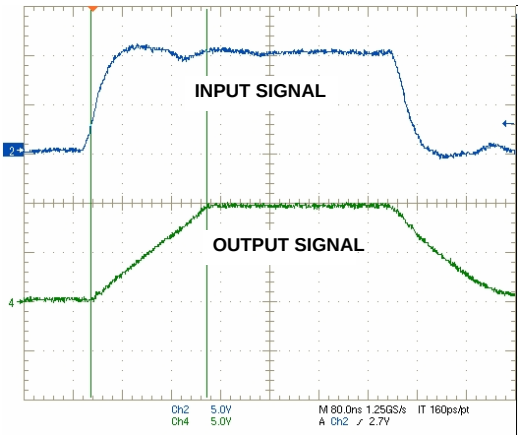
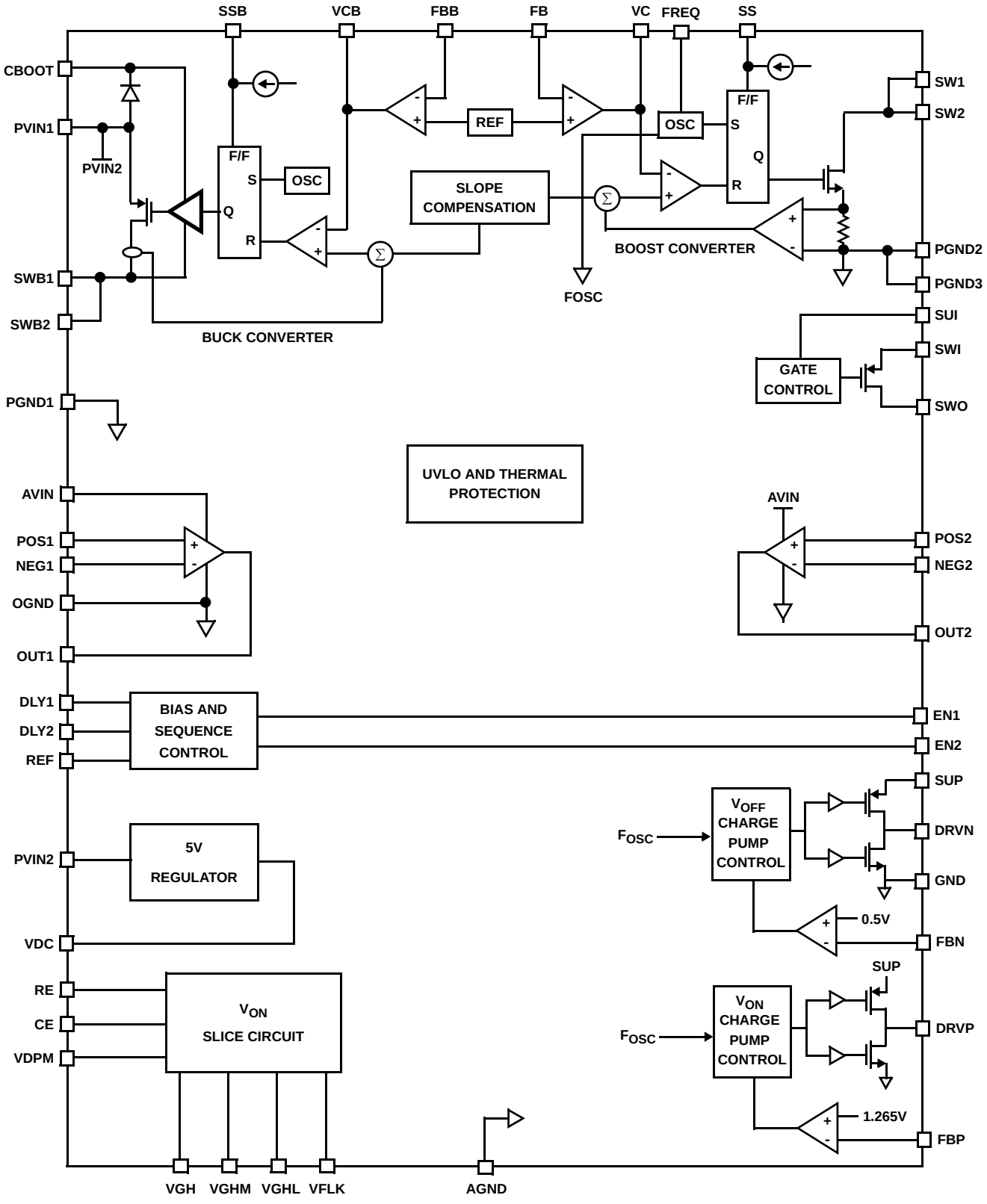


FIGURE 17. V_{COM} RISING SLEW RATE

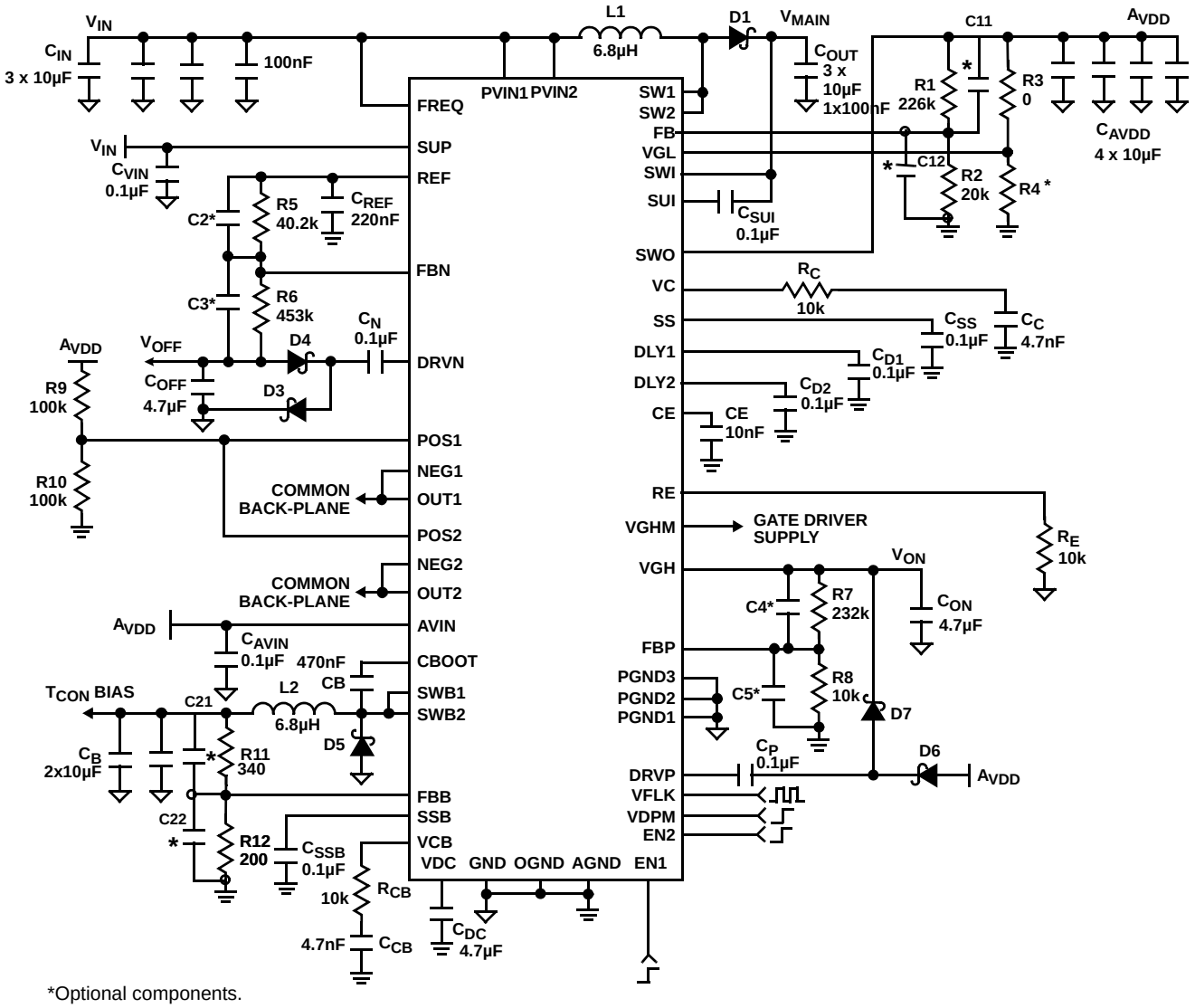
Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1	POS1	Op-amp 1 non-inverting input
2	OUT1	Op-amp 1 output
3	VGL	GPM lower supply pin
4	CE	GPM delay pin
5	VFLK	GPM control pin
6	VDPM	GPM enable pin
7	RE	GPM output voltage slope adjust pin
8	VGHM	GPM output voltage
9	VGH	GPM higher supply pin
10	FBP	Positive charge pump feedback voltage
11	GND	Positive and negative charge pump Ground connection
12	DRVP	Positive charge pump driver output pin
13	SUP	Positive and negative charge pump supply
14	DRVN	Negative charge pump driver output pin
15	AGND	Device analog Ground
16	FBN	Negative charge pump feedback voltage
17	REF	Reference voltage for all internal functions and external V_{OFF} feedback
18	DLY1	Buck and negative charge pump delay pin
19	SSB	Buck soft-start pin
20	VCB	Buck compensation pin
21	FBB	Buck feedback voltage
22	CBOOT	Buck boot-strap capacitor
23, 24	SWB1, SWB2	Buck FET source connection
25, 26	PVIN1, PVIN2	Input supply
27	VDC	Internal regulated 5V supply - attach external decoupling capacitor
28	FREQ	Switching frequency select pin
29	DLY2	Boost and positive charge pump delay pin
30	SS	Boost soft-start pin
31	VC	Boost compensation pin
32	EN2	Boost and positive charge pump enable
33	EN1	Buck and negative charge pump enable
34	PGND1	Device power GND
35, 36	PGND2, PGND3	Boost FET source connection
37, 38	SW1, SW2	Boost FET drain connection
39	SWI	A_{VDD} delay switch source connection
40	SUI	A_{VDD} start-up in-rush control
41	FB	Boost feedback voltage
42	SWO	A_{VDD} delay switch drain connection
43	AVIN	VCOM amplifier positive supply pin
44	NEG2	Op-amp 2 inverting input
45	POS2	Op-amp 2 non-inverting input
46	OUT2	Op-amp 2 output
47	OGND	Op-amp ground
48	NEG1	Op-amp 1 inverting input

Block Diagram



Typical Application Diagram



*Optional components.

NOTE: Separate PGND and SGND planes must be used, see PCB layout procedure section.

Applications Information

The ISL97652 provides a complete power solution for TFT LCD applications. The system consists of one boost converter to generate A_{VDD} voltage for column drivers, one buck converter to provide voltage to logic circuit in the LCD panel, integrated V_{ON} and V_{OFF} charge pump controllers, A_{VDD} delay FET, $V_{ON-SLICE}$ and dual high speed VCOM amplifiers. With the high output current capability, this part is ideal for big screen LCD TV and monitor panel application.

The integrated boost converter and buck converter operate at either 650kHz or 1.3MHz which allow the use of multilayer ceramic capacitors and low profile inductor which result in low cost, compact and reliable system.

Boost Converter

The boost converter is a current mode PWM converter operating at either 650kHz or 1.3MHz. 650kHz operation allows operation down to lower duty cycles. It can operate in both discontinuous conduction mode (DCM) at light load or when operating duty cycle is lower than the minimum duty cycle and continuous mode (CCM). In continuous current mode, current flows continuously in the inductor during the entire switching cycle in steady state operation. The voltage conversion ratio in continuous current mode is given by:

$$\frac{V_{BOOST}}{V_{IN}} = \frac{1}{1-D} \quad \text{(EQ. 1)}$$

Where D is the duty cycle of the switching MOSFET.

The boost converter uses a summing amplifier architecture consisting of gm stages for voltage feedback, current feedback and slope compensation. A comparator looks at the peak inductor current cycle by cycle and terminates the PWM cycle if the current limit is reached.

An external resistor divider is required to divide the output voltage down to the nominal reference voltage. Current drawn by the resistor network should be limited to maintain the overall converter efficiency. The maximum value of the resistor network is limited by the feedback input bias current and the potential for noise being coupled into the feedback pin. A resistor network in the order of 60kΩ is recommended. The boost converter output voltage is determined by the following equation:

$$V_{BOOST} = \frac{R_1 + R_2}{R_2} \times V_{FB} \quad \text{(EQ. 2)}$$

The current through the MOSFET is limited to 2.8Apeak. This restricts the maximum output current (average) based on the following equation:

$$I_{OMAX} = \left(I_{LMT} - \frac{\Delta I_L}{2}\right) \times \frac{V_{IN}}{V_O} \quad \text{(EQ. 3)}$$

Where ΔIL is peak to peak inductor ripple current, and is set by:

$$\Delta I_L = \frac{V_{IN}}{L} \times \frac{D}{f_S} \quad \text{(EQ. 4)}$$

where f_S is the switching frequency

The following table gives typical values (margins are considered 10%, 3%, 20%, 10% and 15% on V_{IN}, V_O, L, f_S and I_{OMAX}):

TABLE 1. MAXIMUM OUTPUT CURRENT CALCULATION

V_{IN} (V)	V_O (V)	L (µH)	f_S (MHz)	I_{OMAX} (mA)
12	15	6.8	0.65	1890
12	15	6.8	1.3	1955
12	18	6.8	0.65	1500
12	18	6.8	1.3	1590
8	15	6.8	0.65	1200
8	15	6.8	1.3	1275
8	18	6.8	0.65	950
8	18	6.8	1.3	1050

When operating at the lower frequency option, 650kHz, the potential increase in ripple current in the inductor can be avoided by increasing the inductor by the same factor. This allows the slope compensation in the boost feedback to remain the same as the 1.3MHz case and this will maintain stability of the converter over the widest operating range. Operation at 650kHz allows boost operation down to lower minimum duty cycles, where the output voltage required is closer to the input voltage than can be achieved when the higher frequency option is selected. The minimum boost duty cycle of the ISL97652 is ~10% for 650kHz and ~20% for 1.3MHz. When the operating duty cycle is lower than the minimum duty cycle, the part will not switch in some cycles randomly, which will cause some LX pulses to be skipped. In this cas, LX pulses are not consistent any more, but the output voltage (A_{VDD}) is still regulated by the ratio of R1 and R2. Because some LX pulses are skipped, the ripple current in the inductor will become bigger. Under the worst case, the ripple current will be from 0 to the threshold of the current limit. In turn, the bigger ripple current will increase the output voltage ripple. Hence, it will need more output capacitors to keep the output ripple at the same level. When the input voltage equals, or is larger than, the output voltage, the boost converter will stop switching. The boost converter is not regulated any more, but the part will still be on and other channels are still regulated.

Boost Converter Input Capacitor

An input capacitor is used to suppress the voltage ripple injected into the boost converter. A ceramic capacitor with capacitance larger than 10µF is recommended. The voltage rating of input capacitor should be larger than the maximum input voltage. Some capacitors are recommended in Table 2 for input capacitor.

TABLE 2. BOOST CONVERTER INPUT CAPACITOR RECOMMENDATION

CAPACITOR	SIZE	VENDOR	PART NUMBER
10µF/25V	1210	TDK	C3225X7R1E106M
10µF/25V	1210	Murata	GRM32DR61E106K

Boost Inductor

The boost inductor is a critical part which influences the output voltage ripple, transient response, and efficiency. Values of 3.3µH to 10µH should be selected to match the internal slope compensation. The inductor must be able to handle the following average and peak current:

$$I_{LAVG} = \frac{I_O}{1 - D} \quad \text{(EQ. 5)}$$

$$I_{LPK} = I_{LAVG} + \frac{\Delta I_L}{2} \quad \text{(EQ. 6)}$$

Some inductors are recommended in Table 3.

TABLE 3. BOOST INDUCTOR RECOMMENDATION

INDUCTOR	DIMENSIONS (mm)	VENDOR	PART NUMBER
6.8µH/ $3A_{PEAK}$	7.3x6.8x3.2	TDK	RLF7030T-6R8N3R0
6.8µH/ $2.9A_{PEAK}$	7.6X7.6X3.0	Sumida	CDR7D28MNNP-6R8NC
5.2µH/ $4.55A_{PEAK}$	10x10.1x3.8	Cooper Bussmann	CD1-5R2

Rectifier Diode (Boost Converter)

A high-speed diode is necessary due to the high switching frequency. Schottky diodes are recommended because of their fast recovery time and low forward voltage. The reverse voltage rating of this diode should be higher than the maximum output voltage. The rectifier diode must meet the output current and peak inductor current requirements. The following table is some recommendations for boost converter diode.

TABLE 4. BOOST CONVERTER RECTIFIER DIODE RECOMMENDATION

DIODE	V_R/I_{AVG} RATING	PACKAGE	VENDOR
SS23	30V/2A	SMB	Fairchild Semiconductor
SL23	30V/2A	SMB	Vishay Semiconductor

Output Capacitor

The output capacitor supplies the load directly and reduces the ripple voltage at the output. Output ripple voltage consists of two components: the voltage drop due to the inductor ripple current flowing through the ESR of output capacitor, and the charging and discharging of the output capacitor.

$$V_{RIPPLE} = I_{LPK} \times ESR + \frac{V_O - V_{IN}}{V_O} \times \frac{I_O}{C_{AVDD}} \times \frac{1}{f_s} \quad \text{(EQ. 7)}$$

For low ESR ceramic capacitors, the output ripple is dominated by the charging and discharging of the output capacitor. The voltage rating of the output capacitor should be greater than the maximum output voltage.

Note: Capacitors have a voltage coefficient that makes their effective capacitance drop as the voltage across then increases. C_{OUT} in Equation 7 above assumes the effective value of the capacitor at a particular voltage and not the manufacturer's stated value, measured at zero volts.

The following table shows some selections of output capacitors.

TABLE 5. BOOST OUTPUT CAPACITOR RECOMMENDATION

CAPACITOR	SIZE	VENDOR	PART NUMBER
10µF/25V	1210	TDK	C3225X7R1E106M
10µF/25V	1210	Murata	GRM32DR61E106K

Loop Compensation (Boost Converter)

The boost converter of ISL97652 can be compensated by a RC network connected from V_C pin to ground. C_C = 4.7nF and R_C = 10k RC network is used in the demo board. A higher resistor value can be used to lower the transient load change A_{VDD} overshoot - however, this may be at the expense of stability to the loop.

The stability can be examined by repeatedly changing the load between 100mA and a max level that is likely to be used in the system being used. The A_{VDD} voltage should be examined with an oscilloscope set to AC 100mV/div and the amount of ringing observed when the load current changes. Reduce excessive ringing by reducing the value of the resistor in series with the VC pin capacitor.

A_{VDD} Delay Switch

The ISL97652 integrates a PMOS disconnect switch for the A_{VDD} boost output to disconnect V_{IN} from A_{VDD} when the EN2 input is not selected. When EN2 is taken high, the PMOS FET is turned on to connect power to the display. The CSUI capacitor provide soft-start control for the connection of this switch.

The operation of the AVDD delay switch is controlled by internal VDSOK and VDSHYS control signals which operate as follows:

During start-up (or during fault conditions):

VDSOK goes to 1 when V(SWI - SWO) becomes less than ~0.5V. This will turn-on the boost function.

VDSOK goes to 0 when VDS_pfet becomes greater than ~1.1V. This will turn-off the boost function.

The threshold voltages have a Vin dependence such that:

For Vin1 = 8V: VDSOK goes to 1 occurs at ~0.5V and VDSOK goes to 0 occurs at ~1.1V.

For Vin1 =18.5V: VDSOK goes to1 occurs at ~1.13V and VDSOK goes to 0 occurs at ~2.65V.

V(SWI - SWO) is the VDS voltage across the internal PFET protection switch. If this voltage exceeds 1.1V for some reason (e.g. under fault conditions or during start-up if VMAIN rises faster than AVDD) the boost is turned-off to allow the AVDD (SWO) potential to catch-up with VMAIN (SWI).

VDSHYS is the VDS hysteresis level;

Once VDSOK goes to 1 the voltage V(SWI - SWO) then needs to exceed 1.1V for VDSOK goes to 0.

During normal operation VDS will be ~Ron_PFET * Iload (~ 0.18x2 = 0.36V for max AVDD load).

If a fault develops on AVDD, which causes VDS to exceed 1.1V, then the boost operation is interrupted by the internal VDSOK goes to 0 signal and fault timers will start to operate while the rising/falling character of AVDD is monitored.

A_{VDD} Delay Switch Fault Operation

When enabled, the gate of the PFET is pulled down with a 30µA current, turning on the FET switch. The speed of this turn-on can be controlled by placing a capacitor from SWI to SUI. In normal operation the gate (and SUI pin) are pulled down to 5V below SWI. The A_{VDD} delay switch circuitry constantly monitors both the current in the switch and the voltage at SWO. If the current exceeds the current limit of 2A, the gate of the FET (and also the SUI pin) will be pulled up to the correct level to limit the current to 2A. In this mode the switch acts like a 2A current source. this current cannot be maintained indefinitely due to the power dissipation on

chip. Therefore, three separate fault mechanisms are operated.

1. The SWO output range is constantly monitored and expected to rise if the PFET is in current limit. The rate of rise at SWO can be calculated from the current limit and the capacitance on SWO by using the equation dV/dt = Ilimit/Cavdd. The SWO voltage range is split into sections of approximately 0.7V such that every time the output rises by this amount the circuit detects that the voltage is rising. Should the circuit remain in current limit for more than 100µs with no such rise taking place the circuit will fault out. In this scenario, the PFET will immediately switch itself off and the rest of the ISL97652 will later fault out due to the boost voltage at A_{VDD} falling away.
2. As well as monitoring any rise in the voltage at SWO, the circuit also monitors any falls in this level. If the output falls by more than a certain amount while it is in current limit the circuit will fault out immediately. This amount varies from about 1V to about 1.4V depending on the output level before the fall. In this scenario, the PFET will immediately switch itself off and the rest of the ISL97652 will later fault out due to the boost voltage falling away.
3. Once the ISL97652 has successfully sequenced the boost on and the boost soft-start capacitor has charged up, a third fault check is also added. After this point if the PFET enters current limit for greater than the global timeout of 40µs then the chip will fault out. In this scenario the whole chip will be disabled with the PFET immediately switched off.

Buck Converter

The buck converter is the step down converter, which supplies the current to the logic circuit of the LCD system. The ISL97652 integrates an 20V N-Channel MOSFET to save cost and reduce external component count. In the continuous current mode, the relationship between input voltage and output voltage is as follows:

$$\frac{V_{LOGIC}}{V_{IN}} = D \quad \text{(EQ. 8)}$$

Where D is the duty cycle of the switching MOSFET. Because D is always less than 1, the output voltage of buck converter is lower than input voltage.

The peak current limit of buck converter is set to 2.5A, which restricts the maximum output current (average) based on the following equation:

$$I_{OMAX} = 2.5A - \Delta I_{PP} \quad \text{(EQ. 9)}$$

Where ΔI_{PP} is the ripple current in the buck inductor as the following equation:

$$\Delta I_{PP} = \frac{V_{LOGIC}}{L \cdot f_s} \cdot (1 - D) \quad \text{(EQ. 10)}$$

Where L is the buck inductor, f_S is the switching frequency.

Feedback Resistors

The buck converter output voltage is determined by the following equation:

$$V_{LOGIC} = \frac{R_{11} + R_{12}}{R_{12}} \times V_{FBB} \quad \text{(EQ. 11)}$$

Where R11 and R12 are the feedback resistors of buck converter to set the output voltage. Current drawn by the resistor network should be limited to maintain the overall converter efficiency. The maximum value of the resistor network is limited by the feedback input bias current and the potential for noise being coupled into the feedback pin. A resistor network in the order of 1kΩ is recommended.

Buck Converter Input Capacitor

The capacitor should support the maximum AC RMS current which happens when D = 0.5 and maximum output current.

$$I_{ACRMS}(C_{IN}) = \sqrt{D \cdot (1 - D)} \cdot I_O \quad \text{(EQ. 12)}$$

Where I_0 is the output current of the buck converter. The following table shows some recommendations for input capacitor.

TABLE 6. INPUT CAPACITOR (BUCK) RECOMMENDATION

CAPACITOR	SIZE	VENDOR	PART NUMBER
10µF/16V	1206	TDK	C3216X7R1C106M
10µF/10V	0805	Murata	GRM21BR61A106K
22µF/16V	1210	Murata	C3225X7R1C226M

Buck Inductor

An 3.3µH-10µH inductor is the good choice for the buck converter. Besides the inductance, the DC resistance and the saturation current are also the factor needed to be considered when choosing buck inductor. Low DC resistance can help maintain high efficiency, and the saturation current rating should be 2.5A. Here are some recommendations for buck inductor.

TABLE 7. BUCK INDUCTOR RECOMMENDATION

INDUCTOR	DIMENSIONS (mm)	VENDOR	PART NUMBER
4.7µH/ $2.7A_{PEAK}$	5.7x5.0x4.7	Murata	LQH55DN4R7M01K
6.8µH/ $3A_{PEAK}$	7.3x6.8x3.2	TDK	RLF7030T-6R8M2R8
10µH/ $2.4A_{PEAK}$	12.95x9.4x3.0	Coilcraft	DO3308P-103

Rectifier Diode (Buck Converter)

A Schottky diode is recommended due to fast recovery and low forward voltage. The reverse voltage rating should be higher

than the maximum input voltage. The peak current rating is 2A, and the average current should be as the following equation,

$$I_{AVG} = (1 - D)*I_o \quad \text{(EQ. 13)}$$

Where I_o is the output current of buck converter. The following table shows some diode recommended.

TABLE 8. BUCK RECTIFIER DIODE RECOMMENDATION

DIODE	V_R/I_{AVG} RATING	PACKAGE	VENDOR
PMEG2020EJ	20V/2A	SOD323F	Philips Semiconductors
SS22	20V/2A	SMB	Fairchild Semiconductor

Output Capacitor (Buck Converter)

Four 10µF or two 22µF ceramic capacitors are recommended for this part. The overshoot and undershoot will be reduced with more capacitance, but the recovery time will be longer.

TABLE 9. BUCK OUTPUT CAPACITOR RECOMMENDATION

CAPACITOR	SIZE	VENDOR	PART NUMBER
10µF/6.3V	0805	TDK	C2012X5R0J106M
10µF/6.3V	0805	Murata	GRM21BR60J106K
22µF/6.3V	1210	TDK	C3216X5R0J226M
100µF/6.3V	1206	Murata	GRM31CR60J107M

PI Loop Compensation (Buck Converter)

The buck converter of ISL97652 can be compensated by a RC network connected from VCB pin to ground. C_{CB} = 4.7nF and R_{CB} = 10k RC network is used in the demo board. The larger value resistor can lower the transient overshoot, however, at the expense of stability of the loop.

The stability can be optimized in a similar manner to that described in the section on "PI Loop Compensation (Boost Converter)".

Bootstrap Capacitor (C_B)

This capacitor is used to provide the supply to the high driver circuitry for the buck MOSFET. The bootstrap supply is formed by an internal diode and capacitor combination. A 470nF is recommended for ISL97652. A low value capacitor can lead to overcharging and in turn damage the part.

If the load is too light, the on-time of the low side diode may be insufficient to replenish the bootstrap capacitor voltage. In this case, if V_{IN}-V_{BUCK} <1.5V, the internal MOSFET pull-up device may be unable to turn-on until V_{LOGIC} falls. Hence, there is a minimum load requirement in this case. The minimum load can be adjusted by the feedback resistors to FBB.

Regulated Charge Pump Controllers (V_{ON} and V_{OFF})

The ISL97652 includes 2 independent charge pumps (see charge pump block and connection diagram). The negative charge pump inverters the V_{SUP} voltage and provides a regulated negative output voltage. The positive charge pump doubles or triples the V_{SUP} voltage and provided a regulated positive output voltage. The regulation of both the negative and positive charge pumps is generated by internal comparator that senses the output voltage and compares it with the internal reference.

The pumps use pulse width modulation to adjust the pump period, depending on the load present. The pumps can provide 30mA for V_{OFF} and 20mA for V_{ON}.

Positive Charge Pump Design Consideration

The positive charge pump can drive multiple stages for 2X/3X step up ratios, or higher. Internal switches (M1 and M2) drive external steering diodes via the pump capacitor CP. Figure 18A shows 2X configuration and Figure 18B shows 3X configuration. The output voltage is divided by feedback resistors R7 and R8, which is then compared to the internal reference via comparator A1. The maximum V_{ON} charge pump current can be estimated from the following equations assuming a 50% switching duty:

$$I_{MAX}(2x) \sim \text{min of 50mA or}$$

$$\frac{2 \bullet V_{SUP} - 2 \bullet V_{DIODE}(2 \bullet I_{MAX}) - V(V_{ON})}{(2 \bullet (R_{ONH} + R_{ONL}))} \bullet 0.95A \quad \text{(EQ. 14)}$$

$$I_{MAX}(3x) \sim \text{min of 50mA or}$$

$$\frac{3 \bullet V_{SUP} - 4 \bullet V_{DIODE}(2 \bullet I_{MAX}) - V(V_{ON})}{4 \bullet (R_{ONH} + R_{ONL})} \bullet 0.95A$$

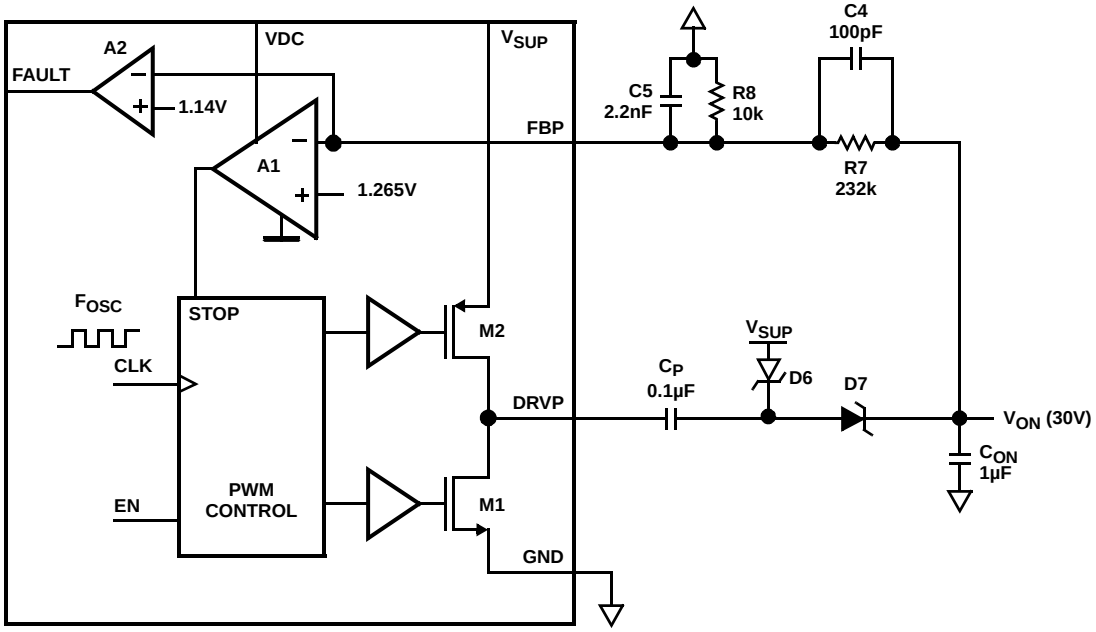


FIGURE 18A. V_{ON} FUNCTION DIAGRAM (VOLTAGE DOUBLER)

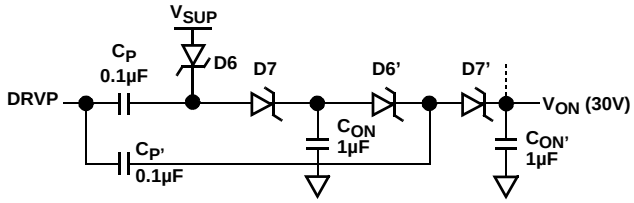


FIGURE 18B. VOLTAGE TRIPLER

FIGURE 18.

In voltage doubler configuration, the maximum V_{ON} is as given by the following equation:

$$V_{ON\_MAX(2x)} = 2 \bullet (V_{SUP} - V_{DIODE}) - 2 \bullet I_{OUT} \bullet (R_{ONH} + R_{ONL}) \quad \text{(EQ. 15)}$$

For Voltage Tripler using additional external diodes and capacitors (Figure 18B):

$$V_{ON\_MAX(3x)} = 3 \bullet V_{SUP} - 4 \bullet V_{DIODE} - 2 \bullet I_{OUT} \bullet (R_{ONH} + R_{ONL}) \quad \text{(EQ. 16)}$$

V_{ON} output voltage is determined by the following equation:

$$V_{ON} = V_{FBP} \times \left(1 + \frac{R7}{R8}\right) \quad \text{(EQ. 17)}$$

Negative Charge Pump Design Consideration

The negative charge pump consists of an internal switcher M1, M2 which drives external steering diodes Dx and Dx via a pump capacitor (CN) to generate the negative V_{OFF} supply. An internal comparator (A1) senses the feedback voltage on FBN and turns on M1 for a period up to half a CLK period to maintain $V_{(FBN)}$ in regulated operation at 0.5V. External feedback resistor R5 is referenced to V_{REF}.

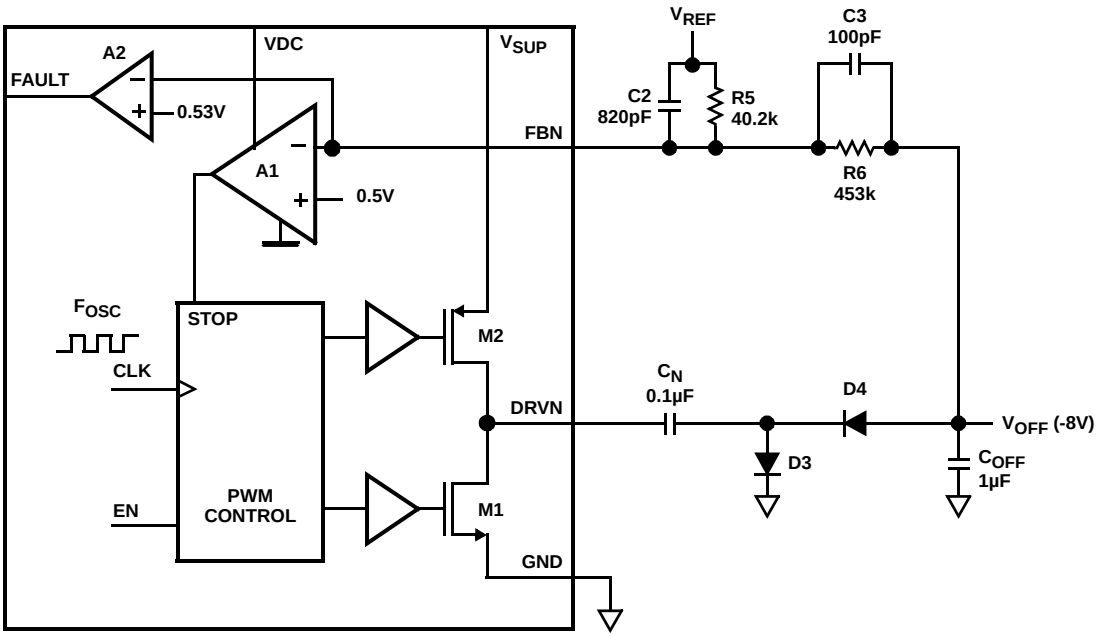


FIGURE 19. NEGATIVE CHARGE PUMP BLOCK DIAGRAM

The maximum V_{OFF} output voltage of a single stage charge pump is:

$$V_{OFF\_MAX}(2x) = -V_{SUP} + V_{DIODE} + 2 \bullet I_{OUT} \bullet (R_{ON}(NOUT)H + R_{ON}(NOUT)L) \quad \text{(EQ. 18)}$$

R5 and R6 in the Typical Application Diagram determine V_{OFF} output voltage.

$$V_{OFF} = V_{FBN} \bullet \left(1 + \frac{R6}{R5}\right) - V_{REF} \bullet \left(\frac{R6}{R5}\right) \quad \text{(EQ. 19)}$$

Charge Pump Supply

The magnitude of the SUP supply will determine the charge pump diode configuration; whether x2 or x3 for the positive charge pump or x1 or x2 for the negative charge pump.

An independent charge pump supply pin 13 (SUP) is provided and this may be connected to Vin, Vmain, AVDD or some other suitable supply.

Note that if AVDD is chosen for the SUP supply, then a potential fault-like interaction with the supply sequencing and fault checking is present; when EN1 goes high (with EN2 low), fault checking on the VOFF charge pump is started by the voltage ramp on DEL1. If this pin reaches ~1.9V before VOFF is within 90% of it's regulation voltage then the buck converter (Tcon bias) and Voff will be continually re-started. This condition will arise if the SUP supply has not been activated by EN2 going high before DEL1 has reached 1.9V. One solution would be to increase the capacitance on DEL1 to overlap enough in time with the EN2 going high. This does have the disadvantage of lengthening the fault detection time of the VOFF charge pump under true fault conditions and it also lengthens the initial VOFF turn-on time. Another solution would be to supply SUP from Vmain as long as the magnitude of Vmain (without the boost running) is large enough to satisfy the regulated VOFF supply.

Improving Charge Pump Noise Immunity

Depending on PCB layout and environment, noise pick-up at the FBP and FBN inputs, which may degrade load regulation performance, can be reduced by the inclusion of capacitors across the feedback resistors (e.g. in the Application Diagram, C4 and C5 for the positive charge pump).
Set R7 • C4 = R8 • C5 with C4 ~ 100pF.

$V_{ON-SLICE}$ Circuit Operation

The Von slice circuit functions as a three way multiplexer, switching VGHM between ground, VGL and VGH (typ 15-30V). Voltage selection is provided by digital inputs VDPM (enable) and VFLK (control). HIGH to LOW delay and slew control is provided by external components on pins CE and RE respectively. The block diagram of the VON-SLICE circuit is shown in Figure 3.

When VDPM is LOW, the block is disabled and VGHM is grounded.

When VDPM is HIGH, VGHM is determined by VFLK; when VFLK goes LOW, there is a delay controlled by the capacitor attached to the CE pin, following which VGHM is driven to VGL, with a slew rate controlled by the resistor attached to the RE pin. Note that VGL is used only as a reference voltage for an amplifier, thus does not have to source or sink a significant DC current. When VFLK goes HIGH, VGHM is

driven HIGH at a rate primarily controlled by the P1 switch resistance (RONVGH) and the external capacitive load.

VGHM HIGH to LOW transitions are more complex; take the case where the block is already enabled (VDPM is HIGH). When VFLK is HIGH, pin CE is grounded. On the falling edge of VFLK, a current is passed into pin CE to charge an external capacitor to VREF. This creates a delay, equal to CE*21300. For example, the delay time is ~10µs for 470pF CE capacitor. At this point, VGHM begins to slew down from VGH to VGL. The slew current is equal to Isl=300/(RE+5kΩ), and the dv/dt slew rate is Isl/Cload.

where Cload is the load capacitance applied to VGHM.

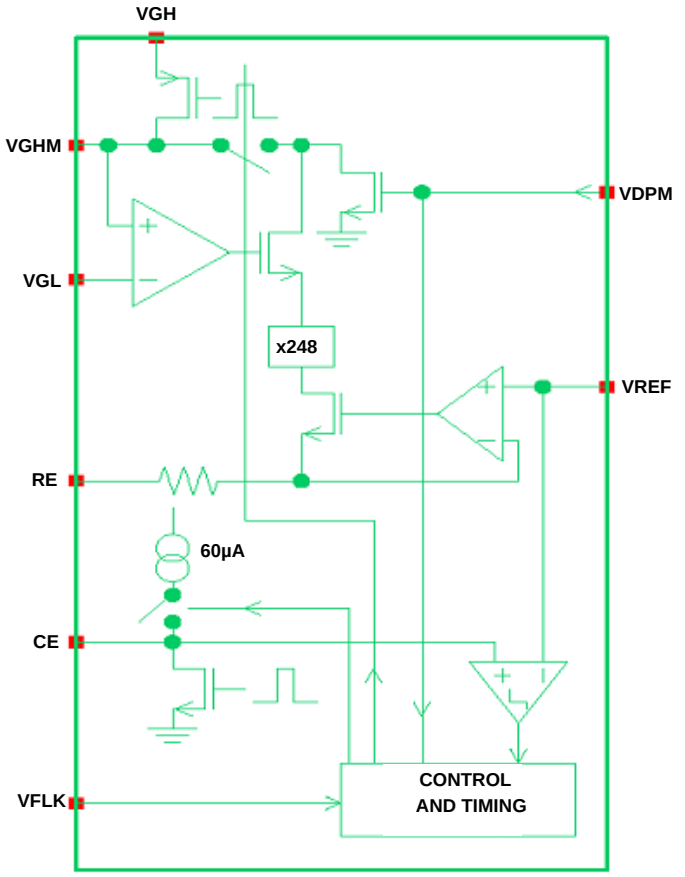


FIGURE 20. VON-SLICE BLOCK DIAGRAM

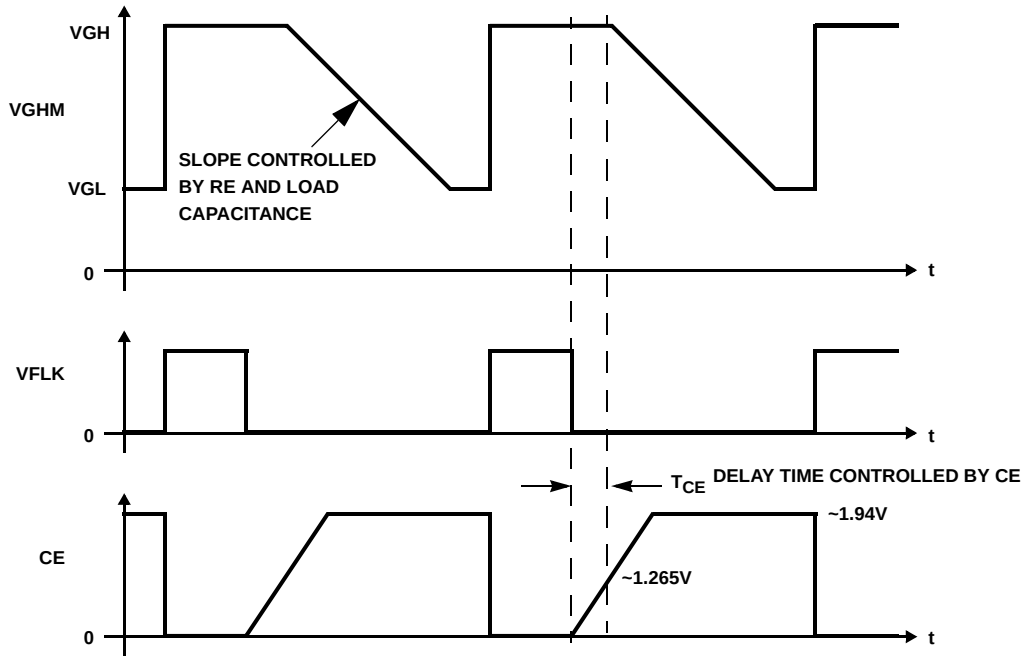


FIGURE 21. VON-SLICE TIMING WAVEFORM

High Performance V_{COM} Amplifiers

The integrated high performance amplifiers are designed to drive the V_{COM} plane in TFT-LCD displays. Under normal operational conditions, the amplifiers are permanently enabled when the AVIN supply is present. Under fault conditions and with EN1 active, the temperature shut-down (T_{OFF} exceeded) will disable the amplifiers until the temperature drops to T_{ON}. Temperature shut-down of the amplifiers is disabled if EN1 is disabled.

The amplifiers integrated in to the ISL97652 feature high output current of 50mA minimum and high slew rate of 50V/µs. Both inputs and outputs have rail-to-rail capability.

Start-Up Sequence Control

The ISL97652 features extensive start-up sequence control options. Two enable pins and two delay control pins are used to set the start-up sequence.

The EN1 enable pin controls the buck regulator and negative charge pump controller. When EN1 goes H, the internal 5.3V regulator starts up. Once the regulator output on pin 27 (VDC) exceeds it's UVLO threshold, the REF pin starts to charge up to the normal output level. Once REF is within 15% of it's final value, the buck regulator will start to operate. Note that if V_{REF} moves more than 15% from it's target value, all major functions will be disabled until REF returns to it's normal range. This involves the chip going through the normal start-up sequence from buck start-up onwards, depending on the state of the enable signals EN1, EN2. The soft-start time is set using the capacitor connected to SSB. Once the output reaches 90% the DLY1 capacitor begins to charge. Once the threshold is reached, the negative charge pump will begin. Removing the DLY1 capacitor will cause the negative charge pump to start immediately once the buck regulator reaches 90% of the target value. The delay time and soft-start times are determined using the following equations:

$$T_{DLY1} = C_{DL1} \times \frac{V_{DL1}}{I_{DL1}} \quad \text{(EQ. 20)}$$

$$T_{SSB} = C_{SSB} \times \frac{V_{SSB}}{I_{SSB}} \quad \text{(EQ. 21)}$$

The EN2 pin is used to control the boost and positive charge pump circuits.Note that EN2 is ignored until the buck converter has reached 90% of it's target value. When taken high, the internal PFET is turned on to connect the input to the A_{VDD} output. A capacitor connected to SUI provides control over the soft connect to limit inrush current. Next, the boost converter starts to operate. The soft-start time for the boost is set using the capacitor tied to the SS pin. Once the output reaches 90% of the target value, the DLY2 timer starts. Once completed, the positive V_{ON} charge pump starts to operate. If CDL2 is not present, the V_{ON} charge pump will start immediately once the boost is in regulation. The delay time is determined using the following equation:

$$T_{DLY2} = C_{DL2} \times \frac{V_{DL2}}{I_{DL2}} \quad \text{(EQ. 22)}$$

$$T_{SS} = C_{SS} \times \frac{V_{SS}}{I_{SS}} \quad \text{(EQ. 23)}$$

Variations on the start-up sequence can be seen in Figures 22, 23 and 24.

The Gate pulse modulator is enabled when both of the following conditions are met:

- VDPM is H
- V_{ON} is over 90% of it's target value.

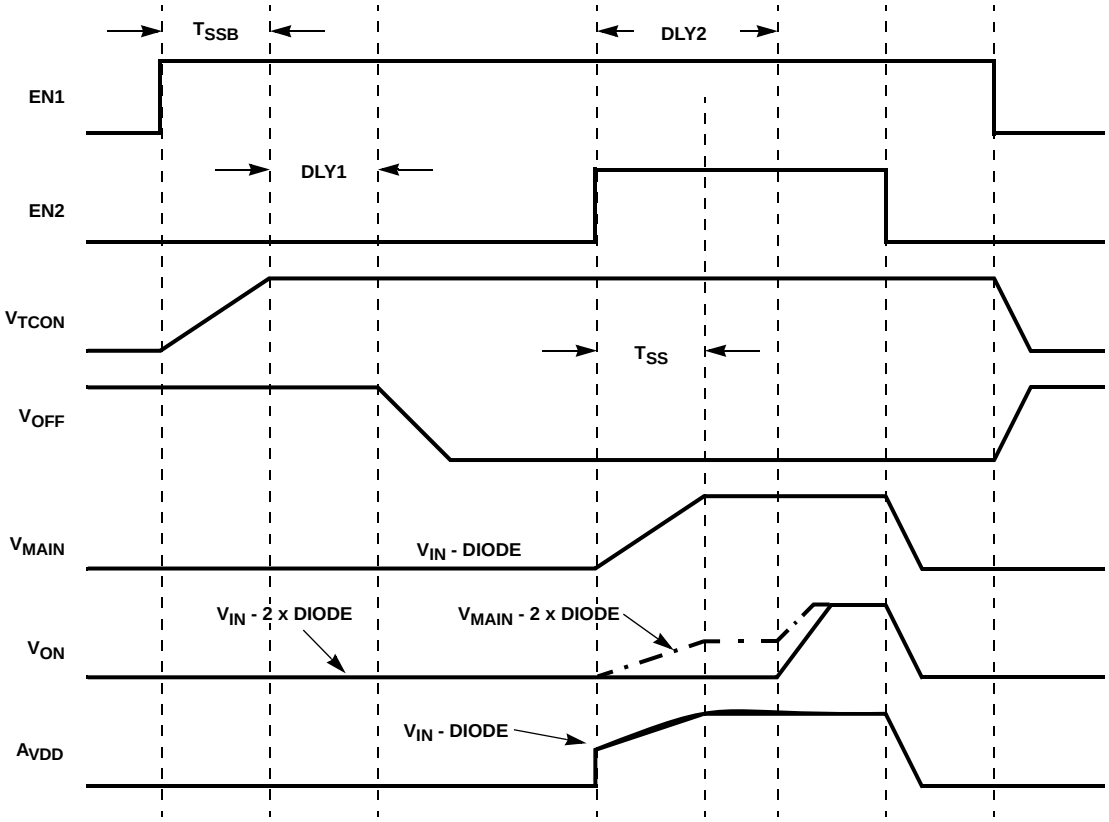


FIGURE 22. TIMING DIAGRAM 1

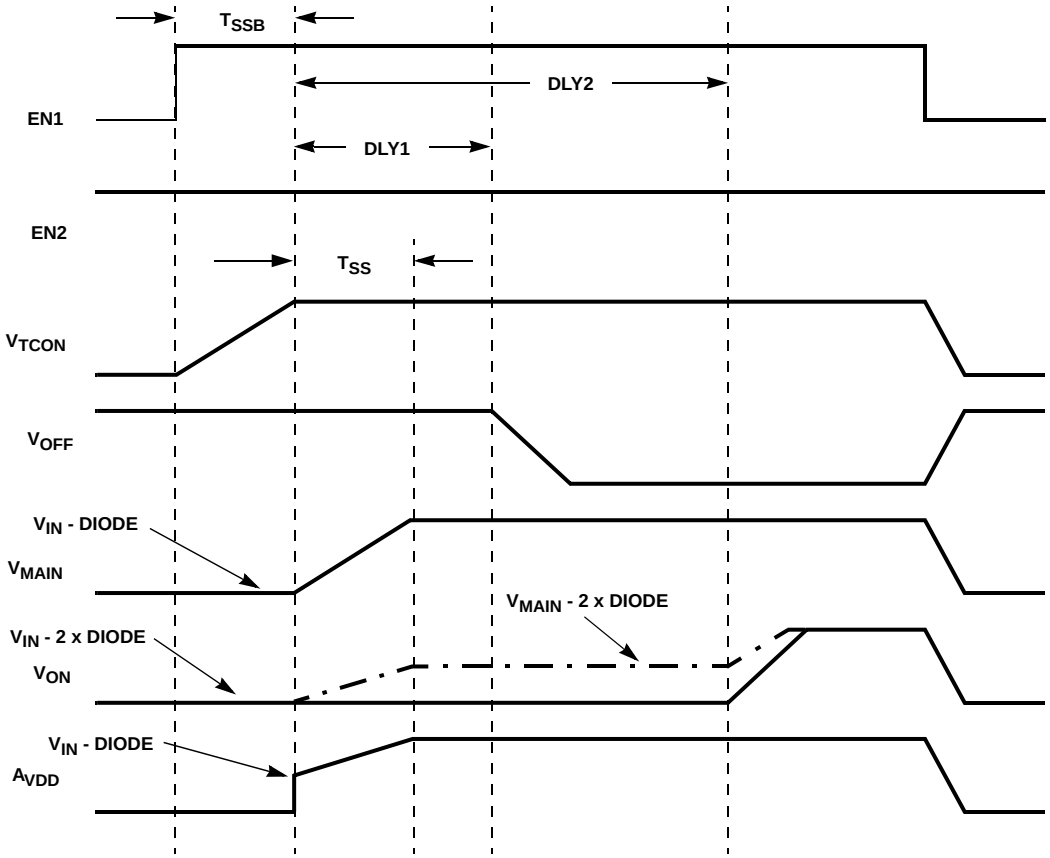


FIGURE 23. TIMING DIAGRAM 2

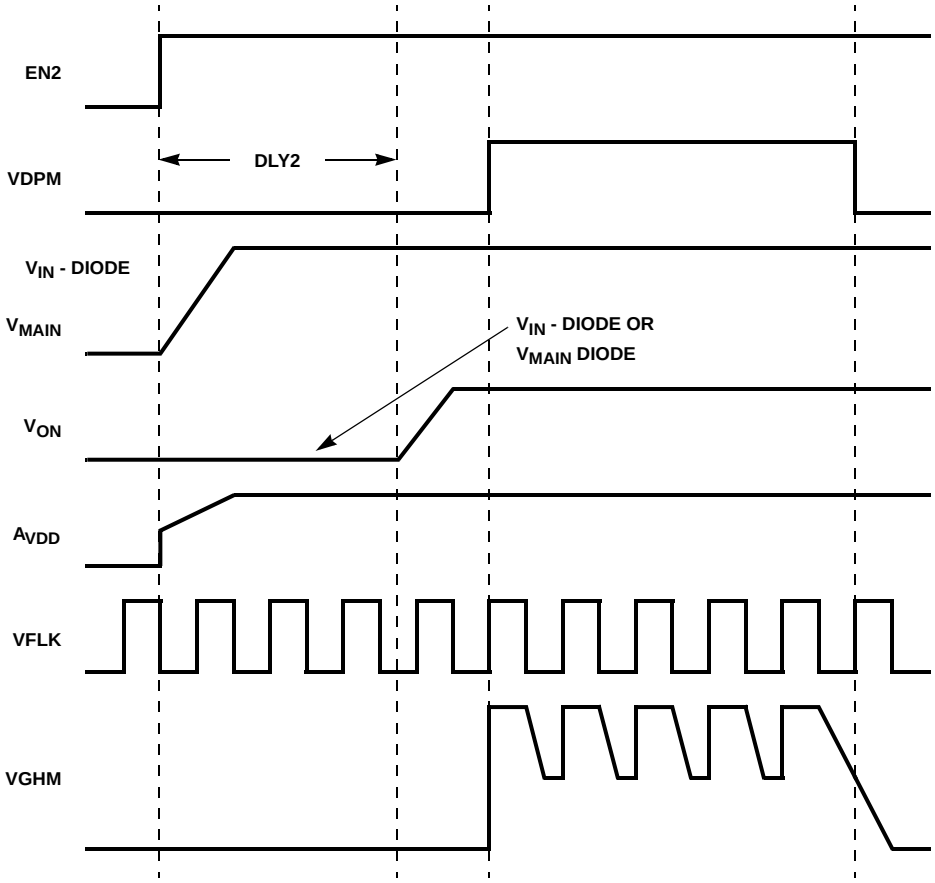


FIGURE 24. TIMING DIAGRAM 3

Switching Frequency Control

The ISL97652 can operate at either 650kHz or 1.3MHz depending on the state of the FREQ pin. When connected to GND, 650kHz is selected. When connected to V_{IN}, 1.3MHz is selected. Higher frequencies enable the selection of smaller inductors and capacitors. Lower frequencies allow closer input/output ratios to be supported. The charge pump circuits switch at half the frequency selected.

Undervoltage Lockout

The integrated undervoltage lockout circuit is designed to power down the TFT-LCD if the input voltage falls below a preset threshold. The ISL97652 will not start if the input voltage is below the UVLO threshold.

Over-Temperature Protection

An internal temperature sensor continuously monitors the die temperature. In the event that the die temperature exceeds the thermal trip point of +150°C, the device will shut down. Operation with die temperatures between +125°C and 150°C can be tolerated for short periods of time, however, in order to maximize the operating life of the IC, it is recommended that the effective continuous operating junction temperature of the die should not exceed +125°C.

Fault Detection

The ISL97652 includes extensive fault handling circuitry, which interacts with the start-up sequence circuitry if a fault is detected.

During normal operation, if EN1 goes L, all major functions are disabled immediately, including the 5V regulator. If EN2 goes L, but EN1 remains H, boost, V_{ON} and GPM are disabled immediately. When EN1 and/or EN2 return H, the start-up sequence restarts from the appropriate point.

If the over-temperature threshold (+150°C nominal) is exceeded, or if V_{IN} drops below the specified lower UVLO limit, all major functions are disabled immediately, excluding the 5.3V regulator. If/when the temperature drops below +100°C, or V_{IN} returns to a level above the upper UVLO threshold the start-up sequence will re-commence by enabling REF.

Timed “Faults”

The four ramp voltages, SSB, SS, DEL1 and DEL2 all ramp linearly from 0V to approximately 2.7V, where they are soft-clamped. The 2V thresholds of each are used to enable timed fault checking on related blocks. Therefore, external capacitor values should be chosen such that all major

outputs are in regulation by the time this threshold is reached. For example, SSB controls step-down regulator fault checking, DEL1 controls V_{OFF} fault checking, SS controls step-up regulator and PFET fault checking, DEL2 controls V_{ON} and GPM fault checking. If a fault on any of the major blocks is detected continuously for a predetermined time interval (currently set to 63µs), when fault checking is enabled for that function, the fault latch will be set. This causes all major functions to be disabled immediately, including the 5.3V regulator. Once VDC falls below its internal UVLO limit (typically 3.6V), the FAULT latch is reset. This will initiate an automatic restart. If the fault has been cleared, the restart will be successful; if the fault persists, the FAULT latch will again be set, and the cycle will repeat itself.

Buck, boost and V_{ON} circuits have fault thresholds at 90% of target values.

The V_{OFF} fault threshold is set at 125mV above the 0.5V regulation point.

GPM fault detection is designed to detect a short circuit on the output, by monitoring whether VGHM fails to pull up to VGH on two consecutive F_{OSC} clock periods.

The A_{VDD} PFET also has fault checking, which will protect the FET in the event of an output short circuit.

Note that the V_{COM} amplifiers are independently biased, and are enabled at all times, except if an over-temperature fault is detected. If this behavior is not desired, then there is an option to power the V_{COM} amplifiers from A_{VDD}, which will keep them disabled until the boost is enabled.

Note also that it is possible to prevent timed fault checking on any or all of the major functions, simply by externally clamping SSB, SS, DEL1 and/or DEL2 to a voltage between 1.3V and 2V.

PCB Layout Procedure

To ensure the user gets the best chip performance with minimum amount of PCB rework in the development phase, the following PCB layout procedure is strongly recommended.

PCB metal layers

Reserve the top PCB metal layer for direct power ground (PGND) connections to the supply pins and switching outputs (buck/boost/charge-pumps). The goal is to ensure there are no VIAS in the boost and buck paths to the smoothing capacitors. The top layer may also be used for general routing of non-sensitive tracks as long as this does not compromise the supply track widths which should be as wide as possible.

Note that using VIAs in series with smoothing capacitors (even if implemented as multiply parallel VIAs) increases the effective high frequency ESR of the capacitors and WILL cause degraded system operation.

(Route the following tracks on the PGND (top) metal layer: PGND1,2,3 [a single wide track] to CIN, Cout and CB, D5. SW1,2 [a single wide track] to L1/D1, SWB1,2 [a single wide track] to L2/D5.)

Reserve the bottom (or an intermediate layer) for the signal ground plane (SGND) and signal routing. It is recommended that all feedback inputs and any other sensitive tracks are routed to the SGND layer using a VIAs as close to the chip as possible. This prevents unwanted interference pick-up and allows the supply smoothing capacitors to be places as close to the chip as possible.

(Route the following tracks on the SGND (bottom or intermediate) metal layer: FB, FBB, FBP, FBN, POS1,2,)

Star Ground

A star ground system is where a number of different grounds (e.g. PGND, SGND°¦) come together at a single location which then becomes the reference ground point for the system as a whole. Star grounding ensures minimum interference between different functions in a system.

Practically, it is difficult to achieve an ideal (single location) ground point due to the physical dimensions of the chip, smoothing capacitors and track routing, however, the exposed die plate and the area immediately next to the PGND1,2,3 pins is defined as the star ground for this chip.

The negative smoothing capacitor terminals of: Cout, CB and CIN must be located as close as possible to the PGND1,2,3 pins. The smoothing capacitors for VIN, Cout and CB come as a block of three or four capacitors with (usually) one small capacitor whose role is to reduce the total effective ESR of the capacitors. It is recommended that the small capacitor and at least one of the large capacitors from each capacitor block is placed as physically close to the chip PGND pins as possible. The other capacitors from each block can be placed a little further away, if necessary.

Exposed Die plate connection

The exposed die plate connection to the underside of the chip must directly connect the PGNDs (pins 34,35,36) and AGND (pin 15) with an equivalent area of metal. The other ground pins (amplifier OGND and charge pump GND pins may also be connected to the die plate.

The exposed die plate connection must have multiple VIAs (use a 4x4 array) connecting the top metal PGND layer to the bottom SGND metal layer. The bottom SGND metal area around the VIA array should be maximized in order to keep the thermal resistance of the chip and PCB system as low as possible. This will optimise operation at high currents or in high ambient temperature applications.

Order of component placement

The order of component placement should be as follows. This procedure minimizes the high current PGND and supply track impedance to the chip pins.

1). Cout, Cin, CB ®C get these components as close to PGND1,2,3 as possible and use wide tracks on the top PGND layer with no VIAs.

2). L1, D1, L2, D5 ®C get these components as close to the chip pins as possible having observed 1/ and use wide tracks on the top PGND layer with no VIAs.

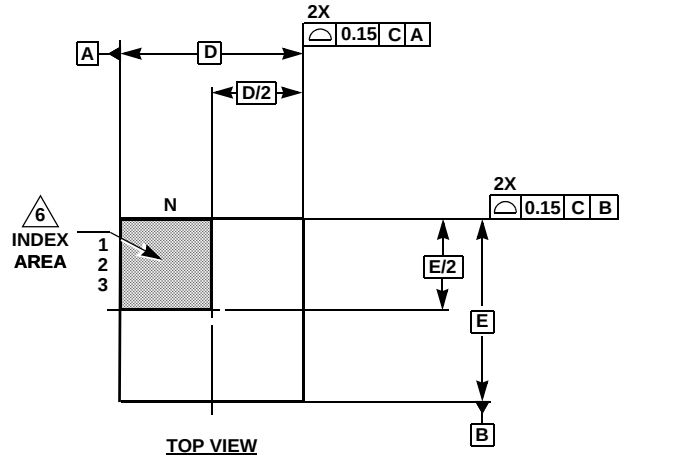
3). Feedback resistor networks connected to FB, FBB, FBP, FBN, POS1,2 - keep tracks as short as possible, having first observed 1/ and 2/. Routing on the SGND layer should be used. Avoid routing this tracks under switching tracks on the top surface.

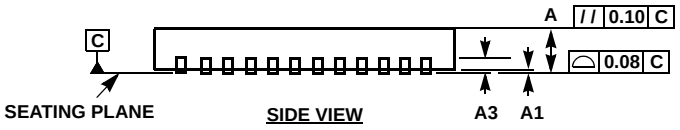
4). All other components - keep all switching output tracks (SW1,2, SWB1,2, CBOOT, DRVP, DRVN, VGHM, VFLK) on the PGND layer shielded from adjacent tracks.

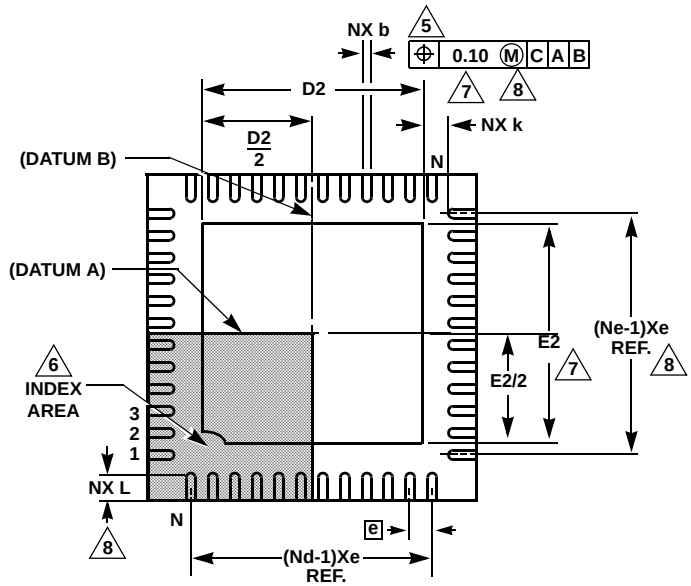
Evaluation PCB

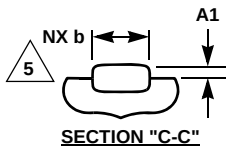
A two layer evaluation PCB is available which follows the above procedure and may be useful as a reference to guide the PCB layout engineer. For example, the smoothing capacitor positive rail to PVin does contain VIAs in series ®C however, a small capacitor has been used directly at the PVin pins which overcomes the ESR objection.

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)









L48.7x7

48 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VKKD-2 ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A3		0.20 REF		-
b	0.18	0.23	0.30	5, 8
D		7.00 BSC		-
D2	4.15	4.30	4.45	7, 8
E		7.00 BSC		-
E2	4.15	4.30	4.45	7, 8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.30	0.40	0.50	8
N		48		2
Nd		12		3
Ne		12		3

Rev. 2 5/06

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.