

March 1997

### Features

- Performs Memory Address Latch and Decoder Functions Multiplexed or Non-Multiplexed
- Interfaces Directly with the CDP1800-Series Microprocessors
- Allows Decoding for Systems Up to 32K Bytes

### Ordering Information

5V	10V	TEMP. RANGE	PACKAGE	PKG. NO.
CDP1883CE	CDP1883E	-40°C to +85°C	PDIP	E20.3

### Description

The CDP1883 is a CMOS 7-bit memory latch and decoder circuit intended for use in CDP1800-series microprocessor systems. It can serve as a direct interface between the multiplexed address bus of this system and up to four 8K x 8-bit memories to implement a 32K-byte memory system. With four 4K x 8-bit memories, a 16K-byte system can be decoded.

The device is also compatible with non-multiplexed address bus microprocessors. By connecting the clock input to  $V_{DD}$ , the latches are in the data-following mode and the decoded outputs can be used in general-purpose memory-system applications.

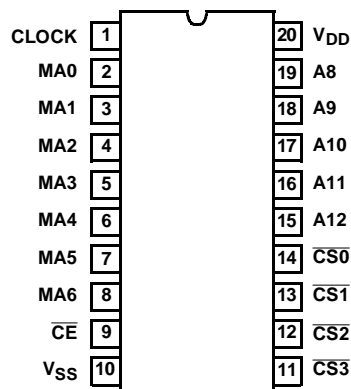
The CDP1833 is compatible with CDP1800-series microprocessors operating at maximum clock frequency.

The CDP1883 and CDP1883C are functionally identical. They differ in that the CDP1883 has a recommended operating voltage range of 4V to 10.5V and the C version has a recommended operating voltage range of 4V to 6.5V.

The CDP1883 and CDP1883C are supplied in 20 lead dual-in-line plastic packages (E Suffix).

### Pinout

CDP1883, CDP1883C  
(PDIP)  
TOP VIEW



# CDP1883, CDP1883C

## Absolute Maximum Ratings

DC Supply Voltage Range, ( $V_{DD}$ )  
 (All Voltages Referenced to  $V_{SS}$  Terminal)  
 CDP1883 . . . . . -0.5V to +11V  
 CDP1883C . . . . . -0.5V to +7V  
 Input Voltage Range, All Inputs . . . . . -0.5V to  $V_{DD}$  +0.5V  
 DC Input Current, Any One Input . . . . .  $\pm 10$ mA

## Thermal Information

Thermal Resistance (Typical)  $\theta_{JA}$  ( $^{\circ}\text{C}/\text{W}$ )  
 PDIP Package . . . . . 80  
 Device Dissipation Per Output Transistor  
 $T_A$  = Full Package Temperature Range . . . . . 100mW  
 Operating Temperature Range ( $T_A$ )  
 Package Type E . . . . . -40 $^{\circ}\text{C}$  to +85 $^{\circ}\text{C}$   
 Storage Temperature Range ( $T_{STG}$ ) . . . . . -65 $^{\circ}\text{C}$  to +150 $^{\circ}\text{C}$   
 Lead Temperature (During Soldering)  
 At distance 1/16"  $\pm$  1/32 In. (1.59  $\pm$  0.79mm)  
 from case for 10s max. . . . . +265 $^{\circ}\text{C}$

*CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.*

## Recommended Operating Conditions

At  $T_A$  = Full Package Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

PARAMETER	SYMBOL	CDP1883		CDP1883C		UNITS
		MIN	MAX	MIN	MAX	
DC Operating Voltage Range		4	10.5	4	6.5	V
Input Voltage Range		$V_{SS}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	V

## Static Electrical Specifications

At  $T_A$  = -40 $^{\circ}\text{C}$  to +85 $^{\circ}\text{C}$ ,  $V_{DD} \pm 5\%$ , Except as Noted:

PARAMETER	SYMBOL	CONDITIONS			CDP1883			CDP1883C			UNITS
		$V_O$ (V)	$V_{IN}$ (V)	$V_{DD}$ (V)	MIN	(NOTE 1) TYP	MAX	MIN	(NOTE 1) TYP	MAX	
Quiescent Device Current	$I_{DD}$	-	0, 5	5	-	1	10	-	5	50	$\mu\text{A}$
		-	0, 10	10	-	10	100	-	-	-	$\mu\text{A}$
Output Low Drive (Sink) Current	$I_{OL}$	0.4	0, 5	5	1.6	3.2	-	1.6	3.2	-	mA
		0.5	0, 10	10	3.2	6.4	-	-	-	-	mA
Output High Drive (Source) Current	$I_{OH}$	4.6	0, 5	5	-1.15	-2.3	-	-1.15	-2.3	-	mA
		9.5	0, 10	10	-2.3	-4.6	-	-	-	-	mA
Output Voltage Low-Level (Note 2)	$V_{OL}$	-	0, 5	5	-	0	0.1	-	0	0.1	V
		-	0, 10	10	-	0	0.1	-	-	-	V
Output Voltage High-Level (Note 2)	$V_{OH}$	-	0, 5	5	4.9	5	-	4.9	5	-	V
		-	0, 10	10	9.9	10	-	-	-	-	V
Input Low Voltage	$V_{IL}$	0.5, 4.5	-	5	-	-	1.5	-	-	1.5	V
		0.5, 9.5	-	10	-	-	3	-	-	-	V
Input High Voltage	$V_{IH}$	0.5, 4.5	-	5	3.5	-	-	3.5	-	-	V
		0.5, 9.5	-	10	7	-	-	-	-	-	V
Input Leakage Current	$I_{IN}$	Any Input	0, 5	5	-	-	$\pm 1$	-	-	$\pm 1$	$\mu\text{A}$
			0, 10	10	-	-	$\pm 2$	-	-	-	$\mu\text{A}$
Operating Current (Note 3)	$I_{DD1}$	0, 5	0, 5	5	-	-	2	-	-	2	mA
		0, 10	0, 10	10	-	-	4	-	-	-	mA

## CDP1883, CDP1883C

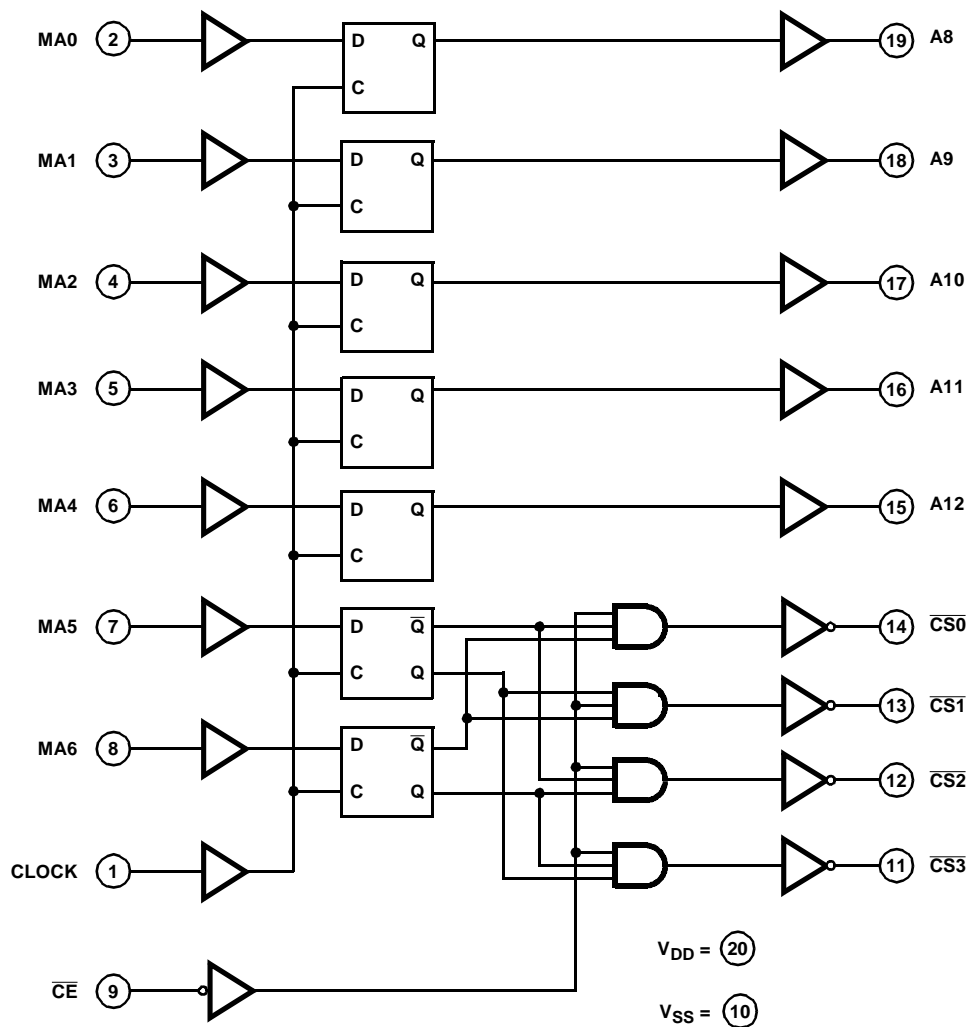
**Static Electrical Specifications** At  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{DD} \pm 5\%$ , Except as Noted: **(Continued)**

PARAMETER	SYMBOL	CONDITIONS			CDP1883			CDP1883C			UNITS
		$V_O$ (V)	$V_{IN}$ (V)	$V_{DD}$ (V)	MIN	(NOTE 1) TYP	MAX	MIN	(NOTE 1) TYP	MAX	
Minimum Data Retention Voltage	$V_{DR}$	$V_{DD} = V_{DR}$			-	2	2.4	-	2	2.4	V
Data Retention Current	$I_{DR}$	$V_{DD} = 2.4\text{V}$			-	0.01	1	-	0.5	5	$\mu\text{A}$
Input Capacitance	$C_{IN}$	-	-	-	-	5	7.5	-	5	7.5	pF
Output Capacitance	$C_{OUT}$	-	-	-	-	10	15	-	10	15	pF

**NOTES:**

1. Typical values are for  $T_A = +25^{\circ}\text{C}$ .
2.  $I_{OL} = I_{OH} = \mu\text{A}$
3. Operating current measured at 200kHz for  $V_{DD} = 5\text{V}$  and 400kHz for  $V_{DD} = 10\text{V}$ , with outputs open circuit.

### Functional Diagram



### Signal Descriptions/Pin Functions

**CLOCK:** Latch Input Control - a high on the clock input will allow data to pass through the latch to the output pin. Data is latched on the high-to-low transition of the clock input. This pin is connected to TPA in CDP1800-series systems and tied to  $V_{DD}$  for other applications.

**MA0 - MA4:** Address inputs to the high-byte address latches.

**MA5 - MA6:** High byte address inputs decoded to produce chip selects  $\overline{CS0}$  -  $\overline{CS3}$ .

**$\overline{CE}$ :** CHIP ENABLE input - A low on this pin will enable the chip select decoder. A high on this pin forces  $\overline{CS0}$ ,  $\overline{CS1}$ ,  $\overline{CS2}$ , and  $\overline{CS3}$  outputs to a high (false) state.

**A8 - A12:** Latched high-byte address outputs.

**$\overline{CS0}$  -  $\overline{CS3}$ :** One of four latched and decoded Chip Select outputs.

**$V_{DD}$ ,  $V_{SS}$ :** Power and ground pins, respectively.

TRUTH TABLE

INPUTS				OUTPUTS			
$\overline{CE}$	CLK	MA5	MA6	$\overline{CS0}$	$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$
0	1	0	0	0	1	1	1
0	1	1	0	1	0	1	1
0	1	0	1	1	1	0	1
0	1	1	1	1	1	1	0
0	0	X	X	Previous State			
1	X	X	X	1	1	1	1

TRUTH TABLE

INPUTS			OUTPUTS
$\overline{CE}$	CLK	MA0 - 4	A8 - A12
X	1	1	1
X	1	0	0
X	0	X	Previous State

X = Don't Care

### Application Information

The CDP1883 and CDP1883C can be interfaced, without external components, with CDP1800-series microprocessor systems. These microprocessors feature a multiplexed address bus and provide an address latch signal (TPA) that is used as the clock input of the CDP1883. See Figure 2 and Figure 3.

This signal is used to latch 7 bits of the high-order address. The lower five high-order address inputs are latched and held to be used with the eight lower-order address inputs to access an 8K x 8-bit memory. The two upper high-order address inputs are latched and decoded for use as chip selects.

The latched address and decoding functions of the CDP1883 and CDP1883C allow them to operate with 32K-byte memory systems. In addition, smaller memory systems can be configured with 4K x 8-bit or smaller memories, or a mix of memory sizes up to 8K x 8-bit.

## CDP1883, CDP1883C

**Dynamic Electrical Specifications**  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{DD} \pm 5\%$ ,  $t_R, t_F = 20\text{ns}$ ,  $V_{IH} = 0.7 V_{DD}$ ,  $V_{IL} = 0.3 V_{DD}$ ,  $C_L = 100\text{pF}$ .  
See Figure 1

PARAMETER		$V_{DD}$ (V)	CDP1883			CDP1883C			UNITS
			MIN	(NOTE 1) TYP	(NOTE 2) MAX	MIN	(NOTE 1) TYP	(NOTE 2) MAX	
Minimum Setup Time, Memory Address to CLOCK	$t_{MACL}$	5	-	10	35	-	10	35	ns
		10	-	8	25	-	-	-	ns
Minimum Hold Time, Memory Address After CLOCK	$t_{CLMA}$	5	-	8	25	-	8	25	ns
		10	-	8	25	-	-	-	ns
Minimum CLOCK Pulse Width	$t_{CLCL}$	5	-	50	75	-	50	75	ns
		10	-	25	40	-	-	-	ns
PROPAGATION DELAY TIMES									
Chip Enable to Chip Select	$t_{CECS}$	5	-	75	150	-	75	150	ns
		10	-	45	100	-	-	-	ns
CLOCK to Chip Select	$t_{CLCS}$	5	-	100	175	-	100	175	ns
		10	-	65	125	-	-	-	ns
CLOCK to Address	$t_{CLA}$	5	-	100	175	-	100	175	ns
		10	-	65	125	-	-	-	ns
Memory Address to Chip Select	$t_{MACS}$	5	-	100	175	-	100	175	ns
		10	-	75	125	-	-	-	ns
Memory Address to Address	$t_{MAA}$	5	-	80	125	-	80	125	ns
		10	-	40	60	-	-	-	ns

**NOTES:**

1. Typical values are for  $T_A = 25^{\circ}\text{C}$ .
2. Maximum limits of minimum characteristics are the values above which all devices function.

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# CDP1883, CDP1883C

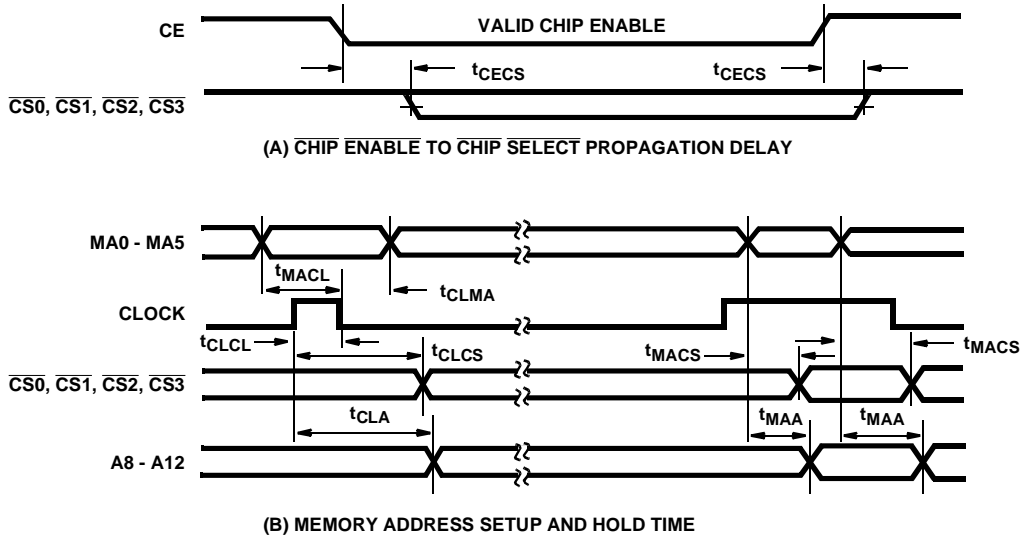


FIGURE 1. CDP1883 TIMING WAVEFORMS

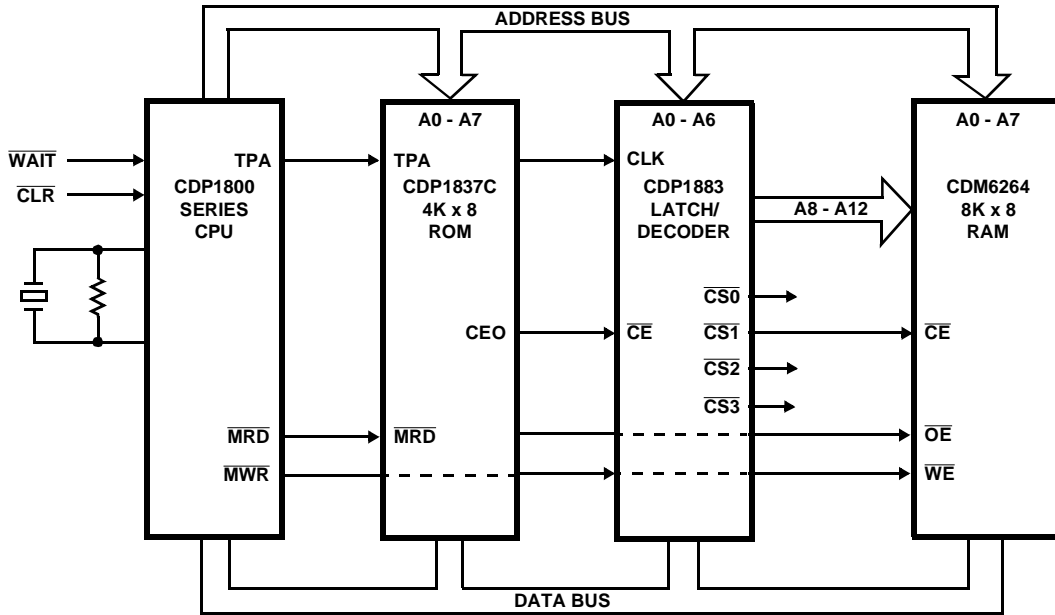


FIGURE 2. MINIMUM CDP1800-SYSTEM USING THE CDP1883 INTERFACE WITH AN 8K X 8-BIT MEMORY

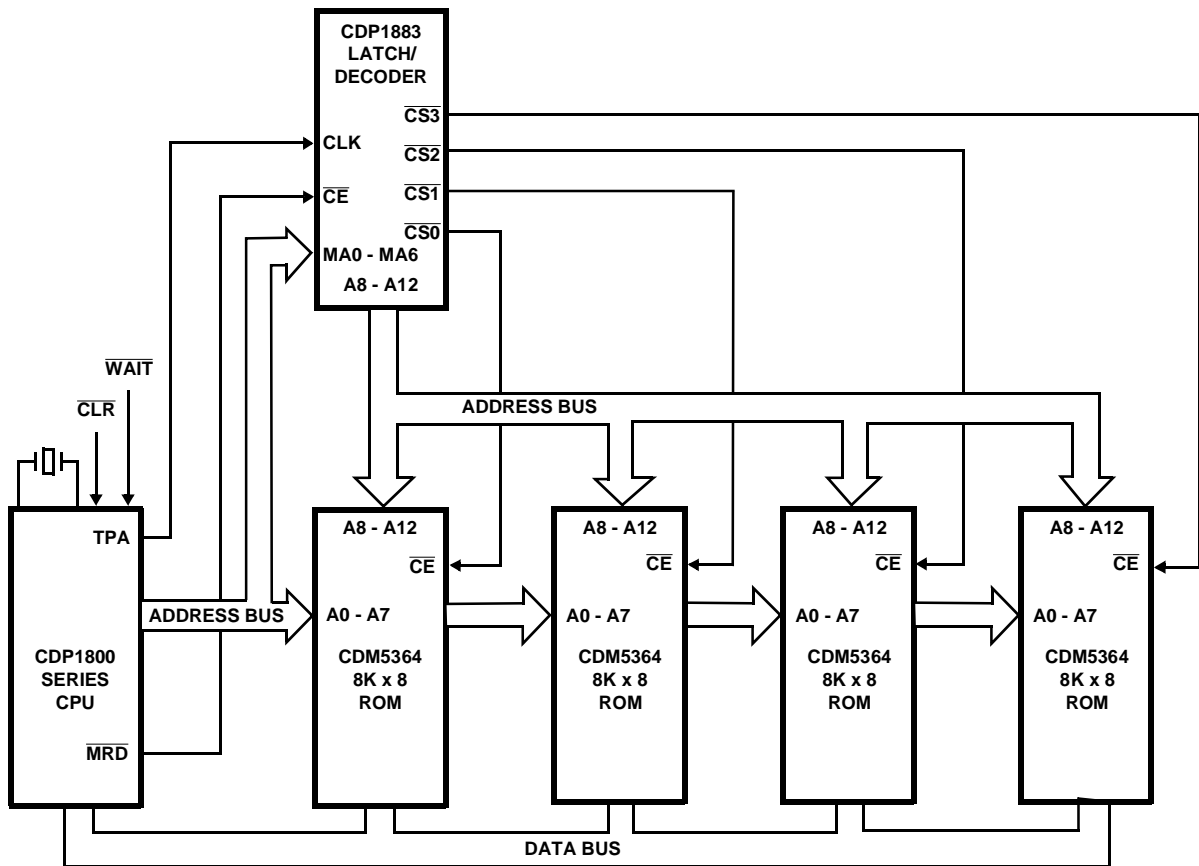


FIGURE 3. 32K-BYTE ROM SYSTEM USING THE CDP1883