

December 1999

**OBSOLETE PRODUCT
FOR A POSSIBLE SUBSTITUTE PRODUCT**
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or email: centapp@intersil.com

Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Block Oriented 24-Bit Sequencer
- Configurable as Two Independent 12-Bit Sequencers
- 24 x 24 Crosspoint Switch
- Programmable Delay on 12 Outputs 9-
- Multi-Chip Synchronization Signals
- Standard μ P Interface
- 100pF Drive on Outputs
- DC to 40MHz Clock Rate

Applications

- 1-D, 2-D Filtering
- Pan/Zoom Addressing

- FFT Processing
- Matrix Math Operations

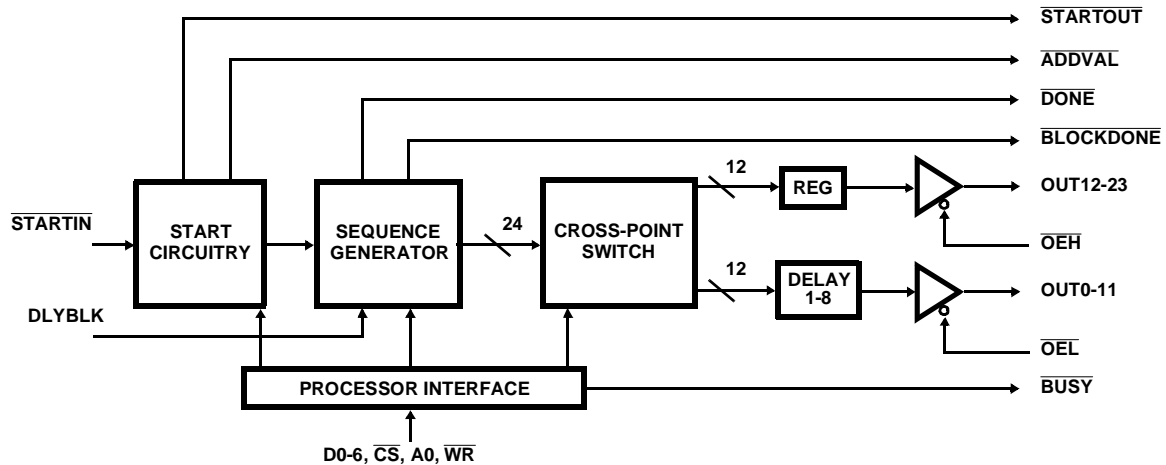
Ordering Information

| PART NUMBER | TEMP. RANGE (°C) | PACKAGE | PKG. NO. |
|-------------------|------------------|-----------|----------|
| HSP45240GM-25/883 | -55 to 125 | 68 Ld PGA | |
| HSP45240GM-33/883 | -55 to 125 | 68 Ld PGA | |
| HSP45240GM-40/883 | -55 to 125 | 68 Ld PGA | |

Description

The Intersil HSP45240/883 is a high speed Address Sequencer which provides specialized addressing for functions like FFTs, 1-D and 2-D filtering, matrix operations, and image manipulation. The sequencer supports block oriented addressing of large data sets up to 24 bits at clock speeds up to 40MHz.

Block Diagram



HSP45240/883

Absolute Maximum Ratings

Supply Voltage +8.0V
 Input, Output Voltage Applied. GND -0.5V to V_{CC} +0.5V
 ESD Classification Class 1

Operating Conditions

Temperature Range -55°C to 125°C
 Voltage Range +4.5V to +5.5V

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W) θ_{JC} (°C/W)
 PGA Package 37.1 10.1
 Maximum Package Power Dissipation at 125°C
 PGA Package 1.35W
 Maximum Junction Temperature. 175°C
 Maximum Storage Temperature Range -65°C to 150°C
 Maximum Lead Temperature (Soldering 10s). 300°C

Die Characteristics

Gate Count 8,388

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

TABLE 1. DC ELECTRICAL SPECIFICATIONS

Device Guaranteed and 100% Tested

| PARAMETER | SYMBOL | TEST CONDITIONS | GROUP A SUB- GROUPS | TEMPERATURE (°C) | LIMITS | | UNITS |
|--------------------------------|------------|---|---------------------------|-------------------------|--------|-----|---------|
| | | | | | MIN | MAX | |
| Logical One Input Voltage | V_{IH} | $V_{DD} = 5.5V$ | 1, 2, 3 | $-55 \leq T_A \leq 125$ | 2.2 | - | V |
| Logical Zero Input Voltage | V_{IL} | $V_{DD} = 4.5V$ | 1, 2, 3 | $-55 \leq T_A \leq 125$ | - | 0.8 | V |
| Output HIGH Voltage | V_{OH} | $I_{OH} = -400\mu A$ $V_{DD} = 4.5V$ (Note 2) | 1, 2, 3 | $-55 \leq T_A \leq 125$ | 2.6 | - | V |
| Output LOW Voltage | V_{OL} | $I_{OL} = +2.0mA$ $V_{CC} = 4.5V$ (Note 2) | 1, 2, 3 | $-55 \leq T_A \leq 125$ | - | 0.4 | V |
| Input Leakage Current | I_I | $V_{IN} = V_{CC}$ or GND $V_{CC} = 5.5V$ | 1, 2, 3 | $-55 \leq T_A \leq 125$ | -10 | +10 | μA |
| Output Leakage Current | I_O | $V_{OUT} = V_{CC}$ or GND $V_{CC} = 5.5V$ | 1, 2, 3 | $-55 \leq T_A \leq 125$ | -10 | +10 | μA |
| Clock Input High | V_{IHC} | $V_{CC} = 5.5V$ | 1, 2, 3 | $-55 \leq T_A \leq 125$ | 3.0 | - | V |
| Clock Input Low | V_{ILC} | $V_{CC} = 4.5V$ | 1, 2, 3 | $-55 \leq T_A \leq 125$ | - | 0.8 | V |
| Standby Power Supply Current | I_{CCSB} | $V_{IN} = V_{CC}$ or GND $V_{CC} = 5.5V$, Outputs Open | 1, 2, 3 | $-55 \leq T_A \leq 125$ | - | 500 | μA |
| Operating Power Supply Current | I_{CCOP} | $f = 33MHz$ $V_{CC} = 5.5V$ (Note 3) | 1, 2, 3 | $-55 \leq T_A \leq 125$ | - | 99 | mA |
| Functional Test | FT | (Note 4) | 7, 8 | $-55 \leq T_A \leq 125$ | - | - | |

NOTES:

- Interchanging of force and sense conditions is permitted.
- Operating Supply Current is proportional to frequency, typical rating is 3mA/MHz.
- Tested as follows: $t = 1MHz$, $V_{IH} = 2.6$, $V_{IL} = 0.4$, $V_{OH} \geq 1.5V$, $V_{OL} \leq 1.5V$, $V_{IHC} = 3.4V$, and $V_{ILC} = 0.4V$.

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TABLE 2. AC ELECTRICAL SPECIFICATIONS

Device Guaranteed and 100% Tested

| PARAMETER | SYMBOL | GROUP A SUBGROUP | TEMPERATURE (°C) | -25 (25MHz) | | -33 (33MHz) | | -40 (40MHz) | | UNITS |
|---|------------------|---------------------|----------------------------|----------------|-----|-------------|-----|-------------|-----|-------|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| Clock Period | t _{CP} | 9, 10, 11 | -55 ≤ T _A ≤ 125 | 39 | - | 30 | - | 25 | - | ns |
| Clock Pulse Width High | t _{CH} | 9, 10, 11 | -55 ≤ T _A ≤ 125 | 15 | - | 12 | - | 10 | - | ns |
| Clock Pulse Width Low | t _{CL} | 9, 10, 11 | -55 ≤ T _A ≤ 125 | 15 | - | 12 | - | 10 | - | ns |
| Setup Time D0-6 to \overline{WR} High | t _{DS} | 9, 10, 11 | -55 ≤ T _A ≤ 125 | 17 | - | 16 | - | 14 | - | ns |
| Hold Time D0-6 from \overline{WR} Low | t _{DH} | 9, 10, 11 | -55 ≤ T _A ≤ 125 | 0 | - | 0 | - | 0 | - | ns |
| Setup Time A, \overline{CS} to \overline{WR} Low | t _{AS} | 9, 10, 11 | -55 ≤ T _A ≤ 125 | 5 | - | 5 | - | 5 | - | ns |
| Hold Time A, \overline{CS} from \overline{WR} High | t _{AH} | 9, 10, 11 | -55 ≤ T _A ≤ 125 | 0 | - | 0 | - | 0 | - | ns |
| Pulse Width for \overline{WR} Low | t _{WRL} | 9, 10, 11 | -55 ≤ T _A ≤ 125 | 18 | - | 14 | - | 12 | - | ns |
| Pulse Width for \overline{WR} High | t _{WRH} | 9, 10, 11 | -55 ≤ T _A ≤ 125 | 18 | - | 14 | - | 12 | - | ns |
| \overline{WR} Cycle Time | t _{WP} | 9,10,11 | -55 ≤ T _A ≤ 125 | 39 | - | 30 | - | 25 | - | ns |
| Set-up Time $\overline{STARTIN}$, DLYBLK, to Clock High | t _{IS} | 9, 10, 11 | -55 ≤ T _A ≤ 125 | 15 | - | 12 | - | 10 | - | ns |
| Hold Time $\overline{STARTIN}$, DLYBLK, to Clock High | t _{IH} | 9, 10, 11 | -55 ≤ T _A ≤ 125 | 0 | - | 0 | - | 0 | - | ns |
| Clock to Output Prop. Delay on OUT0-23 | t _{PDO} | 9, 10, 11 | -55 ≤ T _A ≤ 125 | - | 18 | - | 16 | - | 14 | ns |
| Clock to Prop. Delay, on $\overline{STARTOUT}$, BLKDONE, DONE, ADVAL, and BUSY | t _{PDS} | 9, 10, 11 | -55 ≤ T _A ≤ 125 | - | 18 | - | 16 | - | 14 | ns |
| Output Enable Time (Note 6) | t _{EN} | 9, 10, 11 | -55 ≤ T _A ≤ 125 | - | 22 | - | 20 | - | 15 | ns |
| \overline{RST} Low Time | t _{RST} | 9, 10, 11 | -55 ≤ T _A ≤ 125 | 2 Clock Cycles | | | | | | ns |

NOTES:

- AC Testing: V_{CC} = 4.5V and 5.5V, inputs are driven at 3.0V for Logic "1" and 0.0V for a Logic "0". Input and output timing measurements are made at 1.5V for both a logic "1" and "0". CLK is driven at 4.0V and 0V and measured at 2.0V.
- Transition is measured at ±200mV from steady state voltage with loading as specified by test load circuit and C_L = 40pF.

TABLE 3. ELECTRICAL PERFORMANCE SPECIFICATIONS

| PARAMETERS | SYMBOL | TEST CONDITIONS | NOTES | TEMPERATURE | -25 (25MHz) | | -33 (33MHz) | | -40 (40MHz) | | UNITS |
|--------------------|------------------|--|-------|----------------------------|-------------|-----|-------------|-----|-------------|-----|-------|
| | | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| Input Capacitance | C _{IN} | V _{CC} = Open, f = 1MHz, All measurements are referenced to device GND. | 7 | T _A = 25 | - | 10 | - | 10 | - | 10 | pF |
| Output Capacitance | C _{OUT} | V _{CC} = Open, f = 1MHz, All measurements are referenced to device GND. | 7 | T _A = 25 | - | 10 | - | 10 | - | 10 | pF |
| Output Disable | t _{OEZ} | | 7, 8 | -55 ≤ T _A ≤ 125 | - | 22 | - | 20 | - | 15 | ns |

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TABLE 3. ELECTRICAL PERFORMANCE SPECIFICATIONS (Continued)

| PARAMETERS | SYMBOL | TEST CONDITIONS | NOTES | TEMPERATURE | -25 (25MHz) | | -33 (33MHz) | | -40 (40MHz) | | UNITS |
|------------------|-----------------|-----------------|-------|----------------------------|------------------|-----------------|----------------|------|----------------------------|-----|-------|
| | | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| | | | | | Output Rise Time | t _{OR} | | 7, 8 | -55 ≤ T _A ≤ 125 | - | |
| Output Fall Time | t _{OF} | | 7, 8 | -55 ≤ T _A ≤ 125 | - | 5 | - | 5 | - | 3 | ns |

NOTES:

7. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.
8. Loading is as specified in the test load circuit with C_L = 40pF.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

| CONFORMANCE GROUPS | METHOD | SUBGROUPS |
|--------------------|--------------|-------------------------------|
| Initial Test | 100%/5004 | - |
| Interim Test | 100%/5004 | - |
| PDA | 100% | 1 |
| Final Test | 100% | 2, 3, 8A, 8B, 10, 11 |
| Group A | - | 1, 2, 3, 7, 8A, 8B, 9, 10, 11 |
| Groups C and D | Samples/5005 | 1, 7, 9 |

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Burn-In Circuit

| | | | | | | | | | | | |
|---|---------------|-----------------|---------------|-----------------|-----------------|---------------|-----------------|-------|-----------------|-------|-----------------|
| L | | OE \bar{H} | DLY BLK | START OUT | V _{CC} | BLOCK DONE | GND | OUT1 | OUT2 | NC | |
| K | NC | NC | OEL \bar{E} | START IN | ADD VAL | BUSY | DONE | OUT0 | V _{CC} | NC | OUT3 |
| J | RST \bar{B} | V _{CC} | | | | | | | | GND | OUT4 |
| H | CLK | GND | | | | | | | | OUT5 | V _{CC} |
| G | CS \bar{B} | A0 | | | | | | | | OUT6 | OUT7 |
| F | WR \bar{B} | GND | | | | | | | | GND | OUT8 |
| E | D6 | D5 | | | | | | | | OUT9 | V _{CC} |
| D | D4 | D3 | | | | | | | | OUT10 | OUT11 |
| C | D2 | D1 | | | | | | | | GND | OUT12 |
| B | D0 | NC | OUT22 | OUT21 | GND | OUT18 | OUT17 | GND | OUT14 | NC | NC |
| A | | GND | OUT23 | V _{CC} | OUT20 | OUT19 | V _{CC} | OUT16 | OUT15 | OUT13 | |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |

| PGA PIN | PIN NAME | BURN- IN SIGNAL | PGA PIN | PIN NAME | BURN- IN SIGNAL | PGA PIN | PIN NAME | BURN- IN SIGNAL | PGA PIN | PIN NAME | BURN- IN SIGNAL |
|------------|-----------------|-----------------------|------------|-----------------|-----------------------|------------|-----------------|-----------------------|------------|-----------------|-----------------------|
| A2 | GND | GND | B9 | OUT14 | V _{CC} /2 | F11 | OUT8 | V _{CC} /2 | K6 | BUSYB | V _{CC} /2 |
| A3 | OUT23 | V _{CC} /2 | C1 | D2 | F10 | G1 | CSB | F5 | K7 | DONEB | V _{CC} /2 |
| A4 | V _{CC} | V _{CC} | C2 | D1 | F9 | G2 | A0 | F6 | K8 | OUT0 | V _{CC} /2 |
| A5 | OUT20 | V _{CC} /2 | C10 | GND | GND | G10 | OUT6 | V _{CC} /2 | K9 | V _{CC} | V _{CC} |
| A6 | OUT19 | V _{CC} /2 | C11 | OUT12 | V _{CC} /2 | G11 | OUT7 | V _{CC} /2 | K11 | OUT3 | V _{CC} /2 |
| A7 | V _{CC} | V _{CC} | D1 | D4 | F12 | H1 | CLK | F0 | L2 | OEHB | F13 |
| A8 | OUT16 | V _{CC} /2 | D2 | D3 | F11 | H2 | GND | GND | L3 | DLYBLK | F11 |
| A9 | OUT15 | V _{CC} /2 | D10 | OUT10 | V _{CC} /2 | H10 | OUTS | V _{CC} /2 | L4 | STARTOUTB | V _{CC} /2 |
| A10 | OUT13 | V _{CC} /2 | D11 | OUT11 | V _{CC} /2 | H11 | V _{CC} | V _{CC} | LS | V _{CC} | V _{CC} |
| B1 | D0 | F8 | E1 | D6 | F7 | J1 | RSTB | F14 | L6 | BLOCKDONEB | V _{CC} /2 |
| B3 | OUT22 | V _{CC} /2 | E2 | D5 | F13 | J2 | V _{CC} | V _{CC} | L7 | GND | GND |
| B4 | OUT21 | V _{CC} /2 | E10 | OUT9 | V _{CC} /2 | J10 | GND | GND | L8 | OUT1 | V _{CC} /2 |
| B5 | GND | GND | E11 | V _{CC} | V _{CC} | J1 1 | OUT4 | V _{CC} /2 | L9 | OUT2 | V _{CC} /2 |
| B6 | OUT18 | V _{CC} /2 | F1 | WRB | F4 | K3 | OELB | F12 | | | |
| B7 | OUT17 | V _{CC} /2 | F2 | GND | GND | K4 | START1NB | F6 | | | |
| B8 | GND | GND | F10 | GND | GND | K5 | ADVALB | V _{CC} /2 | | | |

NOTES:

9. V_{CC}/2 (2.7V ± 10%) used for outputs only.
10. 47Ω (±20%) resistor connected to all pins except V_{CC} and GND.
11. V_{CC} = 5.5 ± 0.5V.
12. 0.1μF (min) capacitor between V_{CC} and GND per position.
13. F0 = 100kHz ± 10%, F1 = F0/2, F2 = F1/2....., F11 = F10/2, 40% -60% Duty Cycle.
14. Input voltage limits: V_{IL} = 0.8V max., V_{IH} = 4.5V ± 10%.

Die Characteristics

DIE DIMENSIONS:

186 mils x 222 mils x 19 ±1mils

METALLIZATION:

Type: Si - Al or Si-Al-Cu

Thickness: 8kÅ

GLASSIVATION:

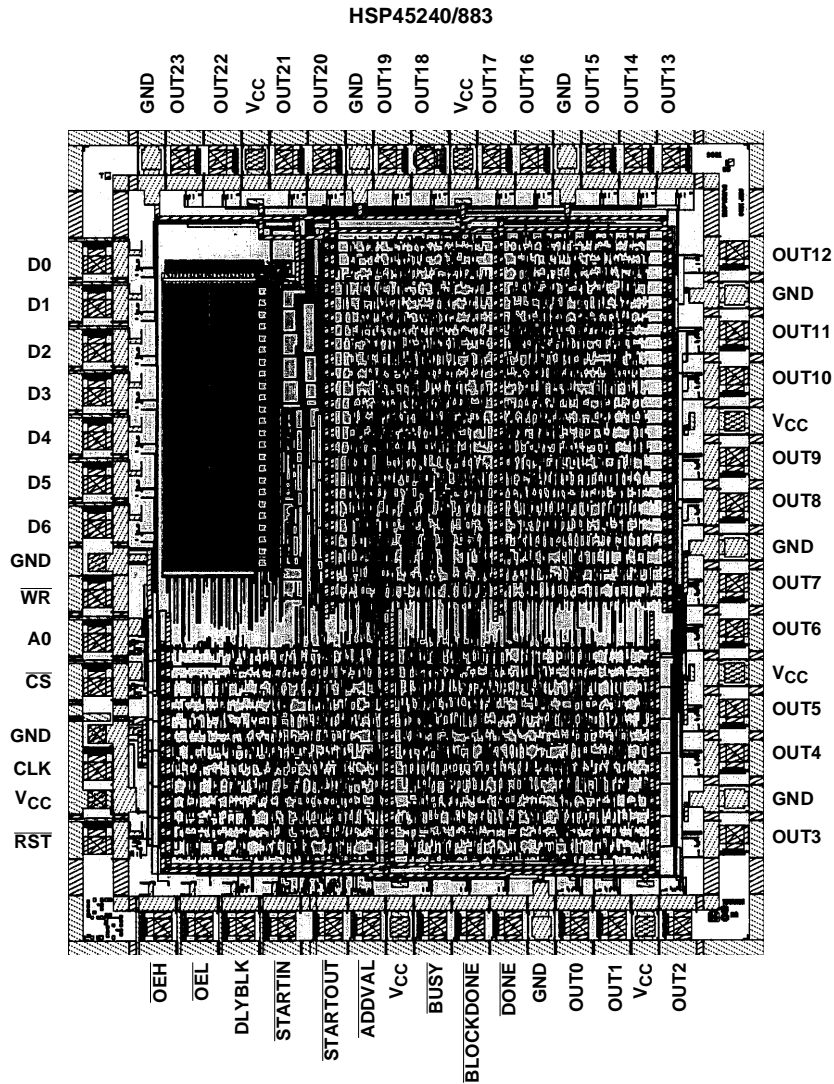
Type: Nitrox

Thickness: 10kÅ

WORST CASE CURRENT DENSITY:

1.8 x 10⁵A/cm²

Metallization Mask Layout



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