

August 1997

### Features

- Hour Meter Requires Only 4 Parts Total
- Micropower Operation: < 1 $\mu$ A at 2.8V (Typ)
- 10 Year Operation On One Lithium Cell. 2<sup>1</sup>/<sub>2</sub> Year Battery Life with Display Connected
- Directly Drives 5<sup>1</sup>/<sub>2</sub> Digit LCD
- 14 Programmable Modes of Operation
- Times Hrs., 0.1 Hrs., 0.01 Hrs., 0.1 Mins.
- Counts 1's, 10's, 100's, 1000's
- Dual Function Input Circuit
  - Selectable Debounce for Counter
  - High-Pass Filter for Timer
- Direct AC Line Triggering with Input Resistor
- Winking "Timer Active" Display Output
- Display Test Feature

### Applications

- AC or DC Hour Meters
- AC or DC Totalizers
- Portable Battery Powered Equipment
- Long Range Service Meters

### Ordering Information

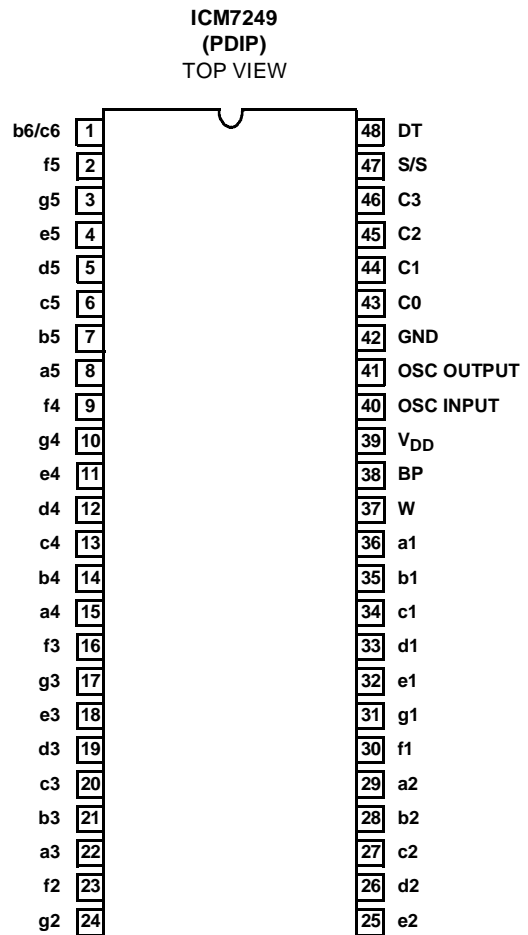
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
ICM7249IPM	-20 to 85	48 Ld PDIP	E48.6

### Description

The ICM7249 Timer/Counter is intended for long-term battery-supported industrial applications. The ICM7249 typically draws 1 $\mu$ A during active timing or counting, due to Intersil' special low-power design techniques. This allows more than 10 years of continuous operation without battery replacement. The chip offers four timing modes, eight counting modes and four test modes.

The ICM7249 is a 48 lead device, powered by a single DC voltage source and controlled by a 32.768kHz quartz crystal. No other external components are required. Inputs to the chip are TTL-compatible and outputs drive standard direct drive LCD segments.

### Pinout





# ICM7249

## Absolute Maximum Ratings

Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 6V  
 Input Voltage, Pins 43 - 48 (Note 1) . . ( $V_{SS} - 0.3V$ ) to ( $V_{DD} + 0.3V$ )

## Operating Conditions

Temperature Range . . . . . -40°C to 85°C

## Thermal Information

Thermal Resistance (Typical, Note 2)  $\theta_{JA}$  (°C/W)  
 PDIP Package . . . . . 50  
 Maximum Junction Temperature. . . . . 150°C  
 Maximum Storage Temperature Range . . . . . -65°C to 150°C  
 Maximum Lead Temperature (Soldering, 10s) . . . . . 300°C

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTES:

1. Due to the SCR structure inherent in junction-isolated CMOS devices, the circuit can be put in a latchup mode if large currents are injected into device inputs or outputs. For this reason special care should be taken in a system with multiple power supplies to prevent voltages being applied to inputs or outputs before power is applied. If only inputs are affected, latchup also can be prevented by limiting the current into the input terminal to less than 1mA.
2.  $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

**Electrical Specifications** Temperature = -40°C to 85°C,  $V_{DD} = 2.5V$  to  $5.5V$ ,  $V_{SS} = 0V$ , Unless Otherwise Specified. Typical Specifications Measured at Temperature = 25°C and  $V_{DD} = 2.8V$ , Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage, $V_{DD}$	Note 1	2.5	-	5.5	V
Operating Current, $I_{DD}$	All Inputs = $V_{DD}$ or GND, Note 2 $V_{DD} = 2.8V$	-	1.0	10.0	$\mu A$
	$V_{DD} = 5.5V$	-	4.0	20.0	$\mu A$
<b>INPUT CURRENT</b>					
C0 - C3, $I_{IN}$	All Inputs $V_{DD}$ or GND $V_{DD} = 2.8V$ Note 3	0.0	-	1	$\mu A$
S/S, $I_{SS}$		0.5	1.5	3.0	$\mu A$
DT, $I_{DT}$		40.0	-	110	$\mu A$
<b>INPUT VOLTAGE</b>					
C0 - C3, DT, S/S $V_{IL}$		-	-	$0.3V_{DD}$	V
		$V_{IH}$	$0.7V_{DD}$	-	-
Segment Output Voltage $V_{OL}$	$I_{OL} = 1\mu A$	-	-	0.8	V
	$I_{OH} = 1\mu A$	$V_{DD} - 0.8$	-	-	V
Backplane Output Voltage $V_{OL}$	$I_{OL} = 10\mu A$	-	-	0.8	V
	$I_{OH} = 10\mu A$	$V_{DD} - 0.8$	-	-	V
<b>OSCILLATOR STABILITY</b>					
Temperature = 25°C, $V_{DD} = 2.5V$ to $5.5V$		-	0.1	-	ppm
Temperature = -40°C to 85°C, $V_{DD} = 2.5V$ to $5.5V$		-	5	-	ppm
<b>S/S PULSE WIDTH</b>					
High-Pass Filter (Modes 0 - 3), $t_{HP}$		5	-	10,000	$\mu s$
Debounce (Modes 4, 6, 8, 10), $t_{DE}$		10,000	-	-	$\mu s$
Without Debounce (Modes 5, 7, 9, 11), $t_{DE}$		5	-	-	$\mu s$

### NOTES:

1. Internal reset to 00000 requires a maximum  $V_{DD}$  rise time of 1 $\mu s$ . Longer rise times at power-up may cause improper reset.
2. Operating current is measured with the LCD disconnected, and input current  $I_{SS}$  and  $I_{DT}$  supplied externally.
3. Inputs C0 - C3 are latched internally and draw no DC current after switching. During switching, a 90 $\mu A$  peak current may be drawn for 10ns.

Timing Waveforms

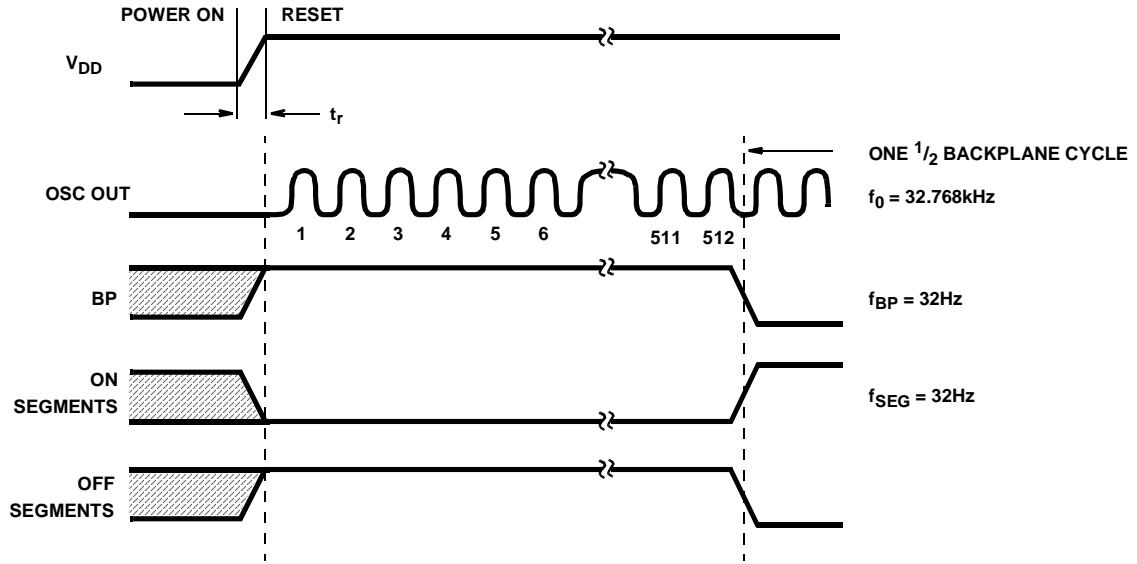


FIGURE 1. POWER ON/RESET WAVEFORMS

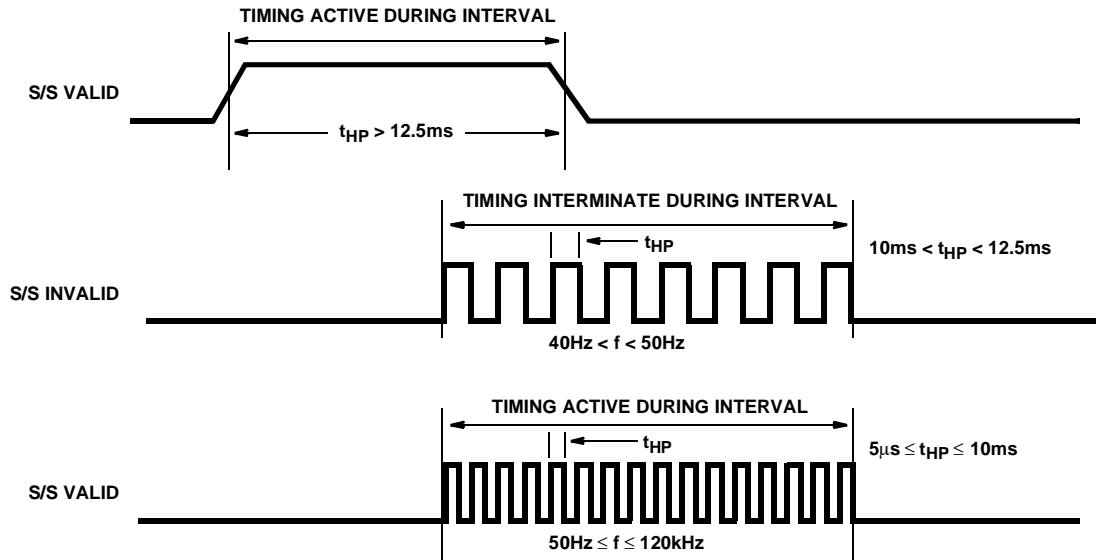


FIGURE 2. START/STOP INPUT HIGH-PASS FILTERING IN TIMING MODES

Timing Waveforms (Continued)

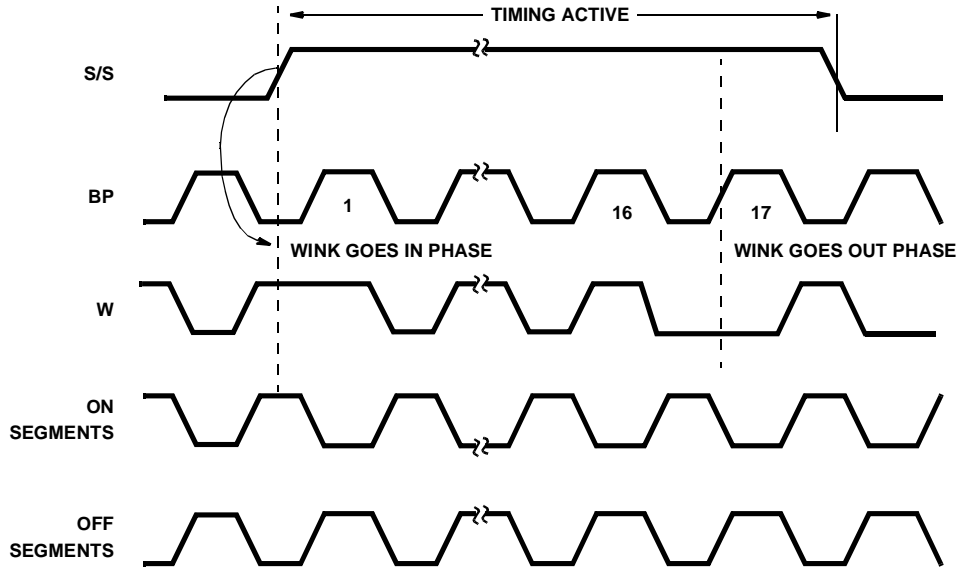


FIGURE 3. WINK WAVEFORMS IN TIMING MODES

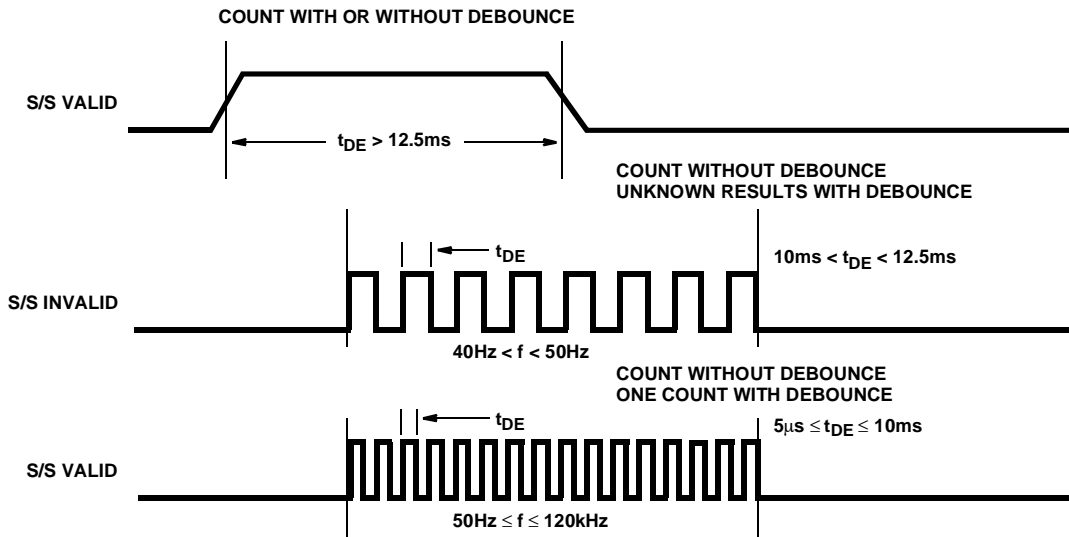


FIGURE 4. START/STOP INPUT DEBOUNCE FILTERING IN COUNTING MODES

**Timing Waveforms** (Continued)

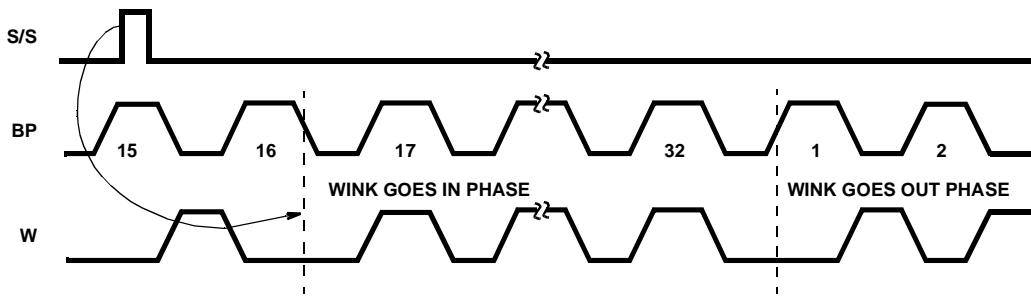


FIGURE 5. WINK WAVEFORMS IN COUNTING MODES

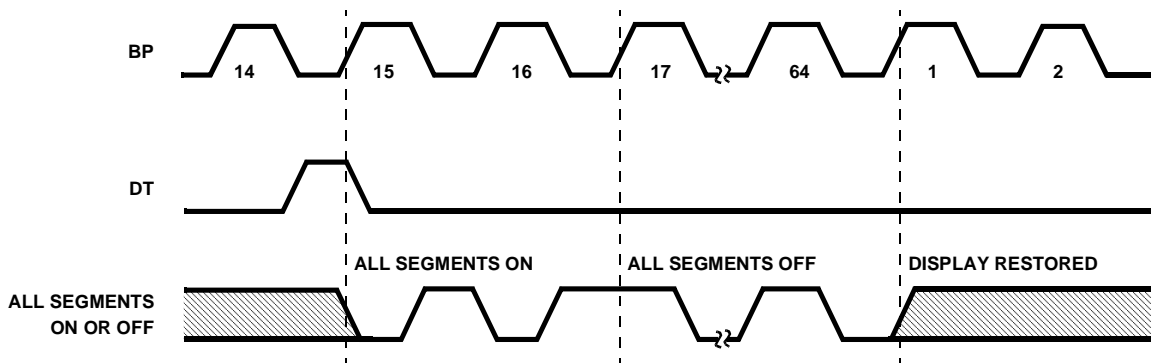


FIGURE 6. DISPLAY TESTING

**Pin Descriptions**

PIN	NAME	DESCRIPTION
1	b6/c6	Half-Digit LCD Segment Output.
2	f5	Seven-Segment LCD Output.
3	g5	Seven-Segment LCD Output.
4	e5	Seven-Segment LCD Output.
5	d5	Seven-Segment LCD Output.
6	c5	Seven-Segment LCD Output.
7	b5	Seven-Segment LCD Output.
8	a5	Seven-Segment LCD Output.
9	f4	Seven-Segment LCD Output.
10	g4	Seven-Segment LCD Output.
11	e4	Seven-Segment LCD Output.
12	d4	Seven-Segment LCD Output.
13	c4	Seven-Segment LCD Output.
14	b4	Seven-Segment LCD Output.
15	a4	Seven-Segment LCD Output.

PIN	NAME	DESCRIPTION
16	f3	Seven-Segment LCD Output.
17	g3	Seven-Segment LCD Output.
18	e3	Seven-Segment LCD Output.
19	d3	Seven-Segment LCD Output.
20	c3	Seven-Segment LCD Output.
21	b3	Seven-Segment LCD Output.
22	a3	Seven-Segment LCD Output.
23	f2	Seven-Segment LCD Output.
24	g2	Seven-Segment LCD Output.
25	e2	Seven-Segment LCD Output.
26	d2	Seven-Segment LCD Output.
27	c2	Seven-Segment LCD Output.
28	b2	Seven-Segment LCD Output.
29	a2	Seven-Segment LCD Output.
30	f1	Seven-Segment LCD Output.

PIN	NAME	DESCRIPTION
31	91	Seven-Segment LCD Output.
32	e1	Seven-Segment LCD Output.
33	d1	Seven-Segment LCD Output.
34	c1	Seven-Segment LCD Output.
35	b1	Seven-Segment LCD Output.
36	a1	Seven-Segment LCD Output.
37	W	Wink-Segment Output.
38	BP	Backplane for LCD Reference.
39	V <sub>DD</sub>	Positive Supply Voltage.
40	OSC IN	Quartz Crystal Connection.
41	OSC OUT	Quartz Crystal Connection.
42	GND	Supply GRouND.
43	C0	Mode-select Control Input.
44	C1	Mode-select Control Input.
45	C2	Mode-select Control Input.
46	C3	Mode-select Control Input.
47	S/S	Start/Stop Input.
48	DT	Display Test Input.

TABLE 1. MODE SELECT TABLE

MODE	CONTROL PIN INPUTS				FUNCTION
	C3	C2	C1	C0	
0	0	0	0	0	1 Hour Interval Timer
1	0	0	0	1	0.1 Hour Interval Timer
2	0	0	1	0	0.01 Hour Interval Timer
3	0	0	1	1	0.1 Minute Interval Timer
4	0	1	0	0	1's Counter with Debounce
5	0	1	0	1	1's Counter
6	0	1	1	0	10's Counter with Debounce
7	0	1	1	1	10's Counter
8	1	0	0	0	100's Counter with Debounce
9	1	0	0	1	100's Counter
10	1	0	1	0	1000's Counter with Debounce
11	1	0	1	1	1000's counter
12	1	1	0	0	Test Display Digits
13	1	1	0	1	Internal Test
14	1	1	1	0	Internal Test
15	1	1	1	1	Reset

**Detailed Description**

As the Functional Diagram shows the device consists of the following building blocks:

- A 32.768kHz crystal oscillator with the associated dividers to generate timebase signals for periods of 1s (frequency of 1Hz), 6s (1/10 min) and 36s (1/100 hour), and 32Hz signal for LCD drivers.
- A debounce/high-pass detect circuit for the S/S (Start/Stop) input.
- A chain of cascaded decade counters, 3 decade counters for prescaling and 5<sup>1/2</sup> BCD decade counters for display driving.
- Display control circuitry and BCD to 7-segment decoder/drivers.
- A control decoder to select different modes of operation. This is done by routing different signals to the different points in the chain of decade counters.

The control decoder has 4 inputs for selecting 16 possible modes of operation, numbered 0 to 15. The 16 modes are selected by placing the binary equivalent of the mode number on inputs C0 to C3. Table 2 shows the control inputs and the modes of operation.

After applying power, the ICM7249 requires a rise time of t<sub>r</sub> to become active and for oscillation to begin, as shown in Figure 1. The BP (backplane) output changes state once every 512 cycles of the crystal oscillator, resulting in a square wave of 32Hz. The display segments drive signal has the same level and frequency as BP. Segments are off when in phase with BP and are on when out of phase with BP.

A non-multiplexed LCD display is used because it is more stable over temperature and allows many standard LCD displays to be used.

**Timer Mode of Operation**

In modes 0 to 3 the device functions as an interval timer. In this mode, one of the timebase signals will be routed to the decade counters at a proper point in the chain. Depending on the selected mode the display will be incremented at 0.1 min, 0.01 hour, 0.1 hour or 1 hour rates.

Control of timing function is handled by the S/S input. There is a high-pass filtering effect on the S/S input in timer modes. Referring to Figure 2, timing is active when either S/S is held high for more than 12.5ms, or if input frequency is 50Hz to 120kHz. Driving S/S with a frequency between 40Hz to 50Hz has an indeterminate effect on timing and should be avoided. Note that the t<sub>HP</sub> intervals shown on Figure 1 are also applied to the intervals when the S/S input is low.

**Counter Mode of Operation**

In modes 4 to 11 the device functions as an event counter or totalizer. In this mode the S/S input will be routed to the decade counters at a proper point in the chain. Each positive transition of the S/S will be registered as one count. Depending on the selected mode, the display will be incremented by each pulse, every 10 pulses, every 100 pulses or every 1000 pulses.

In counter modes 4, 6, 8 and 10 the S/S input is subjected to

debounce filtering. Referring to Figure 4, only the pulses with a frequency of less than 40Hz are valid and will be counted. Input pulses with a frequency of 50Hz to 120kHz are not counted individually, but each burst of input pulses will be counted as one pulse if it lasts at least 12.5ms. Driving S/S with a frequency between 40Hz to 50Hz has an indeterminate result and should be avoided.

In counter modes 5, 7, 9 and 11 the S/S input is not subjected to any debouncing action and input pulses will be counted up to a frequency of 120kHz.

**Wink Segment**

The wink segment is provided as a annunciator to indicate the ICM7249 is working. It can be connected to any kind of annunciator on an LCD, like the flashing colons in a clock type LCD.

In the timer modes, the wink segment flashes while timing is taking place. The wink segment waveform is shown on Figure 3 for timer modes. On the positive transition of S/S, the wink output turns off. It remains off for 16 BP cycles and turns back on for another 16 cycles. If timing is still active, this will be repeated, giving a wink flash rate of 1Hz; otherwise, the wink segment remains on while timing is not active.

In the counter modes, the wink segment stays on until a pulse occurs on S/S input, then it winks off indicating a pulse is counted. This will happen regardless of whether the display is incremented. Figure 5 shows the wink waveform for counter modes. When a count occurs, the wink segment turns off at the end of the 16th BP cycle and turns back on at the end of the 32nd BP cycle, giving a half-second wink. If the counting occurs more frequently than once a second, the wink output will continue to flash at the constant rate of 1Hz.

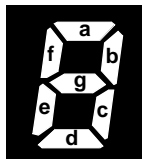


FIGURE 7. DIGITS SEGMENT ASSIGNMENT

**Display Test and Reset**

The display may be tested at any time without disturbing operation by pulsing DT high, as seen in Figure 6. On the next positive transition of BP, all the segments turn on and remain on until the end of the 16th BP cycle. This takes a half-second or less. All the segments then turn off for an additional 48 BP cycles (the end of the 64th cycle), after which valid data returns to the display. As long as DT is held high, the segments will remain on.

Additional display testing is provided by using mode 12. In this mode each displayed decade is incremented on each positive transition of S/S. Modes 13 and 14 are manufacturer testing only.

Mode 15 resets all the decades and internal counters to zero, essentially bringing everything back to power-up status.

**Applications**

A typical use of the ICM7249 is seen in Figure 8, the Motor Hour Meter. In this application the ICM7249 is configured as an hours-in-use meter and shows how many whole hours of line voltage have been applied. The resistor network and high-pass filtering allow AC line activation of the S/S input. This configuration, which is powered by a 3V lithium cell, will operate continuously for 2<sup>1</sup>/<sub>2</sub> years. Without the display, which only needs to be connected when a reading is required, the span of operation is extended to 10 years.

When the ICM7249 is configured as an attendance counter, as shown in Figure 9, the display shows each increment. By using mode 2, external debouncing of the gate switch is unnecessary, provided the switch bounce is less than 10ms.

The 3V lithium battery can be replaced without disturbing operation if a suitable capacitor is connected in parallel with it. The display should be disconnected, if possible, during the procedure to minimize current drain. The capacitor should be large enough to store charge for the amount of time needed to physically replace the battery ( $\Delta t = \Delta VC/I$ ). A 100 $\mu$ F capacitor initially charged to 3V will supply a current of 1.0 $\mu$ A for 50 seconds before its voltage drops to 2.5V, which is the minimum operating voltage for the ICM7249.

Before the battery is removed, the capacitor should be placed in parallel, across the V<sub>DD</sub> and GND terminals. After the battery is replaced, the capacitor can be removed and the display reconnected.



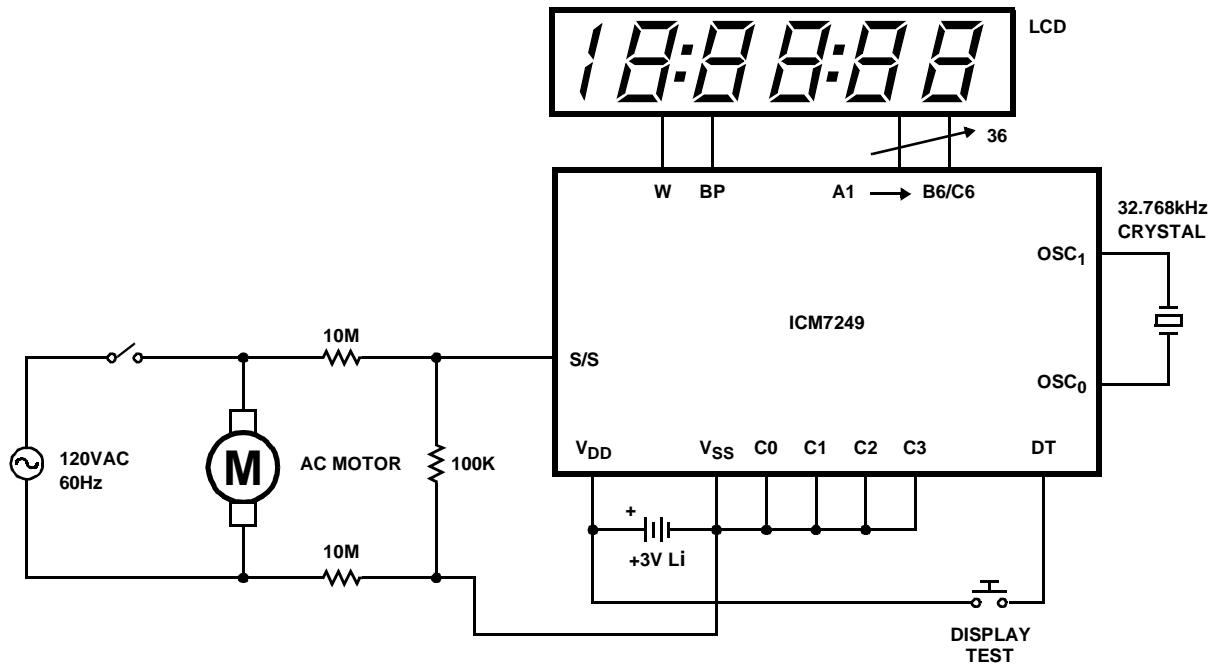


FIGURE 8. MOTOR HOUR METER

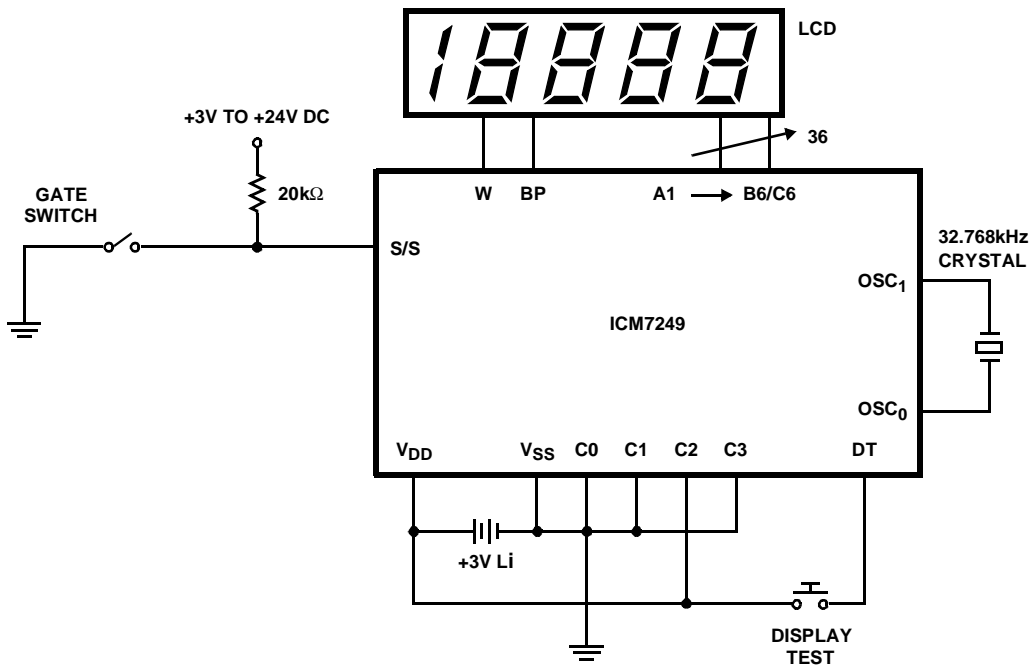


FIGURE 9. ATTENDANCE COUNTER

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