

ADVANCED MODULATION SATELLITE RECEIVER EVALUATION SYSTEM

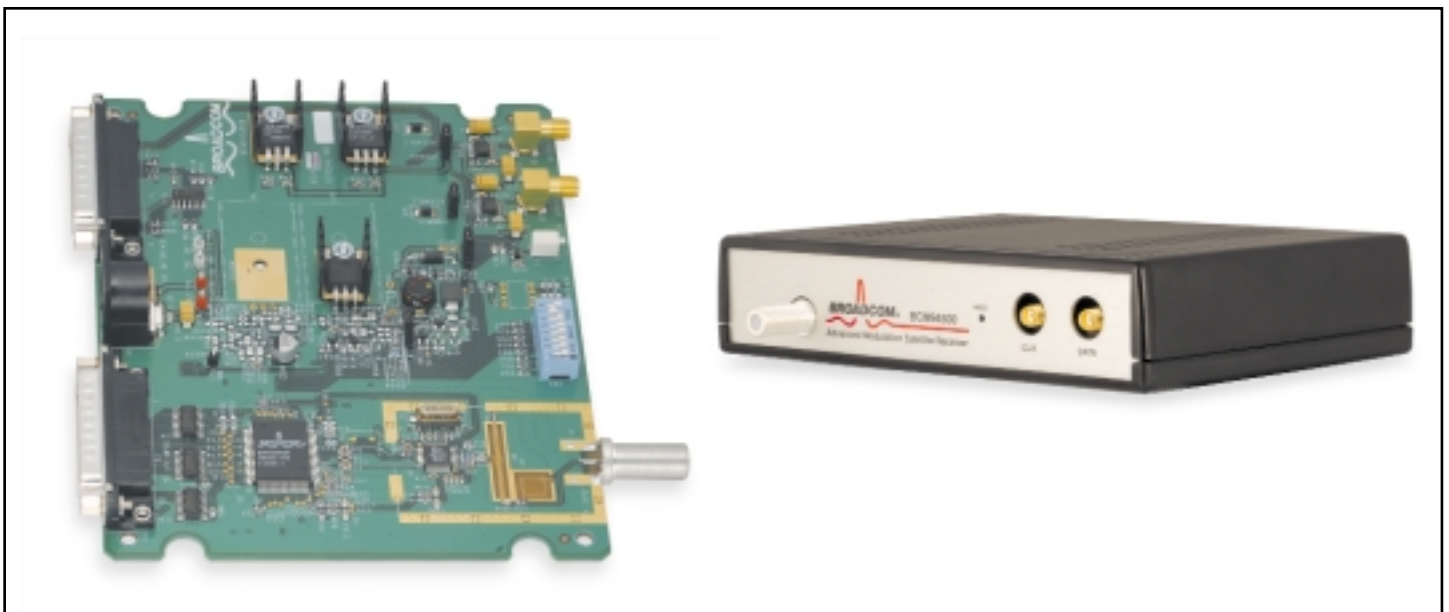
BCM94500 FEATURES

- Evaluation system based on BCM3440 direct conversion CMOS satellite tuner and BCM4500 advanced modulation satellite receiver
- Supports full satellite input range (950–2150 MHz)
- Standard MPEG-2 output in DIRECTV® or DVB format
- Standard DVB-SPI MPEG output interface: 25-pin D connector with LVDS line drivers
- Interfaces to BCM97031 HDTV decoder/graphics evaluation system
- I²C bus interface to PC parallel port for system control
- Internal BERT and external BERT interface
- DiSEqC™ (Digital Satellite Equipment Control) 2.0 2-way interface
- Complete reference design includes
 - Schematic drawings and Gerber files
 - Bill of materials (BOM)
 - Data sheet
 - Software source code
 - User manual
- Compatible with Windows® 95, 98, 2000 or NT host PC operating systems

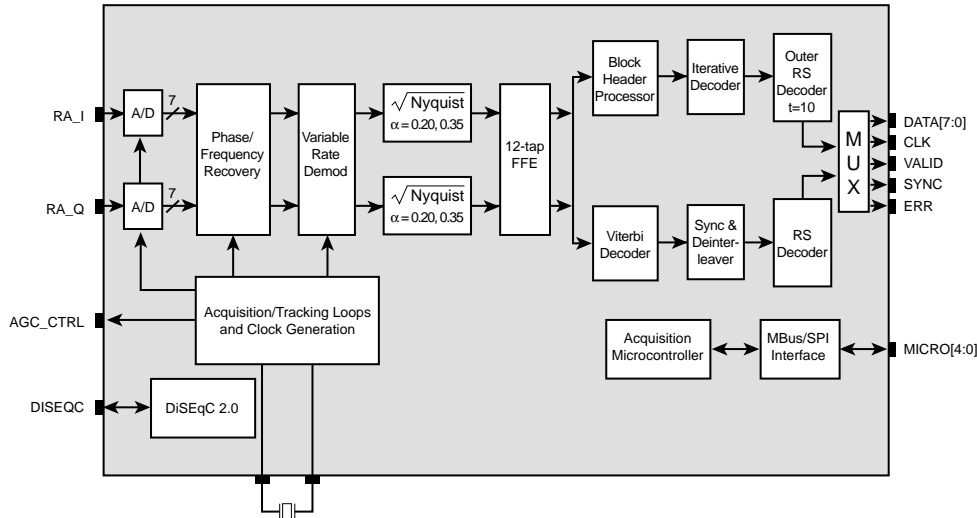
SUMMARY OF BENEFITS

- Demonstrates the high performance of the BCM4500 advanced modulation satellite receiver, which supports QPSK, 8PSK and 16 QAM with a turbo code FEC.
- Supports legacy modes based on DIRECTV® and DVB-S QPSK standards.
- High-performance direct conversion BCM3440 satellite tuner exceeds performance of typical single-chip satellite tuners for increased system performance.
- Highly integrated BCM3440 and BCM4500 devices enable low-cost implementation with minimal external components.
- Host software uses the BCM4500 high-level application program interface (API) implemented in the on-chip microcontroller contained in the BCM4500.
- BCM3440 also controlled by the host through the BCM4500 API.
- Highly integrated Windows® software enables evaluation of all advanced modulation/turbo modes, as well as legacy DVB and DIRECTV modes.
- Easy interface to PC via parallel port and I²C connector on BCM94500.
- Interface to BCM4500 Integrated DiSEqC™ 2.0 for two-way communication with external hardware.

BCM94500 Advanced Modulation Satellite Receiver Evaluation System



BCM4500 Block Diagram



The **BCM94500** advanced modulation satellite receiver evaluation system is intended for use by satellite systems engineers for the evaluation of the high performance offered by the BCM4500 advanced modulation satellite receiver with turbo code FEC. It is also intended for use by hardware designers and software developers to reduce product design and development time.

This evaluation platform provides the ideal environment for systems engineers to explore the emerging technology enabled by turbo code FECs and the unparalleled performance offered by the BCM4500. The simplified user interface gives engineers easy access to various system parameters, allowing them to select optimal settings for the BCM4500 to match the link budget requirements. Hardware engineers and software developers can use the **BCM94500** as a baseline for the final product architecture and also use it as a test and measurement device to verify their final product performance.

The **BCM94500** supports QPSK, 8PSK and 16 QAM operation with turbo code FEC over a range of coding and symbol rates. The system also supports DVB-S and DIRECTV® modes for legacy system compatibility testing.

The **BCM94500** contains the BCM3440 direct conversion CMOS satellite tuner, which supports the full 950–2150 MHz operating range. Baseband IQ outputs are connected directly to the BCM4500 receiver. All tuner AGC loops are controlled by the BCM4500. The BCM4500 process the I/Q baseband signal

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through a variable rate advanced modulation receiver and can use either the turbo code FEC or legacy DVB-S/DIRECTV FEC. The MPEG-2, DIRECTV- or DVB-compliant output is available on a 25-pin connector, driven by line drivers for connection to external test equipment or for interfacing to the BCM97031 HDTV video/graphics subsystem for decoding and display. Additional on-board components are provided as an interface between the BCM4500 DiSeqC™ controller and external devices, such as multiple switches.

The **BCM94500** is delivered with Windows® software for easy installation and testing. The host software communicates with the **BCM94500** via I²C protocol via the PC parallel port. The host software contains several screens for chip configuration, constellation monitoring, and performance monitoring including SNR, block error calculations and other FEC performance parameters. Testing is simplified by having the option to use other external BERTs or the BCM4500 on-chip BERT.

A detailed user manual is provided that describes the host software interface as well as the operation of the BCM4500 API for embedded host software development. All acquisition scripts and monitoring calculations are performed in the BCM4500 internal microcontroller and are transparent to the host. The **BCM94500** package is delivered with the user manual, schematic drawings, and a bill of materials. PCB Gerber files are also available.

