NBSG16

2.5V/3.3V SiGe Differential Receiver/Driver with RSECL* Outputs

*Reduced Swing ECL

The NBSG16 is a differential receiver/driver targeted for high frequency applications. The device is functionally equivalent to the EP16 and LVEP16 devices with much higher bandwidth and lower EMI capabilities.

Inputs incorporate internal 50 Ω termination resistors and accept NECL (Negative ECL), PECL (Positive ECL), HSTL, LVTTL, LVCMOS, CML, or LVDS. Outputs are RSECL (Reduced Swing ECL), 400 mV.

The V_{BB} and V_{MM} pins are internally generated voltage supplies available to this device only. The V_{BB} is used as a reference voltage for single-ended NECL or PECL inputs and the V_{MM} pin is used as a reference voltage for LVCMOS inputs. For all single-ended input conditions, the unused complementary differential input is connected to V_{BB} or V_{MM} as a switching reference voltage. V_{BB} or V_{MM} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{MM} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} and V_{MM} outputs should be left open.

- Maximum Input Clock Frequency > 12 GHz Typical
- Maximum Input Data Rate > 12 Gb/s Typical
- 120 ps Typical Propagation Delay
- 40 ps Typical Rise and Fall Times
- RSPECL Output with Operating Range: V_{CC} = 2.375 V to 3.465 V with V_{EE} = 0 V
- RSNECL Output with RSNECL or NECL Inputs with Operating Range: V_{CC} = 0 V with V_{EE} = -2.375 V to -3.465 V
- RSECL Output Level (400 mV Peak-to-Peak Output), Differential Output Only
- 50 Ω Internal Input Termination Resistors
- Compatible with Existing 2.5 V/3.3 V LVEP, EP, and LVEL Devices
- V_{BB} and V_{MM} Reference Voltage Output

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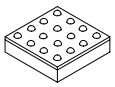
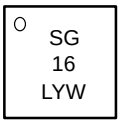
MARKING DIAGRAM*



FCBGA-16
BA SUFFIX
CASE 489



QFN-16
MN SUFFIX
CASE 485G

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For further details, refer to Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
NBSG16BA	4x4 mm FCBGA-16	100 Units/Tray
NBSG16BAR2	4x4 mm FCBGA-16	500/Tape & Reel
NBSG16MN	3x3 mm QFN-16	123 Units/Rail
NBSG16MNR2	3x3 mm QFN-16	3000/Tape & Reel

Board	Description
NBSG16BAEVB	NBSG16BA Evaluation Board

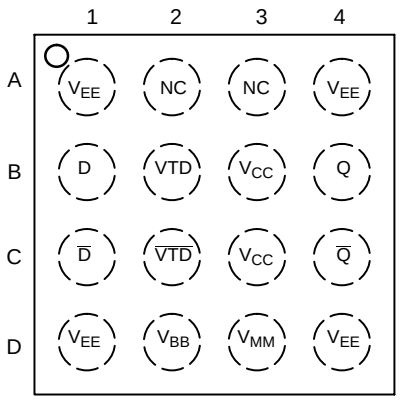


Figure 1. BGA-16 Pinout (Top View)

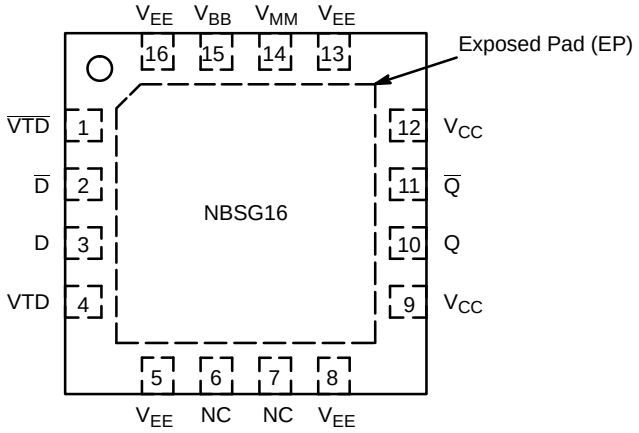


Figure 2. QFN-16 Pinout (Top View)

Table 1. Pin Description

Pin		Name	I/O	Description
BGA	QFN			
C2	1	$\overline{VTD}$	-	Internal 50 Ω Termination Pin. See Table 2.
C1	2	$\overline{D}$	ECL, CML, LVCMOS, LVDS, LVTTL Input	Inverted Differential Input. Internal 75 kΩ to V_{EE} and 36.5 kΩ to V_{CC}.
B1	3	D	ECL, CML, LVCMOS, LVDS, LVTTL Input	Noninverted differential input. Internal 75 kΩ to V_{EE}.
B2	4	VTD	-	Internal 50 Ω Termination Pin. See Table 2.
A1,D1,A4, D4	5,8,13,16	V_{EE}	-	Negative Supply Voltage
A2,A3	6,7	NC	-	No Connect
B3,C3	9,12	V_{CC}	-	Positive Supply Voltage
B4	10	Q	RSECL Output	Noninverted Differential Output. Typically Terminated with 50 Ω to $V_{TT} = V_{CC}$ - 2 V
C4	11	$\overline{Q}$	RSECL Output	Inverted Differential Output. Typically Terminated with 50 Ω to $V_{TT} = V_{CC}$ - 2 V
D3	14	V_{MM}	-	LVCMOS Reference Voltage Output. (V_{CC} - V_{EE})/2
D2	15	V_{BB}	-	ECL Reference Voltage Output
N/A	-	EP	-	Exposed Pad. (Note 2)

1. The NC pins are electrically connected to the die and MUST be left open.
2. All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation. The thermally exposed pad on package bottom (see case drawing) must be attached to a heat-sinking conduit.
3. In the differential configuration when the input termination pins (VTD, $\overline{VTD}$) are connected to a common termination voltage, and if no signal is applied then the device will be susceptible to self-oscillation.

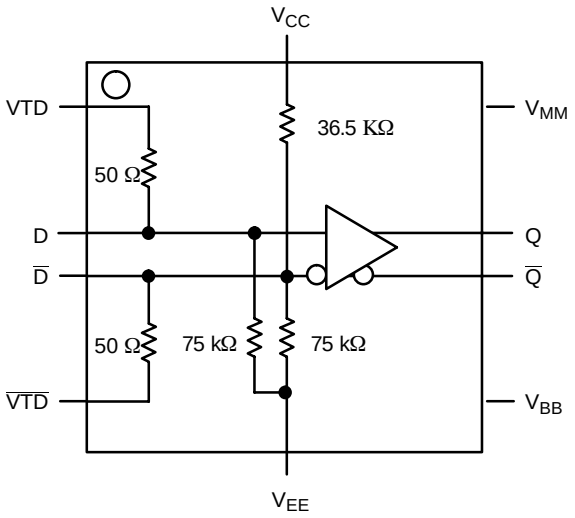


Figure 3. Logic Diagram

Table 2. Interfacing Options

INTERFACING OPTIONS	CONNECTIONS
CML	Connect VTD and $\overline{VTD}$ to V_{CC}
LVDS	Connect VTD and $\overline{VTD}$ together
AC-COUPLED	Bias VTD and $\overline{VTD}$ Inputs within (V_{IHCMR}) Common Mode Range
RSECL, PECL, NECL	Standard ECL Termination Techniques
LVTTL	The external voltage should be applied to the unused complementary differential input. Nominal voltage is 1.5 V for LVTTL.
LVCMOS	V_{MM} should be connected to the unused complementary differential input.

Table 3. ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor (D, $\overline{D}$)		75 kΩ
Internal Input Pullup Resistor ($\overline{D}$)		36.5 kΩ
ESD Protection	Human Body Model Machine Model	> 2 kV > 100 V
Moisture Sensitivity (Note 1)	FCBGA-16 QFN-16	Level 3 Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count		167
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	Positive Power Supply	V_{EE} = 0 V		3.6	V
V_{EE}	Negative Power Supply	V_{CC} = 0 V		-3.6	V
V_I	Positive Input Negative Input	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	3.6 -3.6	V V
V_{INPP}	Differential Input Voltage |D - $\overline{D}$|	V_{CC} - V_{EE} ≥ 2.8 V V_{CC} - V_{EE} < 2.8 V		2.8 $\|V_{CC} - V_{EE}\|$	V V
I_{out}	Output Current	Continuous Surge		25 50	mA mA
I_{BB}	V_{BB} Sink/Source			1	mA
I_{MM}	V_{MM} Sink/Source			1	mA
T_A	Operating Temperature Range			-40 to +85	°C
T_{stg}	Storage Temperature Range			-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient) (Note 3)	0 LFPM 500 LFPM 0 LFPM 500 LFPM	16 FCBGA 16 FCBGA 16 QFN 16 QFN	108 86 41.6 35.2	°C/W °C/W °C/W °C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	1S2P (Note 3) 2S2P (Note 4)	16 FCBGA 16 QFN	5 4.0	°C/W °C/W
T_{sol}	Wave Solder	< 15 sec.		225	°C

2. Maximum Ratings are those values beyond which device damage may occur.
3. JEDEC standard multilayer board - 1S2P (1 signal, 2 power)
4. JEDEC standard multilayer board - 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

Table 5. DC CHARACTERISTICS, INPUT WITH RSPECL OUTPUT V_{CC} = 2.5 V; V_{EE} = 0 V (Note 5)

		-40 °C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Negative Power Supply Current	17	23	29	17	23	29	17	23	29	mA
V_{OH}	Output HIGH Voltage (Note 6)	1450	1530	1575	1525	1565	1600	1550	1590	1625	mV
V_{OUTPP}	Output Voltage Amplitude	350	410	525	350	410	525	350	410	525	mV
V_{IH}	Input HIGH Voltage (Single-Ended) (Note 7)	V_{THR} + 75 mV	V_{CC} - 1.0*	V_{CC}	V_{THR} + 75 mV	V_{CC} - 1.0*	V_{CC}	V_{THR} + 75 mV	V_{CC} - 1.0*	V_{CC}	V
V_{IL}	Input LOW Voltage (Single-Ended) (Note 7)	V_{EE}	V_{CC} - 1.4*	V_{THR} - 75 mV	V_{EE}	V_{CC} - 1.4*	V_{THR} - 75 mV	V_{EE}	V_{CC} - 1.4*	V_{THR} - 75 mV	V
V_{BB}	PECL Output Voltage Reference	1080	1140	1200	1080	1140	1200	1080	1140	1200	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 8) (Differential Configuration)	1.2		2.5	1.2		2.5	1.2		2.5	V
V_{MM}	CMOS Output Voltage Reference $V_{CC}/2$	1100	1250	1400	1100	1250	1400	1100	1250	1400	mV
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
I_{IH}	Input HIGH Current (@ V_{IH})		30	100		30	100		30	100	μA
I_{IL}	Input LOW Current (@ V_{IL})		25	50		25	50		25	50	μA

NOTE: SiGe circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

5. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.125 V to -0.965 V.
6. All loading with 50 Ω to V_{CC}-2.0 volts.
7. V_{THR} is the voltage applied to the complementary input, typically V_{BB} or V_{MM}.
8. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

*Typicals used for testing purposes.

Table 6. DC CHARACTERISTICS, INPUT WITH RSPECL OUTPUT V_{CC} = 3.3 V; V_{EE} = 0 V (Note 9)

		-40 °C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Negative Power Supply Current	17	23	29	17	23	29	17	23	29	mA
V_{OH}	Output HIGH Voltage (Note 10)	2250	2330	2375	2325	2365	2400	2350	2390	2425	mV
V_{OUTPP}	Output Voltage Amplitude	350	410	525	350	410	525	350	410	525	mV
V_{IH}	Input HIGH Voltage (Single-Ended) (Note 11)	V_{THR} + 75 mV	V_{CC} - 1.0*	V_{CC}	V_{THR} + 75 mV	V_{CC} - 1.0*	V_{CC}	V_{THR} + 75 mV	V_{CC} - 1.0*	V_{CC}	V
V_{IL}	Input LOW Voltage (Single-Ended) (Note 11)	V_{EE}	V_{CC} - 1.4*	V_{THR} - 75 mV	V_{EE}	V_{CC} - 1.4*	V_{THR} - 75 mV	V_{EE}	V_{CC} - 1.4*	V_{THR} - 75 mV	V
V_{BB}	PECL Output Voltage Reference	1880	1940	2000	1880	1940	2000	1880	1940	2000	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 12) (Differential Configuration)	1.2		3.3	1.2		3.3	1.2		3.3	V
V_{MM}	CMOS Output Voltage Reference $V_{CC}/2$	1500	1650	1800	1500	1650	1800	1500	1650	1800	mV
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
I_{IH}	Input HIGH Current (@ V_{IH})		30	100		30	100		30	100	μA
I_{IL}	Input LOW Current (@ V_{IL})		25	50		25	50		25	50	μA

NOTE: SiGe Circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

9. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925 V to -0.165 V.
10. All loading with 50 Ω to V_{CC} - 2.0 V.
11. V_{THR} is the voltage applied to the complementary input, typically V_{BB} or V_{MM}.
12. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

*Typicals used for testing purposes.

Table 7. DC CHARACTERISTICS, NECL OR RSNECL INPUT WITH NECL OUTPUT

V_{CC} = 0 V; V_{EE} = -3.465 V to -2.375 V (Note 13)

		-40 °C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Negative Power Supply Current	17	23	29	17	23	29	17	23	29	mA
VOH	Output HIGH Voltage (Note 14)	-1050	-970	-925	-975	-935	-900	-950	-910	-875	mV
V_{OUTPP}	Output Voltage Amplitude	350	410	525	350	410	525	350	410	525	mV
V_{IH}	Input HIGH Voltage (Single-Ended) (Note 15)	V_{THR} + 75 mV	V_{CC} - 1.0*	V_{CC}	V_{THR} + 75 mV	V_{CC} - 1.0*	V_{CC}	V_{THR} + 75 mV	V_{CC} - 1.0*	V_{CC}	V
V_{IL}	Input LOW Voltage (Single-Ended) (Note 15)	V_{EE}	V_{CC} - 1.4*	V_{THR} - 75 mV	V_{EE}	V_{CC} - 1.4*	V_{THR} - 75 mV	V_{EE}	V_{CC} - 1.4*	V_{THR} - 75 mV	V
V_{BB}	NECL Output Voltage Reference	-1420	-1360	-1300	-1420	-1360	-1300	-1420	-1360	-1300	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 16) (Differential Configuration)	V_{EE}+1.2		0.0	V_{EE}+1.2		0.0	V_{EE}+1.2		0.0	V
V_{MM}	CMOS Output Voltage Reference (Note 17)	V_{MMT} -150	V_{MMT}	V_{MMT} + 150	V_{MMT} -150	V_{MMT}	V_{MMT} + 150	V_{MMT} -150	V_{MMT}	V_{MMT} + 150	mV
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
I_{IH}	Input HIGH Current (@ V_{IH})		30	100		30	100		30	100	μA
I_{IL}	Input LOW Current (@ V_{IL})		25	50		25	50		25	50	μA

NOTE: SiGe circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

13. Input and output parameters vary 1:1 with V_{CC}.
14. All loading with 50 Ω to V_{CC} -2.0 volts.
15. V_{THR} is the voltage applied to the complementary input, typically V_{BB} or V_{MM}.
16. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.
17. V_{MM} typical = $|V_{CC} - V_{EE}|/2 + V_{EE} = V_{MMT}$

*Typicals used for testing purposes.

Table 8. AC CHARACTERISTICS for FCBGA-16

V_{CC} = 0 V; V_{EE} = -3.465 V to -2.375 V or V_{CC} = 2.375 V to 3.465 V; V_{EE} = 0 V

		-40 °C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Frequency (See Figure 4. F_{max}/JITTER) (Note 18)	10.7	12		10.7	12		10.7	12		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential	90	110	130	100	120	140	105	125	145	ps
t_{SKEW}	Duty Cycle Skew (Note 19)		3	15		3	15		3	15	ps
t_{JITTER}	RMS Random Clock Jitter f_{in} < 10 GHz Peak-to-Peak Data Dependent Jitter f_{in} < 10 Gb/s		0.2 TBD	1		0.2 TBD	1		0.2 TBD	1	ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 20)	75		2600	75		2600	75		2600	mV
t_r t_f	Output Rise/Fall Times @ 1 GHz Q, $\overline{Q}$ (20% - 80%)	30	45	75	20	40	65	20	40	65	ps

18. Measured using a 400 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC} - 2.0 V. Input edge rates 40 ps (20% - 80%).
19. See Figure 6. $t_{skew} = |t_{PLH} - t_{PHL}|$ for a nominal 50% differential clock input waveform.
20. $V_{INPP(max)}$ cannot exceed $V_{CC} - V_{EE}$

Table 9. AC CHARACTERISTICS for QFN-16

V_{CC} = 0 V; V_{EE} = -3.465 V to -2.375 V or V_{CC} = 2.375 V to 3.465 V; V_{EE} = 0 V

		-40 °C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Frequency (See Figure 4. F_{max}/JITTER) (Note 21)	10.7	12		10.7	12		10.7	12		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential	90	110	130	100	120	140	95	125	145	ps
t_{SKEW}	Duty Cycle Skew (Note 22)		3	15		3	15		3	15	ps
t_{JITTER}	RMS Random Clock Jitter f_{in} < 10 GHz Peak-to-Peak Data Dependent Jitter f_{in} < 10 Gb/s		0.2 TBD	2		0.2 TBD	2		0.2 TBD	2	ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 23)	75		2600	75		2600	75		2600	mV
t_r t_f	Output Rise/Fall Times @ 1 GHz Q, $\overline{Q}$ (20% - 80%)	20	30	50	20	30	50	20	30	50	ps

21. Measured using a 400 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC} - 2.0 V. Input edge rates 40 ps (20% - 80%).
22. See Figure 6. $t_{skew} = |t_{PLH} - t_{PHL}|$ for a nominal 50% differential clock input waveform.
23. $V_{INPP(max)}$ cannot exceed $V_{CC} - V_{EE}$

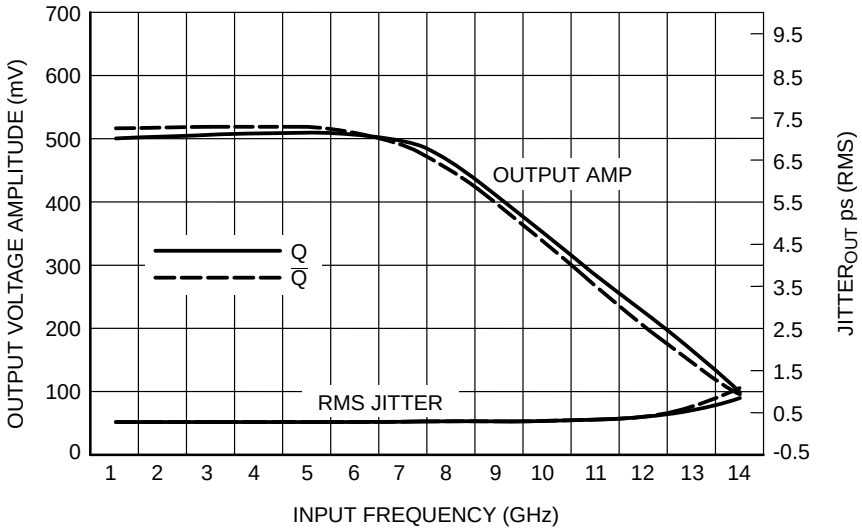
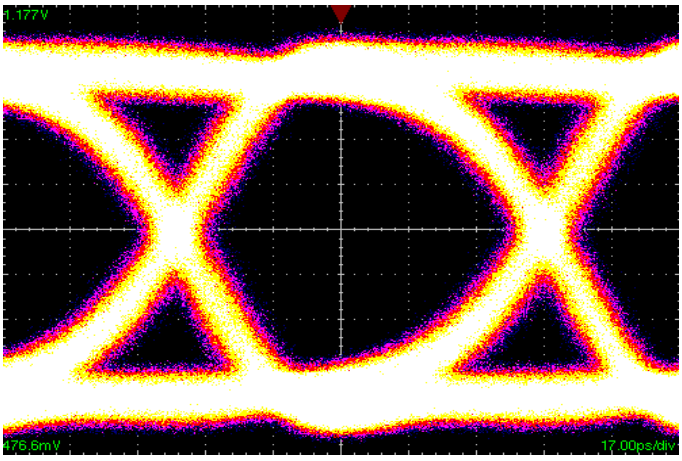


Figure 4. Output Voltage Amplitude (V_{OUTPP}) / RMS Jitter vs. Input Frequency (f_{in}) at Ambient Temperature (Typical)



X = 17ps/Div Y = 70 mV/Div

Figure 5. 10.709 Gb/s Diagram (3.0 V, 25°C)

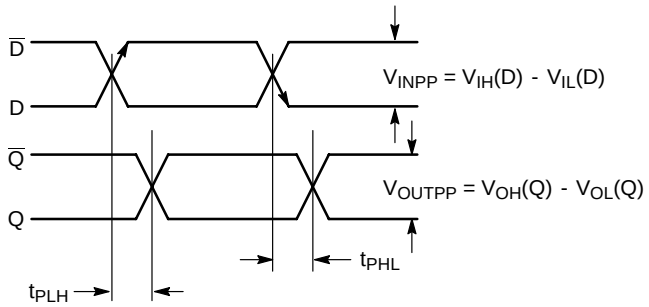
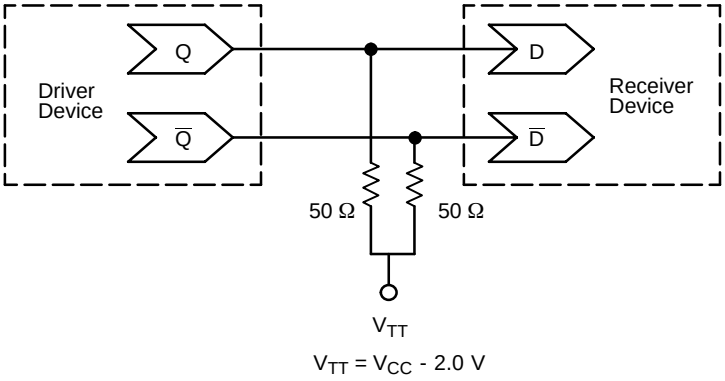


Figure 6. AC Reference Measurement

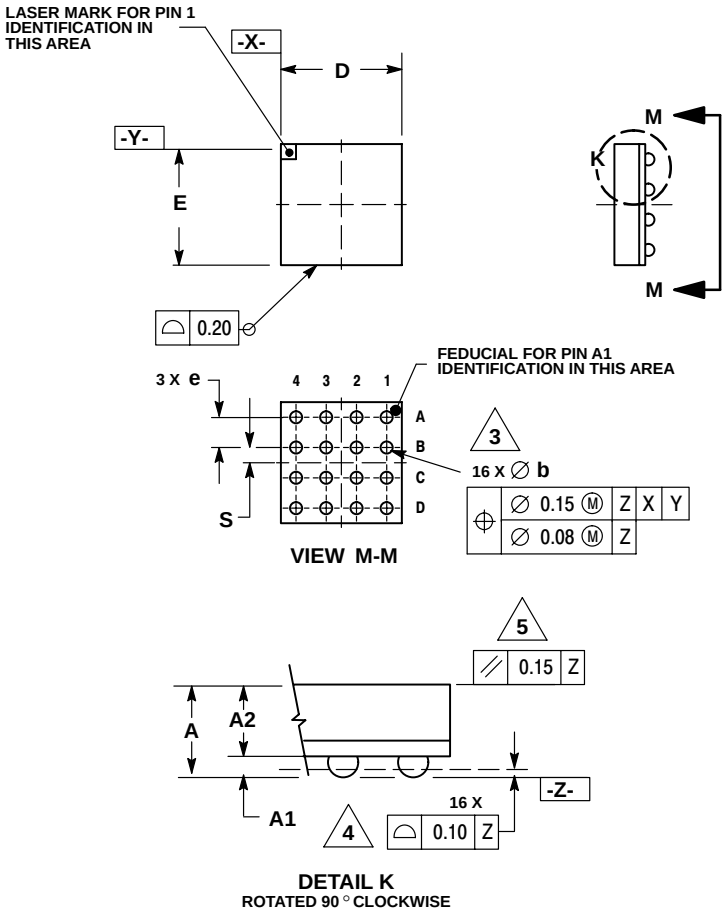


$V_{TT} = V_{CC} - 2.0$ V

Figure 7. Typical Termination for Output Driver and Device Evaluation (Refer to Application Note AND8020 - Termination of ECL Logic Devices)

PACKAGE DIMENSIONS

FCBGA-16
BA SUFFIX
PLASTIC 4 X 4 (mm) BGA FLIP CHIP PACKAGE
CASE 489-01
ISSUE O



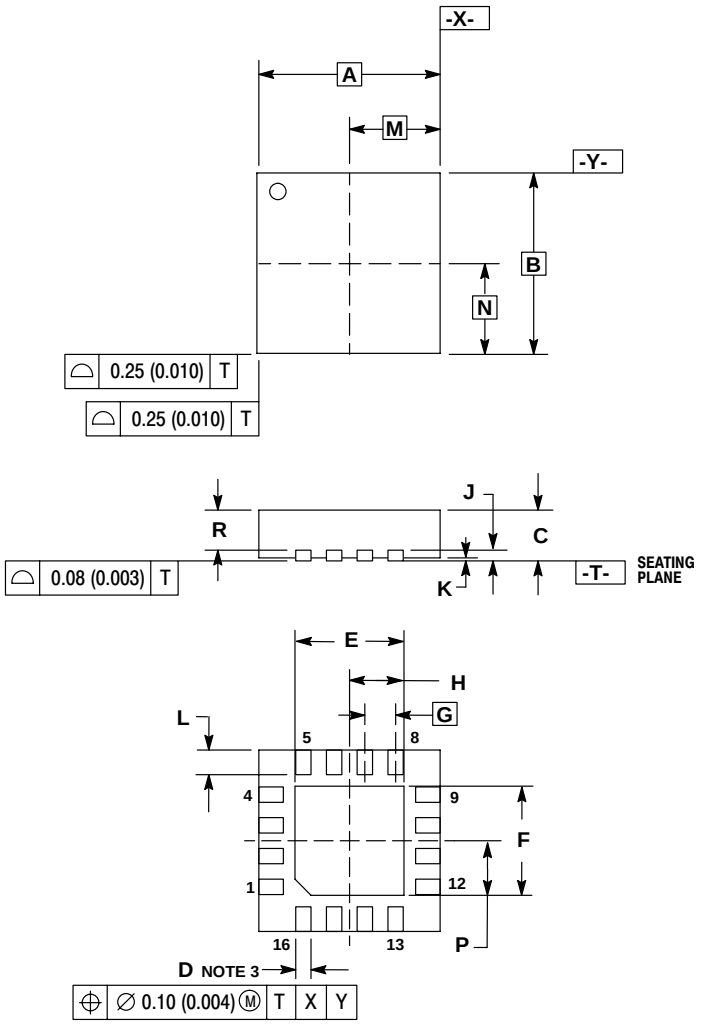
NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

	MILLIMETERS	
DIM	MIN	MAX
A	1.40 MAX	
A1	0.25	0.35
A2	1.20 REF	
b	0.30	0.50
D	4.00 BSC	
E	4.00 BSC	
e	1.00 BSC	
S	0.50 BSC	

NBSG16

PACKAGE DIMENSIONS

16 PIN QFN
MN SUFFIX
CASE 485G-01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	3.00 BSC		0.118 BSC	
B	3.00 BSC		0.118 BSC	
C	0.80	1.00	0.031	0.039
D	0.23	0.28	0.009	0.011
E	1.75	1.85	0.069	0.073
F	1.75	1.85	0.069	0.073
G	0.50 BSC		0.020 BSC	
H	0.875	0.925	0.034	0.036
J	0.20 REF		0.008 REF	
K	0.00	0.05	0.000	0.002
L	0.35	0.45	0.014	0.018
M	1.50 BSC		0.059 BSC	
N	1.50 BSC		0.059 BSC	
P	0.875	0.925	0.034	0.036
R	0.60	0.80	0.024	0.031

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