

U74HCT14

CMOS IC

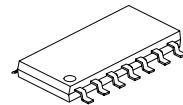
HIGH-SPEED CMOS LOGIC HEX INVERTING SCHMITT TRIGGER

■ DESCRIPTION

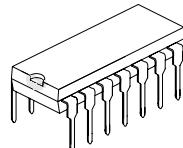
The UTC **74HCT14** each contain six inverting Schmitt triggers in one package. Each of them perform the Boolean function Y=A.

■ FEATURES

- * Widely range of input rise and fall time
- * high noise immunity
- * Fan-out parameters(over temperature range) up to 10 LSTTL Loads
- * Low power consumption
- * Wide range operation 4.5V ~ 5.5V



SOP-14

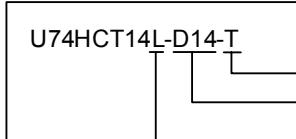


DIP-14

*Pb-free plating product number: 74HCT14L

■ ORDERING INFORMATION

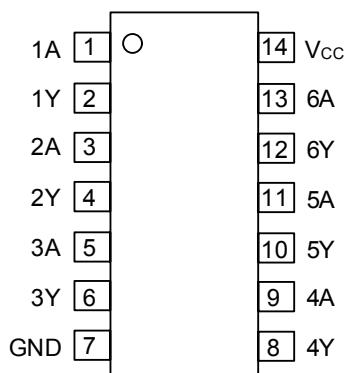
Order Number		Package	Packing
Normal	Lead Free Plating		
U74HCT14-D14-T	U74HCT14L-D14-T	DIP-14	Tube
U74HCT14-S14-R	U74HCT14L-S14-R	SOP-14	Tape Reel
U74HCT14-S14-T	U74HCT14L-S14-T	SOP-14	Tube



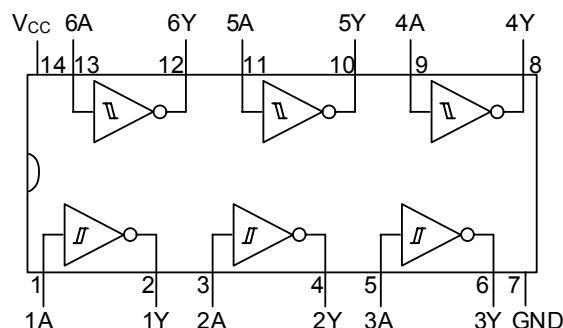
- (1)Packing Type
- (2)Package Type
- (3)Lead Plating

- (1) R: Tape Reel; T: Tube
- (2) D14: DIP-14, S14: SOP-14
- (3) L: Lead Free Plating, Blank: Pb/Sn

■ PIN CONFIGURATION



■ FUNCTIONAL DIAGRAM



■ TRUTH TABLE

INPUT(A)	OUTPUT(Y)
L	H
H	L

H=High level

L=Low Level

■ LOGIC DIAGRAM

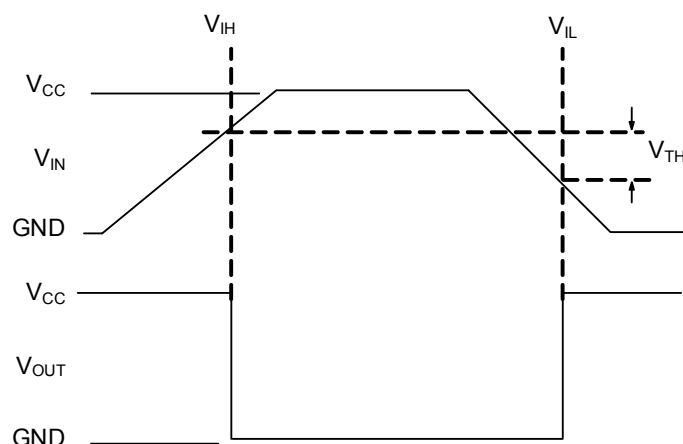
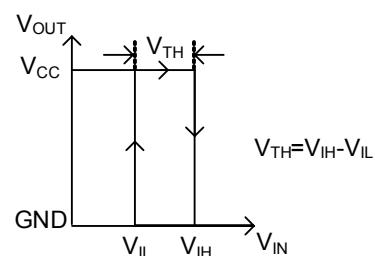
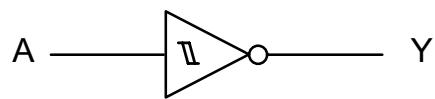


Figure 1. Hysteresis Definition Characteristic And Test Setup

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATINGS	UNIT
DC Supply Voltage		V _{CC}	-0.5V~7V	V
DC Input Clamp Current	For V _{IN} < -0.5V or V _{IN} > V _{CC} + 0.5V	I _{IK}	±20	mA
DC Output Clamp Current	For V _{OUT} < -0.5V or V _{OUT} > V _{CC} + 0.5V	I _{OK}	±20	mA
DC Drain Current, per Output	For -0.5V < V _{OUT} < V _{CC} + 0.5V	I _{OUT}	±25	mA
DC Output Source or Sink Current per Output Pin	For V _{OUT} > -0.5V or V _{OUT} < V _{CC} + 0.5V	I _{OUT}	±25	mA
DC V _{CC} or Ground Current		I _{CC}	±50	mA
Operating Supply Voltage Range		V _{CC}	4.5~5.5	V
Operating DC Input or Output Voltage	V _{IN} , V _{OUT}		0V~V _{CC}	V
Operating Temperature		T _{OPR}	-40 ~ +85	
Storage Temperature		T _{STG}	-65 ~ +150	

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Thermal Resistance Junction Ambient	DIP-14	θ _{JA}	80	/W
	SOP-14		86	

■ ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Switch Points	V _{IH}	V _{CC} =4.5V	1.7		1.79	V
		V _{CC} =5.5V	1.94		1.96	V
	V _{IL}	V _{CC} =4.5V	0.82		0.94	V
		V _{CC} =5.5V	0.96		1.15	V
	V _{TH}	V _{CC} =4.5V	0.8		0.86	V
		V _{CC} =5.5V	0.62		0.83	V
High Level Output Voltage CMOS Loads	V _{OH}	V _{CC} =4.5V, V _{IN} =V _{IH} or V _{IL} , I _{OUT} =-20μA	4.49	4.495	4.498	V
High Level Output Voltage TTL Loads		V _{CC} =4.5V, V _{IN} =V _{IH} or V _{IL} , I _{OUT} =-4mA	3.99	4.00	4.03	V
Low Level Output Voltage CMOS Loads	V _{OL}	V _{CC} =4.5V, V _{IN} =V _{IH} or V _{IL} , I _{OUT} =20μA	0.41	0.66	1.0	mV
Low Level Output Voltage TTL Loads		V _{CC} =4.5V, V _{IN} =V _{IH} or V _{IL} , I _{OUT} =4mA	0.18	0.185	0.19	V
Input Leakage Current	I _{I(LEAK)}	V _{CC} =5.5V, V _{IN} =V _{CC} and GND			<0.1	μA
Quiescent Device Current	I _{CC}	V _{CC} =5.5V, V _{IN} =V _{CC} or GND, I _{OUT} =0mA			<1	μA
Additional Quiescent Device	I _{CC} (Note 1)	V _{CC} =4.5V~5.5V, One input at 2.4V Other inputs at GND or V _{CC}			25	μA
SWITCHING SPECIFICATIONS (Input t _R , t _F = 6ns)						
Propagation Delay, A to Y	t _{PLH} , t _{PHL}	V _{CC} =4.5V, C _L =50pF			30	ns
		V _{CC} =5V, C _L =15pF			2	ns
Output Transition Times	t _{TLH} , t _{THL}	V _{CC} =4.5V, C _L =50pF			12.5	ns
Input Capacitance	C _{IN}				10	pF
Power Dissipation Capacitance (Note 2,3)	C _{PD}	V _{CC} =5V			20	pF

Note: 1. This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

2. C_{PD} is used to determine the dynamic power consumption, per inverter.

3. P_D = V_{CC}² f_i (C_{PD} + C_L) where f_i = input frequency, C_L = output load capacitance, V_{CC} = supply voltage.

■ TEST WAVEFORM

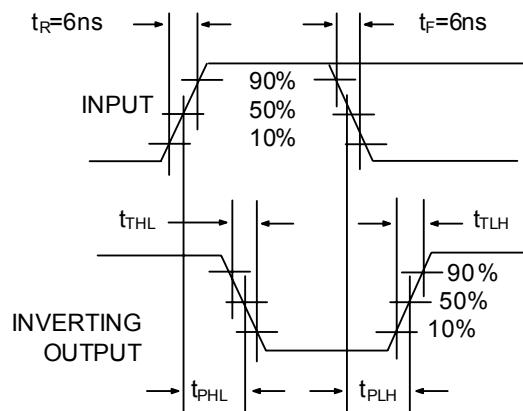


Figure 2. 74HCT14 Transition Times And Propagation Delay Times, Combination Logic

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