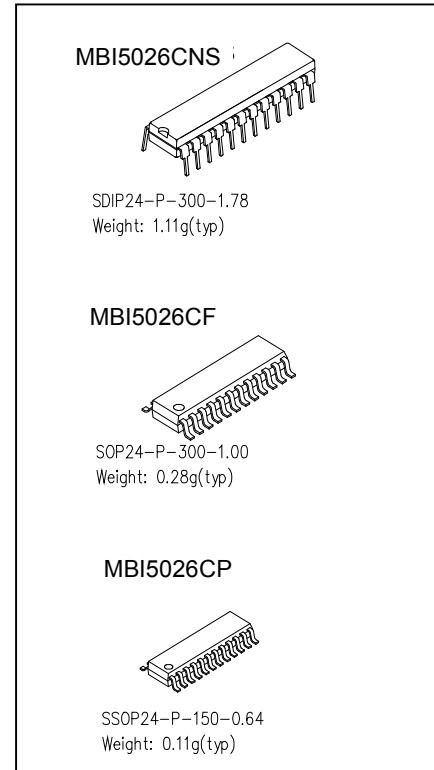




# 16-bit Constant Current LED Sink Driver

## Features

- 16 constant-current output channels
- Constant output current invariant to load voltage change
- Excellent output current accuracy:  
between channels:  $\pm 3\%$  (max.), and  
between ICs:  $\pm 6\%$  (max.)
- Output current adjusted through an external resistor
- Constant output current range: 5-90 mA
- Fast response of output current,  $\overline{OE}$  (min.): 200 ns
- 25MHz clock frequency
- Schmitt trigger input
- 5V supply voltage



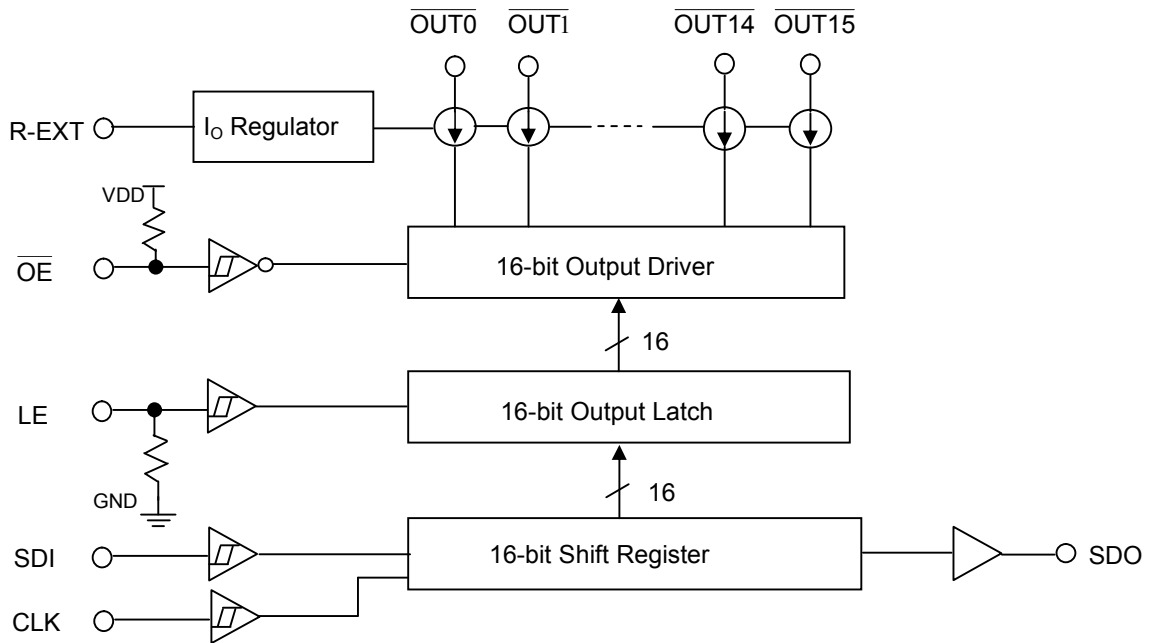
Current Accuracy		Conditions
Between Channels	Between ICs	
< $\pm 3\%$	< $\pm 6\%$	$I_{OUT} = 10 \text{ mA} \sim 60 \text{ mA}$

## Product Description

MBI5026 is designed for LED displays. As an enhancement of its predecessor, MBI5016, MBI5026 exploits PrecisionDrive™ technology to enhance its output characteristics. MBI5026 contains a serial buffer and data latches which convert serial input data into parallel output format. At MBI5026 output stage, sixteen regulated current ports are designed to provide uniform and constant current sinks for driving LEDs within a large range of Vf variations.

MBI5026 provides users with great flexibility and device performance while using MBI5026 in their system design for LED display applications, e.g. LED panels. Users may adjust the output current from 5 mA to 90 mA through an external resistor,  $R_{ext}$ , which gives users flexibility in controlling the light intensity of LEDs. MBI5026 guarantees to endure maximum 17V at the output port. The high clock frequency, 25 MHz, also satisfies the system requirements of high volume data transmission.

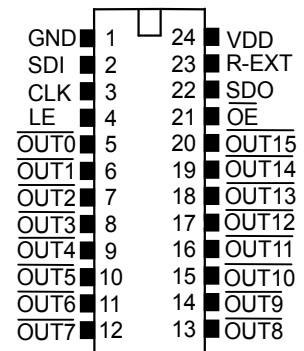
**Block Diagram**



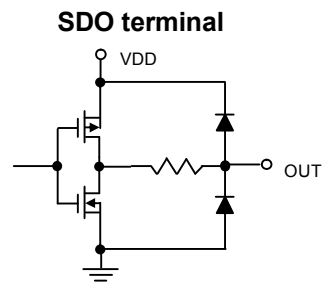
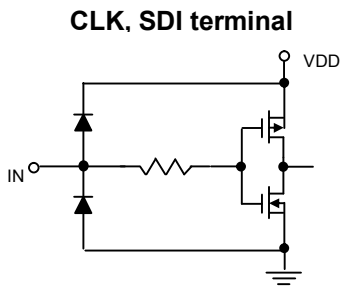
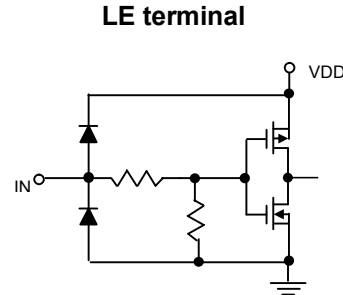
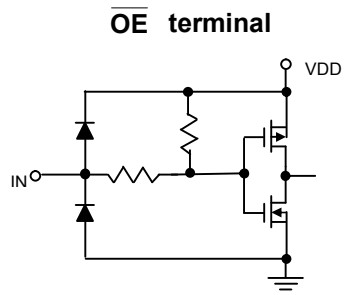
**Terminal Description**

Pin No.	Pin Name	Function
1	GND	Ground terminal for control logic and current sink
2	SDI	Serial-data input to the shift register
3	CLK	Clock input terminal for data shift on rising edge
4	LE	Data strobe input terminal Serial data is transferred to the output latch when LE is high. The data is latched when LE goes low.
5~20	$\overline{\text{OUT0}} \sim \overline{\text{OUT15}}$	Constant current output terminals
21	$\overline{\text{OE}}$	Output enable terminal When (active) low, the output drivers are enabled; when high, all output drivers are turned OFF (blanked).
22	SDO	Serial-data output to the following SDI of next driver IC
23	R-EXT	Input terminal used to connect an external resistor for setting up output current for all output channels
24	VDD	5V supply voltage terminal

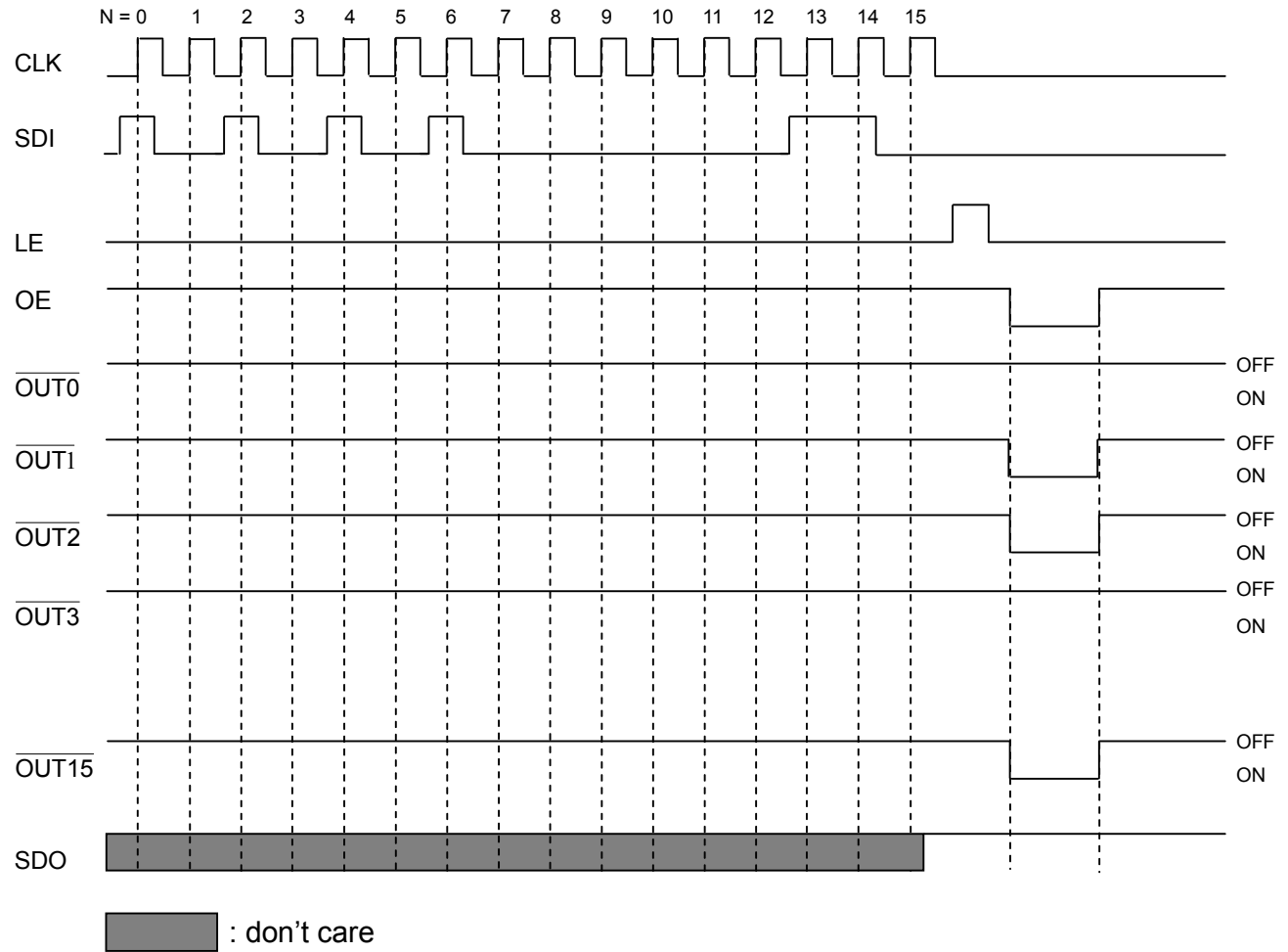
**Pin Configuration**



**Equivalent Circuits of Inputs and Outputs**



**Timing Diagram**



**Truth Table**

CLK	LE	$\overline{\text{OE}}$	SDI	$\overline{\text{OUT0}} \dots \overline{\text{OUT7}} \dots \overline{\text{OUT15}}$	SDO
	H	L	$D_n$	$\overline{D_{n+2}} \dots \overline{D_{n-7}} \dots \overline{D_{n-15}}$	$D_{n-15}$
	L	L	$D_{n+1}$	No Change	$D_{n-14}$
	H	L	$D_{n+2}$	$\overline{D_{n+2}} \dots \overline{D_{n-5}} \dots \overline{D_{n-13}}$	$D_{n-13}$
	X	L	$D_{n+3}$	$\overline{D_{n+2}} \dots \overline{D_{n-5}} \dots \overline{D_{n-13}}$	$D_{n-13}$
	X	H	$D_{n+3}$	Off	$D_{n-13}$

**Maximum Ratings**

Characteristic		Symbol	Rating	Unit
Supply Voltage		$V_{DD}$	0~7.0	V
Input Voltage		$V_{IN}$	-0.4~ $V_{DD} + 0.4$	V
Output Current		$I_{OUT}$	+90	mA
Output Voltage		$V_{DS}$	-0.5~+20.0	V
Clock Frequency		$F_{CLK}$	25	MHz
GND Terminal Current		$I_{GND}$	1440	mA
Power Dissipation (On PCB, $T_a=25^{\circ}C$ )	CNS – type	$P_D$	1.52	W
	CF – type		1.30	
	CP – type		1.11	
Thermal Resistance (On PCB, $T_a=25^{\circ}C$ )	CNS – type	$R_{th(j-a)}$	82	$^{\circ}C/W$
	CF – type		96	
	CP – type		112	
Operating Temperature		$T_{opr}$	-40~+85	$^{\circ}C$
Storage Temperature		$T_{stg}$	-55~+150	$^{\circ}C$

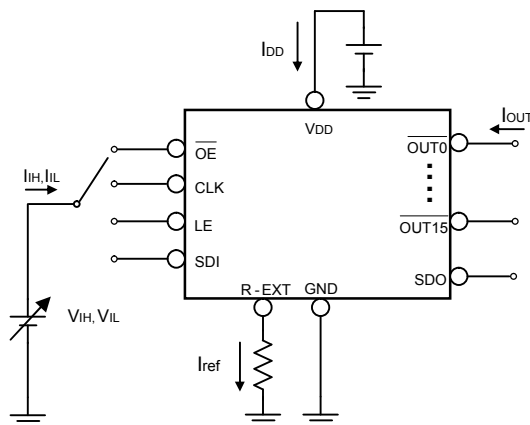
**Recommended Operating Conditions**

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	$V_{DD}$	-	4.5	5.0	5.5	V
Output Voltage	$V_{DS}$	$\overline{OUT0} \sim \overline{OUT15}$	-	-	17.0	V
Output Current	$I_{OUT}$	DC Test Circuit	5	-	60	mA
	$I_{OH}$	SDO	-	-	-1.0	mA
	$I_{OL}$	SDO	-	-	1.0	mA
Input Voltage	$V_{IH}$	CLK, $\overline{OE}$ , LE and SDI	$0.8V_{DD}$	-	$V_{DD}+0.3$	V
	$V_{IL}$	CLK, $\overline{OE}$ , LE and SDI	-0.3	-	$0.3V_{DD}$	V
LE Pulse Width	$t_{w(L)}$	$V_{DD}=4.5\sim 5.5V$	40	-	-	ns
CLK Pulse Width	$t_{w(CLK)}$		20	-	-	ns
$\overline{OE}$ Pulse Width	$t_{w(OE)}$		200	-	-	ns
Setup Time for SDI	$t_{su(D)}$		5	-	-	ns
Hold Time for SDI	$t_{h(D)}$		10	-	-	ns
Setup Time for LE	$t_{su(L)}$		15	-	-	ns
Hold Time for LE	$t_{h(L)}$		15	-	-	ns
Clock Frequency	$F_{CLK}$	Cascade Operation	-	-	25.0	MHz
Power Dissipation	$P_D$	Ta=85°C (CNS type)	-	-	0.79	W
		Ta=85°C (CF type)	-	-	0.67	
		Ta=85°C (CP type)	-	-	0.57	

**Electrical Characteristics**

Characteristic		Symbol	Condition		Min.	Typ.	Max.	Unit
Input Voltage	“H” level	$V_{IH}$	$T_a = -40\sim 85^{\circ}\text{C}$		$0.8V_{DD}$	-	$V_{DD}$	V
	“L” level	$V_{IL}$	$T_a = -40\sim 85^{\circ}\text{C}$		GND	-	$0.3V_{DD}$	V
Output Leakage Current		$I_{OH}$	$V_{OH}=17.0\text{V}$		-	-	0.5	$\mu\text{A}$
Output Voltage	SDO	$V_{OL}$	$I_{OL}=+1.0\text{mA}$		-	-	0.4	V
		$V_{OH}$	$I_{OH}=-1.0\text{mA}$		4.6	-	-	V
Output Current 1		$I_{OUT1}$	$V_{DS}=0.6\text{V}$	$R_{ext}=720\ \Omega$	-	25.0	-	mA
Current Skew		$dI_{OUT1}$	$I_{OL}=25\text{mA}$ $V_{DS}=0.6\text{V}$	$R_{ext}=720\ \Omega$	-	$\pm 1$	$\pm 3$	%
Output Current 2		$I_{OUT2}$	$V_{DS}=0.8\text{V}$	$R_{ext}=360\ \Omega$	-	50.0	-	mA
Current Skew		$dI_{OUT2}$	$I_{OL}=50\text{mA}$ $V_{DS}=0.8\text{V}$	$R_{ext}=360\ \Omega$	-	$\pm 1$	$\pm 3$	%
Output Current vs. Output Voltage Regulation		$\%/dV_{DS}$	$V_{DS}$ within 1.0V and 3.0V		-	$\pm 0.1$	-	% / V
Output Current vs. Supply Voltage Regulation		$\%/dV_{DD}$	$V_{DD}$ within 4.5V and 5.5V		-	$\pm 1$	-	% / V
Pull-up Resistor		$R_{IN(up)}$	$\overline{\text{OE}}$		250	500	800	K $\Omega$
Pull-down Resistor		$R_{IN(down)}$	LE		250	500	800	K $\Omega$
Supply Current	“OFF”	$I_{DD(off) 1}$	$R_{ext}=\text{Open}, \overline{\text{OUT0}} \sim \overline{\text{OUT15}} =\text{Off}$		-	9	-	mA
		$I_{DD(off) 2}$	$R_{ext}=720\ \Omega, \overline{\text{OUT0}} \sim \overline{\text{OUT15}} =\text{Off}$		-	10	-	
		$I_{DD(off) 3}$	$R_{ext}=360\ \Omega, \overline{\text{OUT0}} \sim \overline{\text{OUT15}} =\text{Off}$		-	11	-	
	“ON”	$I_{DD(on) 1}$	$R_{ext}=720\ \Omega, \overline{\text{OUT0}} \sim \overline{\text{OUT15}} =\text{On}$		-	10	-	
		$I_{DD(on) 2}$	$R_{ext}=360\ \Omega, \overline{\text{OUT0}} \sim \overline{\text{OUT15}} =\text{On}$		-	11	-	

**Test Circuit for Electrical Characteristics**

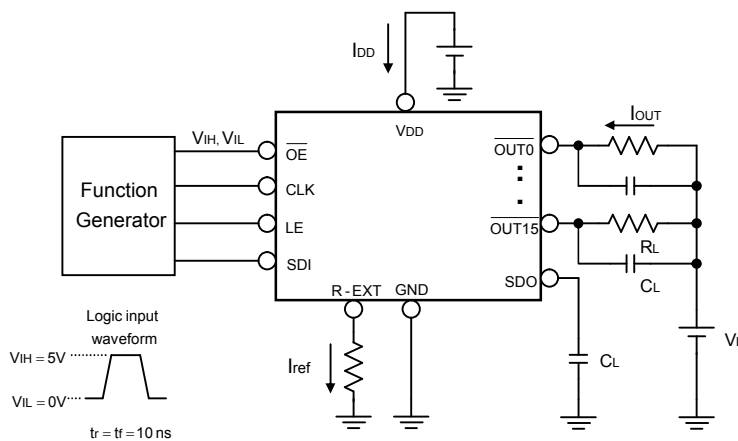


**Switching Characteristics**

Characteristic		Symbol	Condition	Min.	Typ.	Max.	Unit
Propagation Delay Time ("L" to "H")	CLK - $\overline{\text{OUT}}_n$	$t_{pLH1}$	$V_{DD}=5.0\text{ V}$ $V_{DS}=0.8\text{ V}$ $V_{IH}=V_{DD}$ $V_{IL}=GND$ $R_{ext}=300\ \Omega$ $V_L=4.0\text{ V}$ $R_L=52\ \Omega$ $C_L=10\text{ pF}$	-	50	100	ns
	LE - $\overline{\text{OUT}}_n$	$t_{pLH2}$		-	50	100	ns
	$\overline{\text{OE}}$ - $\overline{\text{OUT}}_n$	$t_{pLH3}$		-	20	100	ns
	CLK - SDO	$t_{pLH}$		15	20	-	ns
Propagation Delay Time ("H" to "L")	CLK - $\overline{\text{OUT}}_n$	$t_{pHL1}$		-	100	150	ns
	LE - $\overline{\text{OUT}}_n$	$t_{pHL2}$		-	100	150	ns
	$\overline{\text{OE}}$ - $\overline{\text{OUT}}_n$	$t_{pHL3}$		-	50	150	ns
	CLK - SDO	$t_{pHL}$		15	20	-	ns
Pulse Width	CLK	$t_{w(\text{CLK})}$		20	-	-	ns
	LE	$t_{w(L)}$		20	-	-	ns
	$\overline{\text{OE}}$	$t_{w(\text{OE})}$		200	-	-	ns
Hold Time for LE		$t_{h(L)}$		5	-	-	ns
Setup Time for LE		$t_{su(L)}$		5	-	-	ns
Maximum CLK Rise Time		$t_r^{**}$		-	-	500	ns
Maximum CLK Fall Time		$t_f^{**}$		-	-	500	ns
Output Rise Time of Iout		$t_{or}$		-	70	200	ns
Output Fall Time of Iout		$t_{of}$	-	40	120	ns	

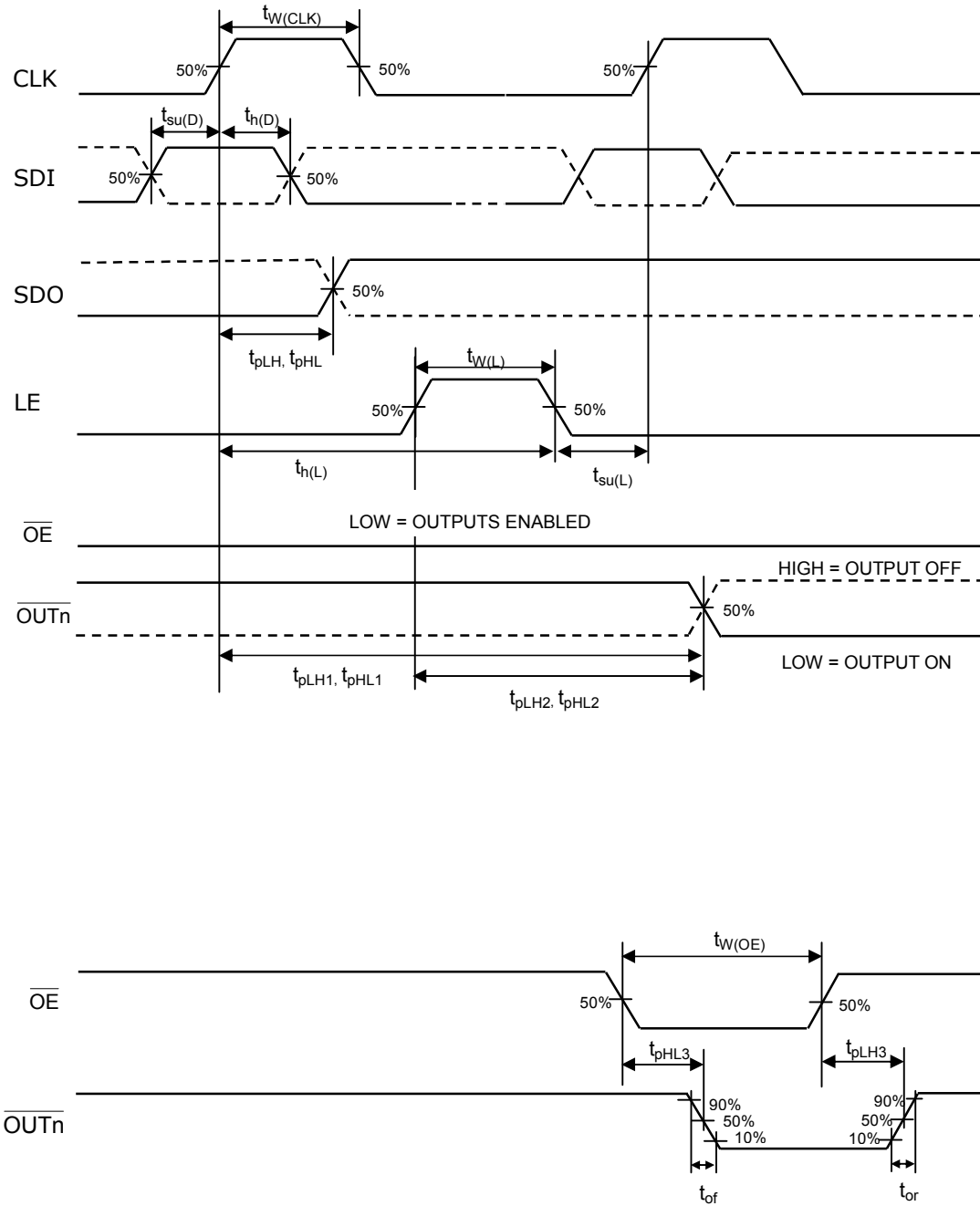
※If the devices are connected in cascade and  $t_r$  or  $t_f$  is large, it may be critical to achieve the timing required for data transfer between two cascaded devices.

**Test Circuit for Switching Characteristics**





**Timing Waveform**

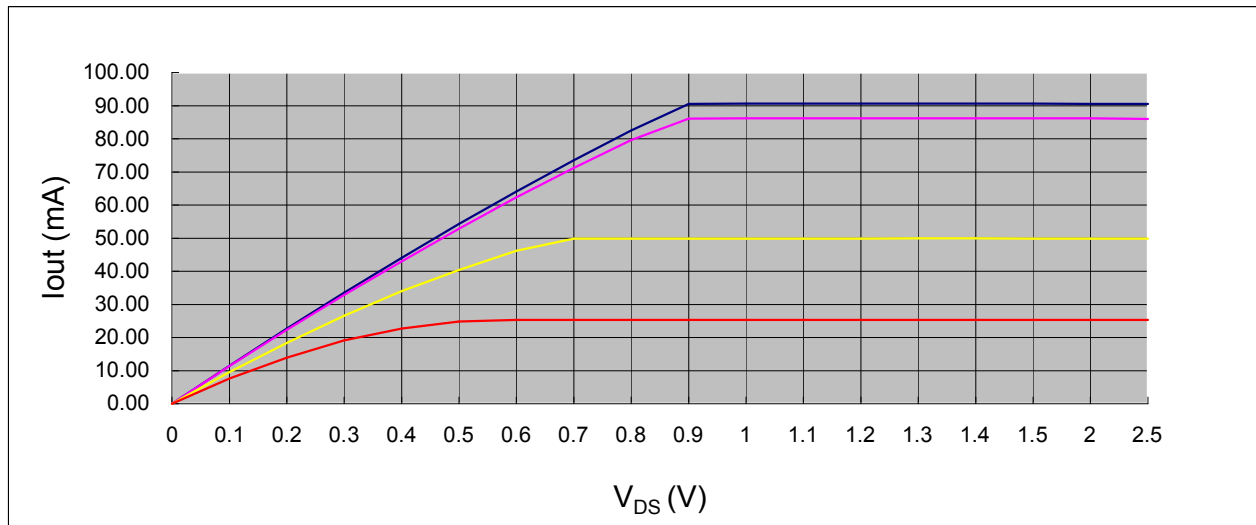


**Application Information**

**Constant Current**

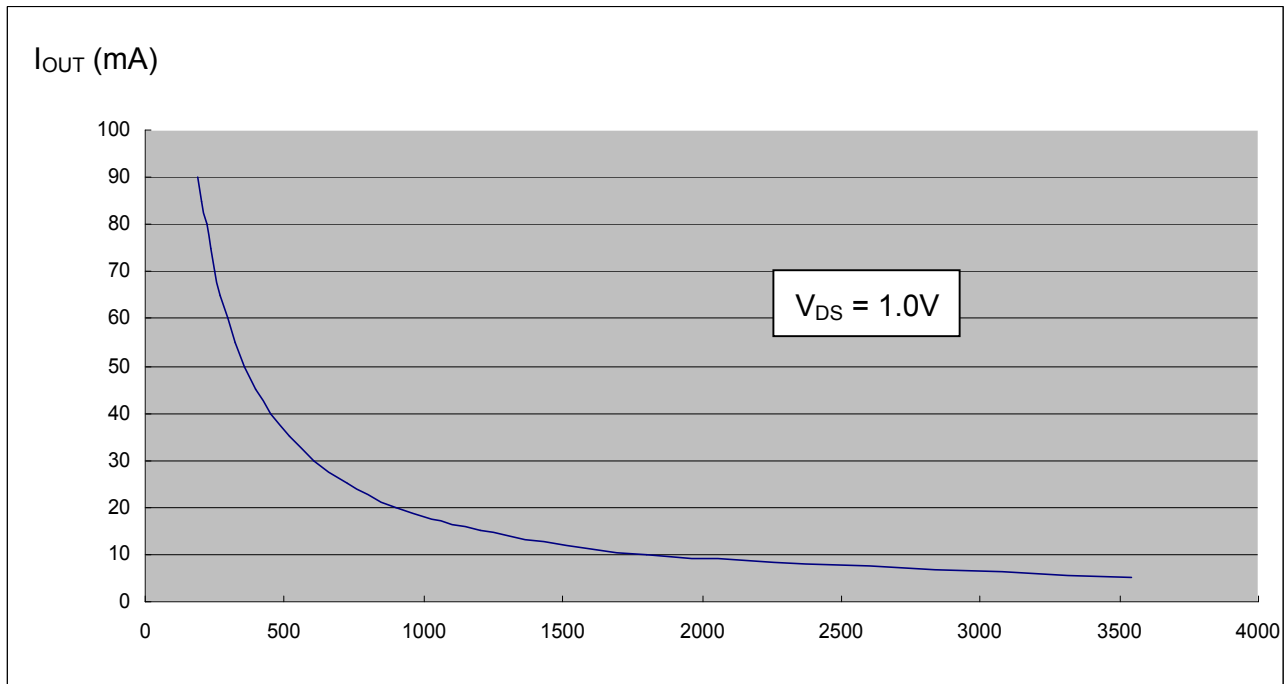
To design LED displays, MBI5026 provides nearly no variations in current from channel to channel and from IC to IC. This can be achieved by:

- 1) The maximum current variation between channels is less than  $\pm 3\%$ , and that between ICs is less than  $\pm 6\%$ .
- 2) In addition, the current characteristic of output stage is flat and users can refer to the figure as shown below. The output current can be kept constant regardless of the variations of LED forward voltages ( $V_f$ ). This performs as a perfection of load regulation.



**Adjusting Output Current**

The output current of each channel ( $I_{OUT}$ ) is set by an external resistor,  $R_{ext}$ . The relationship between  $I_{out}$  and  $R_{ext}$  is shown in the following figure.



**Resistance of the external resistor,  $R_{ext}$ , in  $\Omega$**

Also, the output current in milliamps can be calculated from the equation:

$I_{OUT}$  is  $(625 / R_{ext}) \times 28.8$ , approximately,

where  $R_{ext}$ , in  $\Omega$ , is the resistance of the external resistor connected to R-EXT terminal.

The magnitude of current (as a function of  $R_{ext}$ ) is around 50mA at 360 $\Omega$  and 25mA at 720 $\Omega$ .

**Package Power Dissipation (P<sub>D</sub>)**

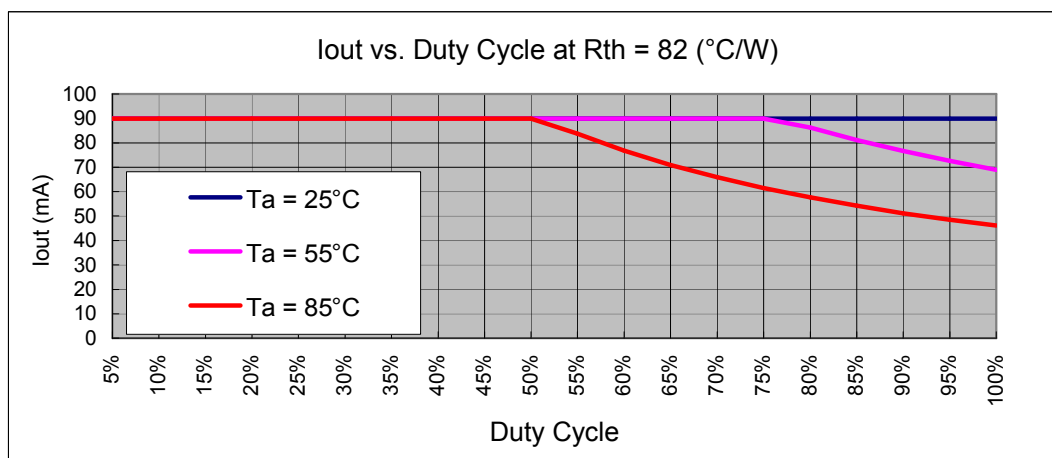
The maximum allowable package power dissipation is determined as  $P_{D(max)} = (T_j - T_a) / R_{th(j-a)}$ . When 16 output channels are turned on simultaneously, the actual package power dissipation is  $P_{D(act)} = (I_{DD} \times V_{DD}) + (I_{OUT} \times Duty \times V_{DS} \times 16)$ . Therefore, to keep  $P_{D(act)} \leq P_{D(max)}$ , the allowable maximum output current as a function of duty cycle is:

$$I_{OUT} = \{ [ (T_j - T_a) / R_{th(j-a)} ] - (I_{DD} \times V_{DD}) \} / V_{DS} / Duty / 16,$$

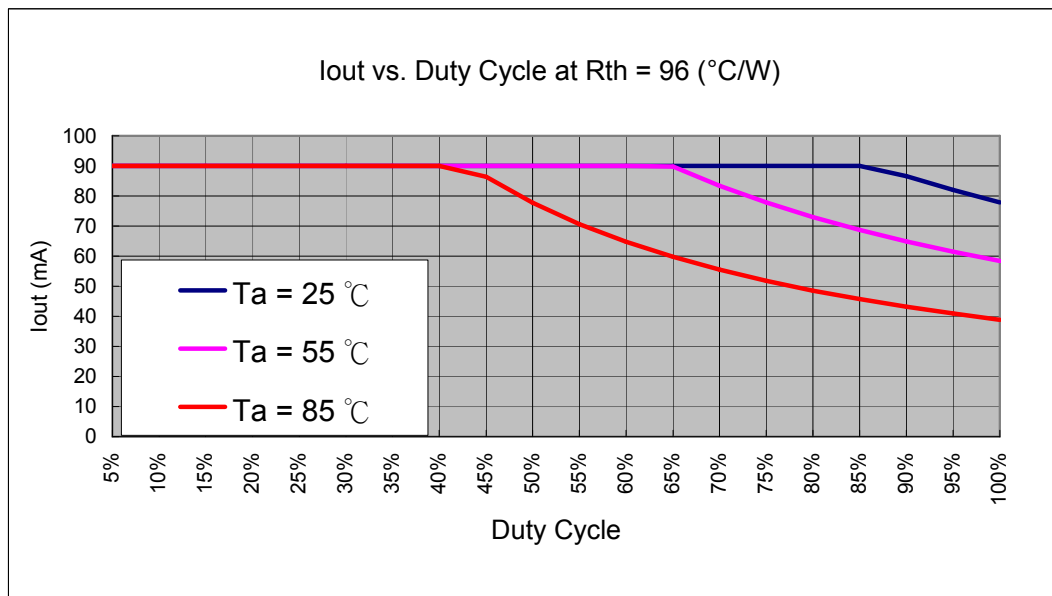
where  $T_j = 150^\circ\text{C}$ .

**(A) I<sub>out</sub> = 90mA, V<sub>DS</sub> = 1.0V, 16 output channels active**

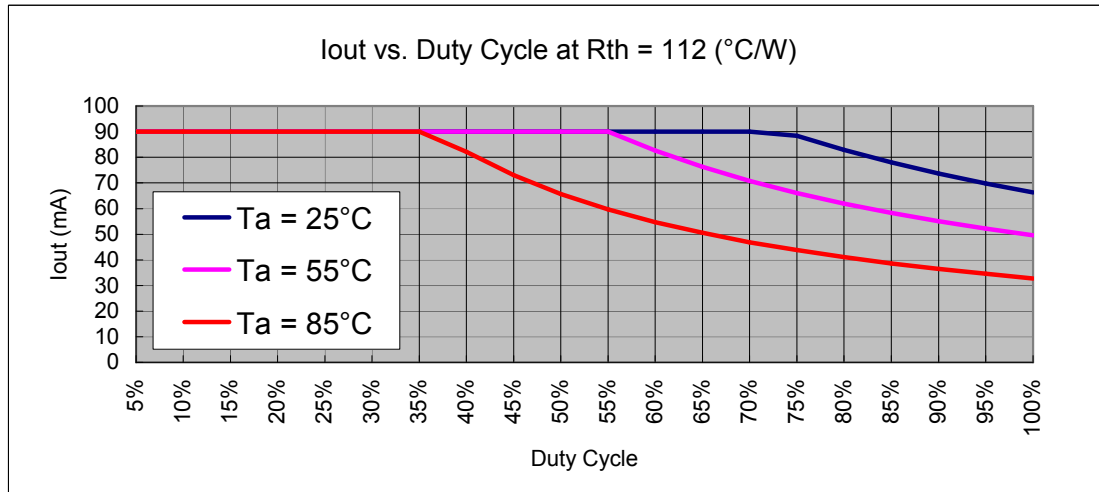
For CNS type package, the thermal resistance is  $R_{th(j-a)} = 82 (\text{°C/W})$



For CF type package, the thermal resistance is  $R_{th(j-a)} = 96 (\text{°C/W})$

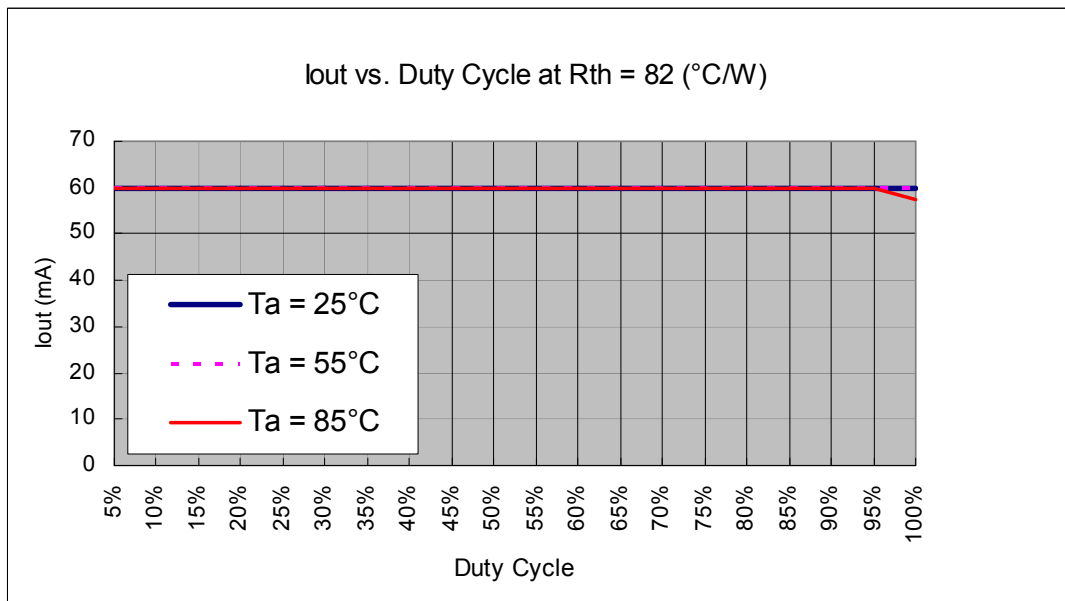


For CP type package, the thermal resistance is  $R_{th(j-a)} = 112 \text{ (}^\circ\text{C/W)}$

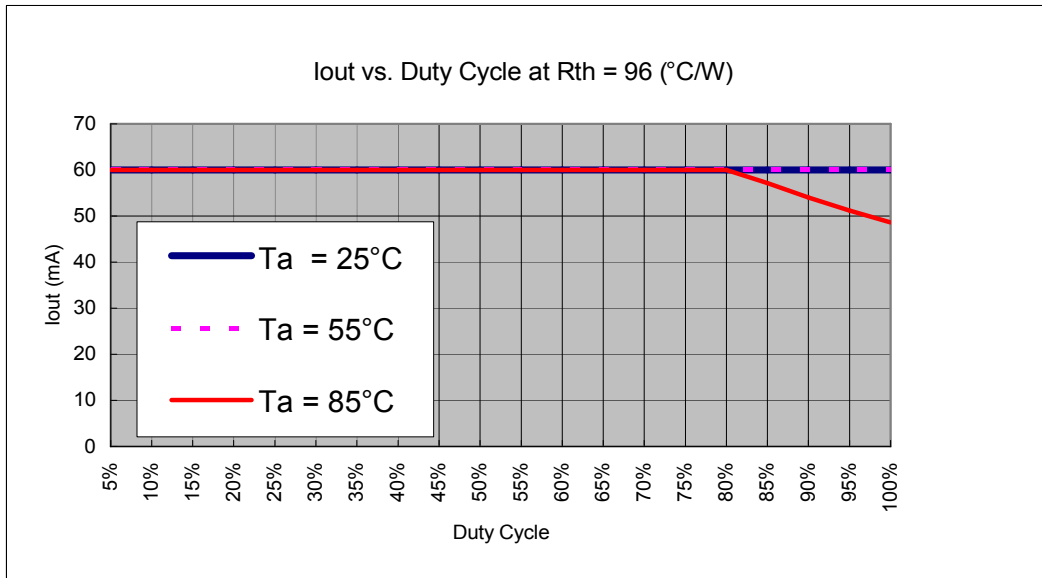


**(B) I<sub>out</sub> = 60mA, V<sub>DS</sub> = 0.8V, 16 output channels active**

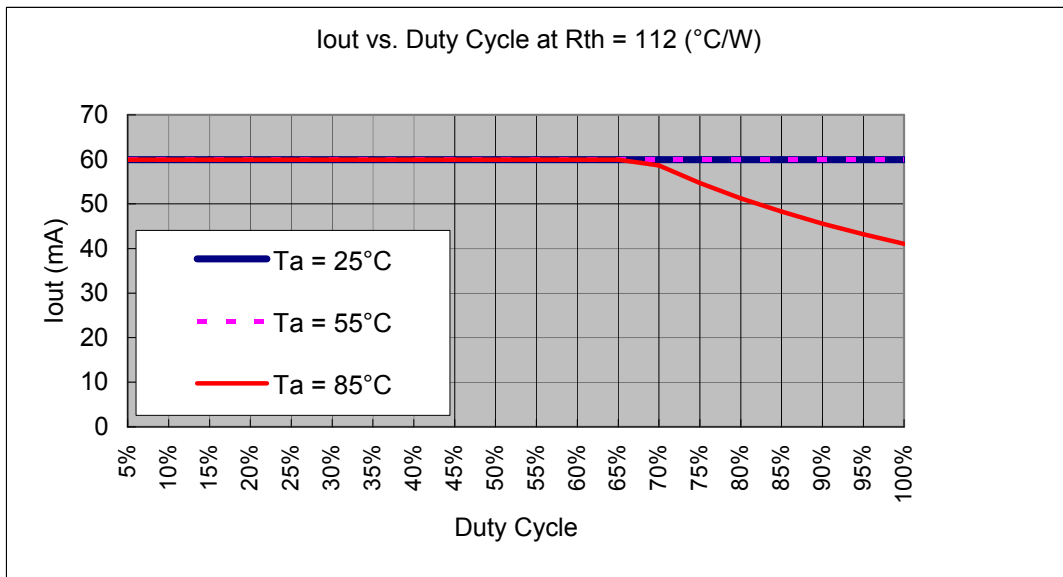
For CNS type package, the thermal resistance is  $R_{th(j-a)} = 82 \text{ (}^\circ\text{C/W)}$



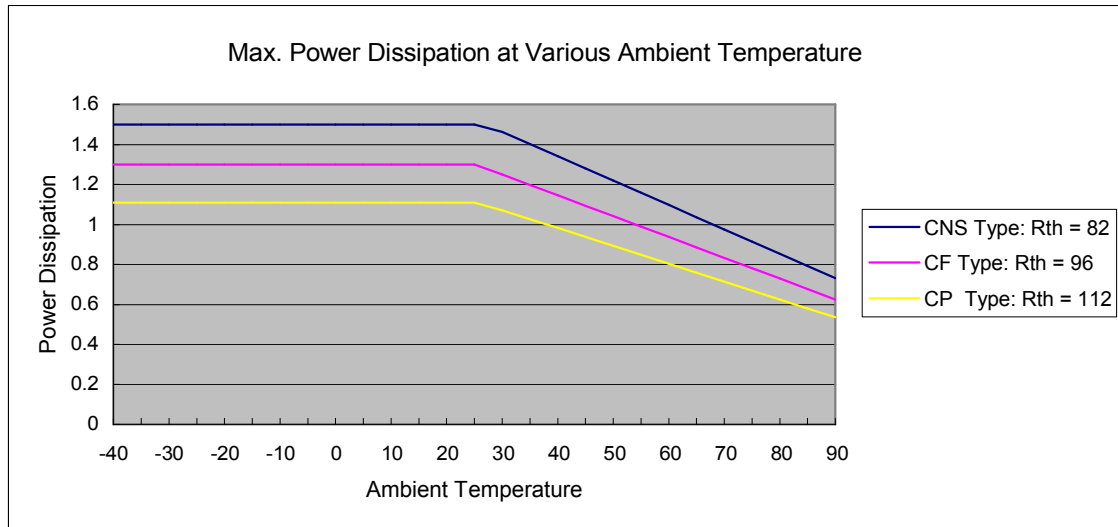
For CF type package, the thermal resistance is  $R_{th(j-a)} = 96 \text{ (}^\circ\text{C/W)}$



For CP type package, the thermal resistance is  $R_{th(j-a)} = 112 \text{ (}^\circ\text{C/W)}$



The maximum power dissipation,  $P_D(\max) = (T_j - T_a) / R_{th(j-a)}$ , decreases as the ambient temperature increases.

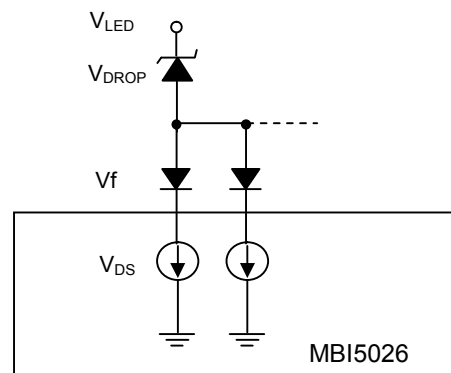
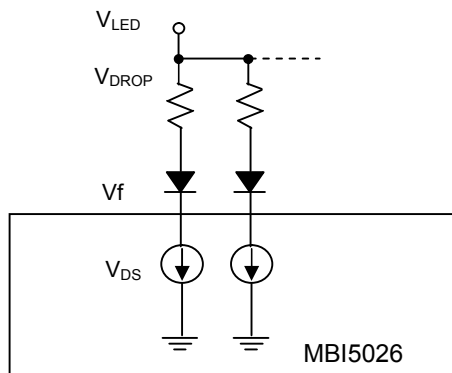


**Load Supply Voltage ( $V_{LED}$ )**

MBI5026 are designed to operate with  $V_{DS}$  ranging from 0.4V to 1.0V considering the package power dissipating limits.  $V_{DS}$  may be higher enough to make  $P_{D(act)} > P_{D(max)}$  when  $V_{LED} = 5V$  and  $V_{DS} = V_{LED} - V_f$ , in which  $V_{LED}$  is the load supply voltage. In this case, it is recommended to use the lowest possible supply voltage or to set an external voltage reducer,  $V_{DROP}$ .

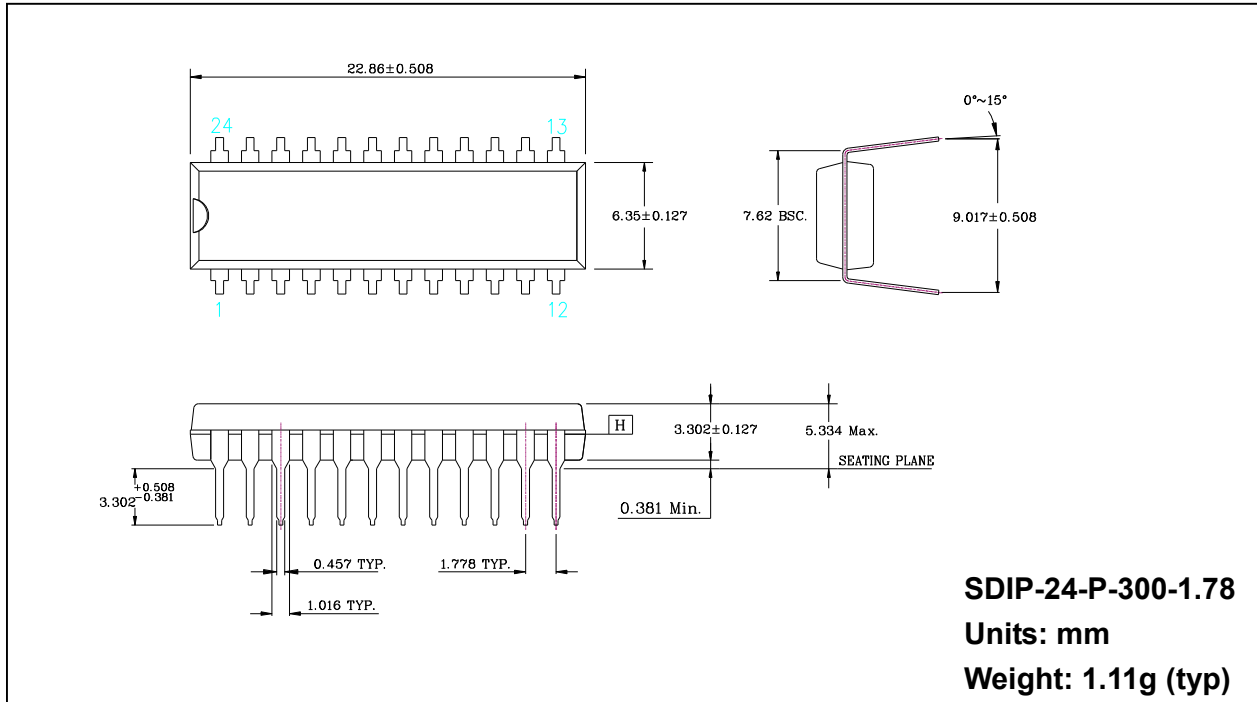
A voltage reducer lets  $V_{DS} = (V_{LED} - V_f) - V_{DROP}$ .

Resistors or Zener diode can be used in the applications as shown in the following figures.

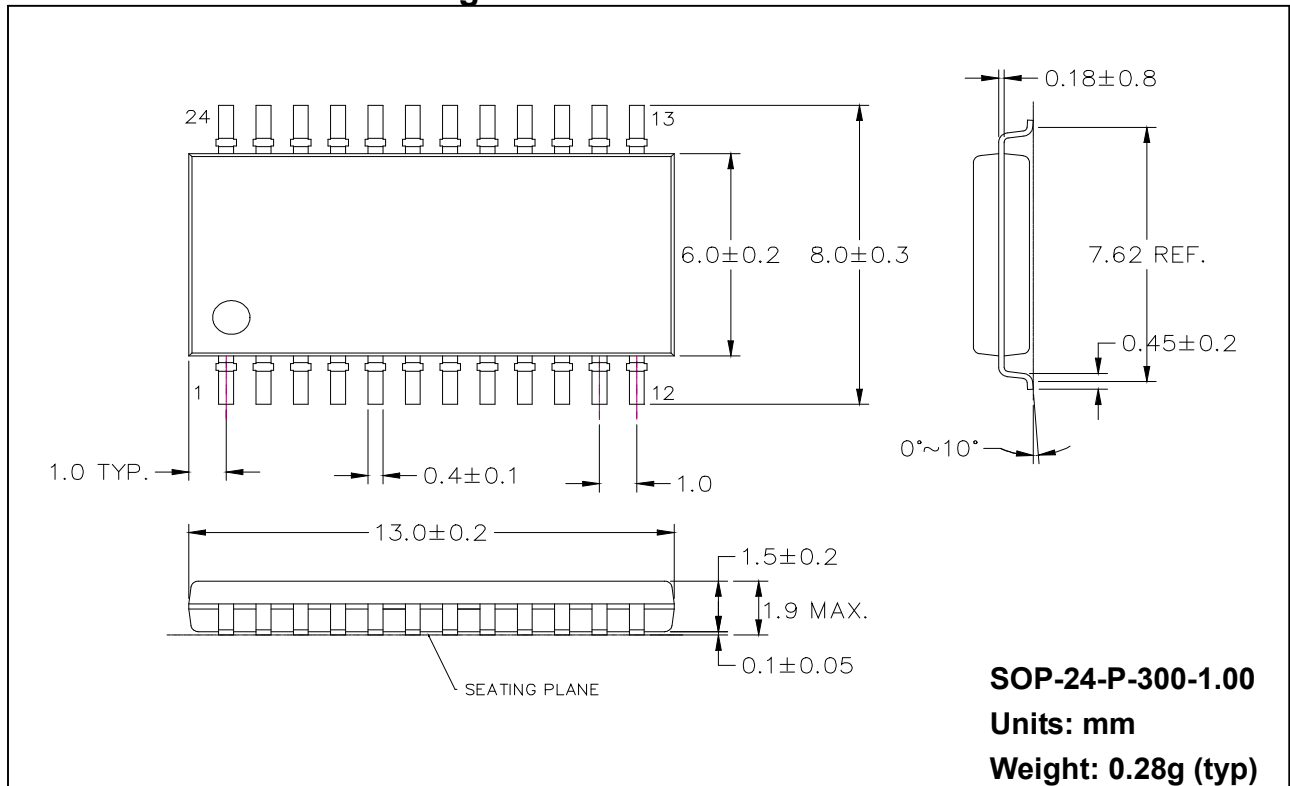


**Package Outlines**

**MBI5026CNS Outline Drawing**



**MBI5026CF Outline Drawing**





MBI5026CP Outline Drawing

