MP75L24

Low Voltage CMOS Buffered Multiplying 8-Bit Digital-to-Analog Converter

March 1998-3

FEATURES

- 3.3 V Operation
- I_{OUT} Pin Voltages are User Definable
- Improved Isolation of Analog from Digital Ground
- Full Four-Quadrant Multiplication
- On-chip Bus Interface Logic
- Low Power Consumption
- Monotonicity Guaranteed (Full Temperature Range)
- Use in Unipolar Supplies
- Extremely Low Power CMOS

APPLICATIONS

- Microprocessor Controlled Gain Circuits
- Microprocessor Controlled Attenuator Circuits
- Microprocessor Controlled Function Generation
- Precision AGC Circuits
- Bus Structured Instruments
- Disk Drives

GENERAL DESCRIPTION

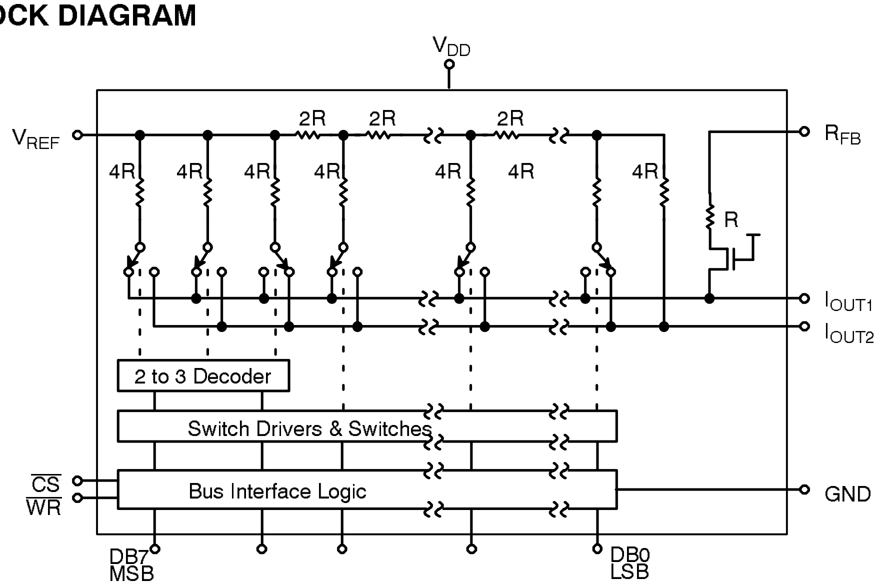
The MP75L24 is a low cost, 8-bit CMOS Digital-to-Analog Converter designed for direct interface to most microprocessors.

The MP75L24 is pin-to-pin compatible to the MP7524A. In addition, the $I_{OUT1,\,2}$ pins may be taken to a non-ground voltage. This allows its use in single supply circuits.

Basically an 8-bit DAC with input latches, the MP75L24's load cycle is similar to the "write" cycle of a random access memory. Using an advanced thin-film on CMOS fabrication process, the MP75L24 provides accuracy to 1 LSB with power dissipation of only 0.3 mW.

Featuring operation from +3.0 V to +3.6 V, the MP75L24 interfaces directly to most microprocessor buses or output ports. Excellent multiplying characteristics (2- or 4-quadrant) make the MP75L24 an ideal choice for many microprocessor controlled gain setting and signal control applications.

SIMPLIFIED BLOCK DIAGRAM



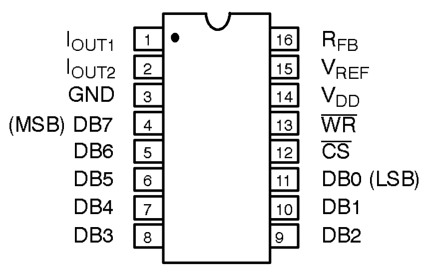
3 Segment D/A Converter with Termination to GND
Logical "1" at Digital Input Steers Current to IOUT1

ORDERING INFORMATION

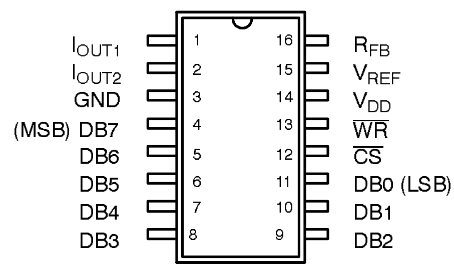
Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (LSB)
Plastic Dip	−40 to +85°C	MP75L24AN	±1	±1	±3
SOIC	−40 to +85°C	MP75L24AR	±1	±1	±3

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



16 Pin PDIP (0.300”)



16 Pin SOIC (Jedec, 0.150”)

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	I_{OUT1}	Current Output 1
2	I_{OUT2}	Current Output 2
3	GND	Ground
4	DB7	Data Input Bit 7 (MSB)
5	DB6	Data Input Bit 6
6	DB5	Data Input Bit 5
7	DB4	Data Input Bit 4
8	DB3	Data Input Bit 3

PIN NO.	NAME	DESCRIPTION
9	DB2	Data Input Bit 2
10	DB1	Data Input Bit 1
11	DB0	Data Input Bit 0 (LSB)
12	$\overline{CS}$	Chip Select
13	$\overline{WR}$	Write
14	V_{DD}	Power Supply
15	V_{REF}	Reference Input
16	R_{FB}	Feedback Resistance

ELECTRICAL CHARACTERISTICS
(V_{DD} = + 3.3 V, V_{REF} = +3 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]						FSR = Full Scale Range
Resolution (All Grades)	N	8			Bits	
Integral Non-Linearity (Relative Accuracy)	INL			±1	LSB	End Point Linearity
Differential Non-Linearity	DNL			±1	LSB	All grades monotonic over full temperature range.
Gain Error	GE			±3	LSB	Using Internal R_{FB} Digital Inputs = V_{INH}
Power Supply Rejection Ratio	PSRR		±100		ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 10% Digital Inputs = V_{INH}
Output Leakage Current	I_{OUT1}			±50nA	nA	Digital Inputs = V_{INL}
DYNAMIC PERFORMANCE						RL = 100Ω, C_L = 10pF
Current Settling Time[2]	t_S		100		ns	Full Scale Change to 1/2 LSB
AC Feedthrough at I_{OUT1}[2]	F_T		±1/2		LSB	V_{REF}=100kHz, 20 Vp-p, sinewave
at I_{OUT2}			±1/2		LSB	DB0-DB7 = 0 V, $\overline{CS}$ = $\overline{WR}$ = 0 V
REFERENCE INPUT						
Input Resistance	R_{IN}	5		20	kΩ	
DIGITAL INPUTS[3]						
Logical "1" Voltage	V_{IH}	+2.0			V	
Logical "0" Voltage	V_{IL}			+0.8	V	
Input Leakage Current	I_{LKG}			±1	μA	
Input Capacitance[2]	C_{IN}			20	pF	V_{IN} = 0 V
ANALOG OUTPUTS[2]						
Output Capacitance						
	C_{OUT1}			70	pF	DAC Inputs all 1's
	C_{OUT1}			30	pF	DAC Inputs all 0's
	C_{OUT2}			20	pF	DAC Inputs all 1's
	C_{OUT2}			60	pF	DAC Inputs all 0's
POWER SUPPLY[5]						
Functional Voltage Range	V_{DD}	3	3.3	3.6	V	
Supply Current	I_{DD}		10	100	μA	All digital inputs = 0 V or all =V_{DD}

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
SWITCHING CHARACTERISTICS[2, 4]						
Chip Select to Write Set-Up Time	t_{CS}		170		ns	
Chip Select to Write Hold Time	t_{CH}		0		ns	
Data Valid to Write Set-Up Time	t_{DS}		135		ns	
Data Valid to Write Hold Time	t_{DH}		10		ns	
Write Pulse Width	t_{WR}		170		ns	
VOLTAGE MODE OPERATION[2, 6]						
Integral Nonlinearity Error @ V_{REF}	INL			1	LSB	I_{OUT1} = 1.2 V I_{OUT2} = 0 V

NOTES:

1 Full Scale Range (FSR) is 3 V for unipolar mode and ±3 V for bipolar.
2 Guaranteed but not production tested .
3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4 See timing diagram.
5 Specified values guarantee functionality. Refer to other parameters for accuracy.
6 Refer to *Figure 7.*

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2]

V_{DD} to GND . . . . −0.5, +5 V
Digital Input Voltage to GND (2) . . GND −0.5 to V_{DD} +0.5 V
I_{OUT1}, I_{OUT2} to GND . . . . −0.5 to 5 V
V_{REF} to GND . . . . ±25 V
V_{RFB} to GND . . . . ±25 V

Storage Temperature . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 seconds) . . . . +300°C
Package Power Dissipation Rating to 75°C
PDIP, SOIC 700mW
Derates above 75°C . . . . 10mW/°C

NOTES:

1 Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies.

APPLICATION NOTES

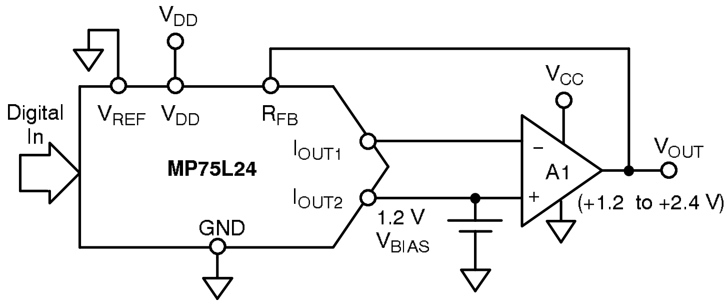


Figure 1. Single Supply Operation with 1.2 V to 2.4 V Swing

The R-2R ladder termination resistor on the MP75L24 is internally connected to I_{OUT2}. This configuration allows the use of the DAC in the single supply current steering mode, where I_{OUT2} is biased above ground level.

Figure 2. shows the generalized configuration.

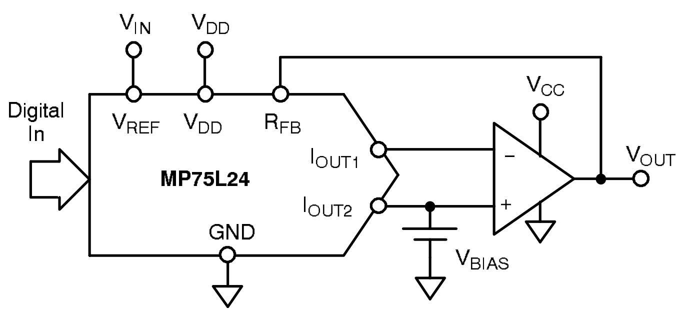


Figure 2. Single Supply Operation in Current Switching Mode

The advantage of this single supply configuration over the voltage switching mode is the greater flexibility with which the output voltage swing can be defined. A low impedance reference bias voltage is needed. Unlike the voltage switching mode which has a minimum output voltage of 0V, the current steering mode allows for output swings that do not have to approach the rail voltages. The equation for this configuration is:

$$V_{OUT} = \frac{D}{256}(V_{BIAS} - V_{IN}) + V_{BIAS}$$

where D=decimal equivalent of the DAC digital input code
V_{BIAS} is a voltage reference: $0\ V \leq V_{BIAS} \leq 1.2V$ for best linearity.
V_{IN} is a bipolar input voltage

By choosing the proper V_{BIAS} and V_{IN}, the output voltage can be set in the range between V_{BIAS} and $2V_{BIAS} - V_{IN}$. For example, for V_{DD} = 3.3, select V_{IN} = 0 V and V_{BIAS} = 1.2 V. This will result in a swing of 1.2 V to 2.4 V.

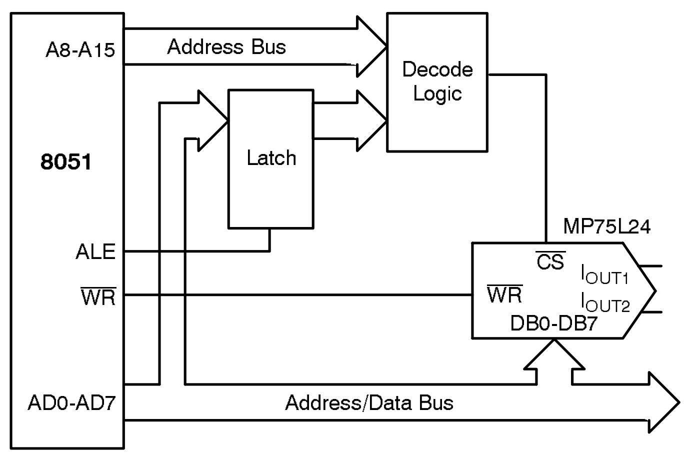


Figure 3. Microcontroller Interface

INTERFACE LOGIC INFORMATION

Mode Selection

MP75L24 mode selection is controlled by the $\overline{\text{CS}}$ and $\overline{\text{WR}}$ inputs.

Write Mode

When $\overline{\text{CS}}$ and $\overline{\text{WR}}$ are both LOW, the MP75L24 is in the WRITE mode, and the MP75L24 analog circuit responds to data activity at the DB0-DB7 data bus inputs. In this mode, the MP75L24 acts like a non-latched input D/A converter.

Hold Mode

When either $\overline{\text{CS}}$ or $\overline{\text{WR}}$ is HIGH, the MP75L24 is in the HOLD mode. The MP75L24 analog output holds the value corresponding to the last digital input present at DB0-DB7 prior to $\overline{\text{WR}}$ or $\overline{\text{CS}}$ assuming the high state.

$\overline{\text{CS}}$	$\overline{\text{WR}}$	Mode	DAC Response
L	L	Write	DAC responds to data bus (DB0-DB7) inputs
H	X	Hold	Data Bus (DB0-DB7) is locked out
X	H	Hold	DAC holds last data present when $\overline{\text{WR}}$ assumed HIGH state

L = LOW state, H = HIGH state, X = Don't care state

Table 1. Mode Selection Table

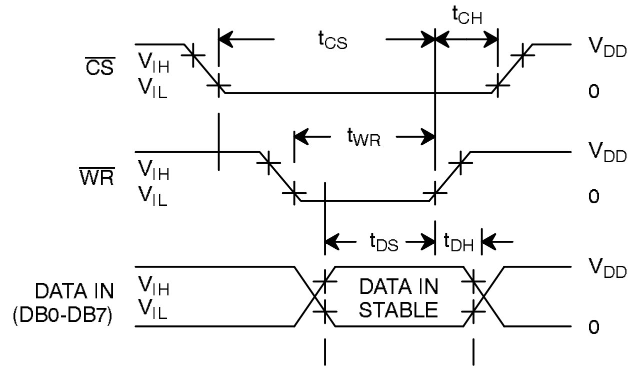


Figure 4. Write Cycle Timing Diagram

MICROPROCESSOR INTERFACE

MP75L24/8080A Interface

Figure 5. shows the MP75L24 used in the MCS-80 microcomputer system as a Memory Mapped Output Device. The basic CPU group consists of the 8080A CPU, 8224 clock generator and 8228 system controller/bus driver. The MP75L24 $\overline{\text{WR}}$ input is connected to the 8228 system data bus outputs. The $\overline{\text{CS}}$ input is connected to the system address decoding logic. Note that pull-up resistors R3 and R4 are required to ensure that the $\overline{\text{CS}}$ and $\overline{\text{WR}}$ input HIGH states reach 3.0V min. Pull-ups are not required on the system data bus since the 8228 V_{OH} is 3.6 V min for DB0-DB7.

System timing is shown in Figure 6. Data is loaded into the MP75L24 when the $\overline{\text{WR}}$ and $\overline{\text{CS}}$ inputs are both LOW. The data is latched into the MP75L24 when $\overline{\text{WR}}$ returns HIGH. MP75L24 updating is accomplished by using any of the 8080A memory write instructions.

The MP75L24 can also be addressed and loaded as an isolated Output Device by connecting the MP75L24 $\overline{\text{WR}}$ input to the 8228 $\overline{\text{I/O W}}$ terminal (instead of $\overline{\text{MEMW}}$).

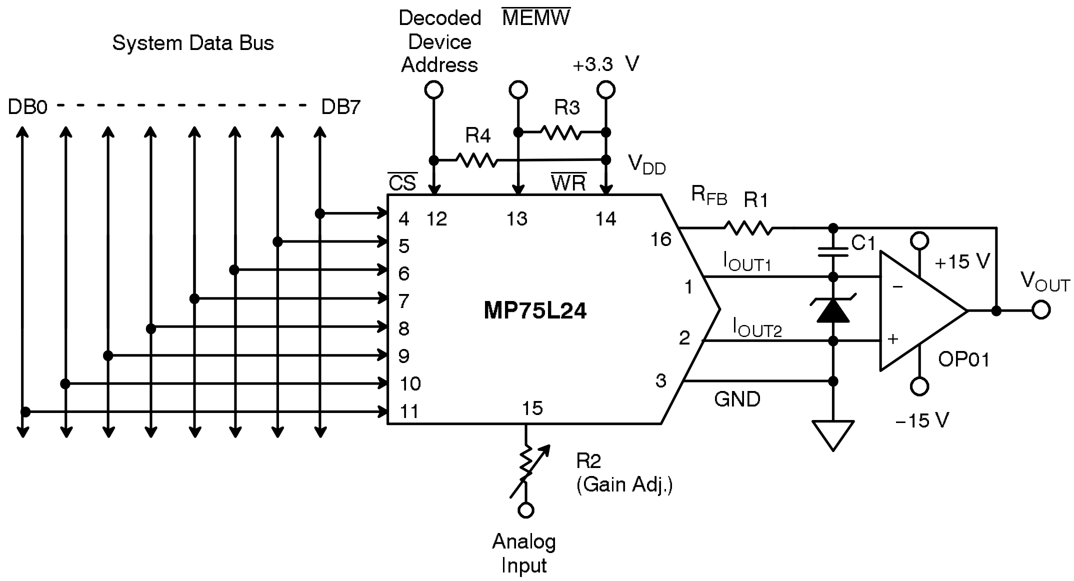


Figure 5. MP75L24/8080A Interface

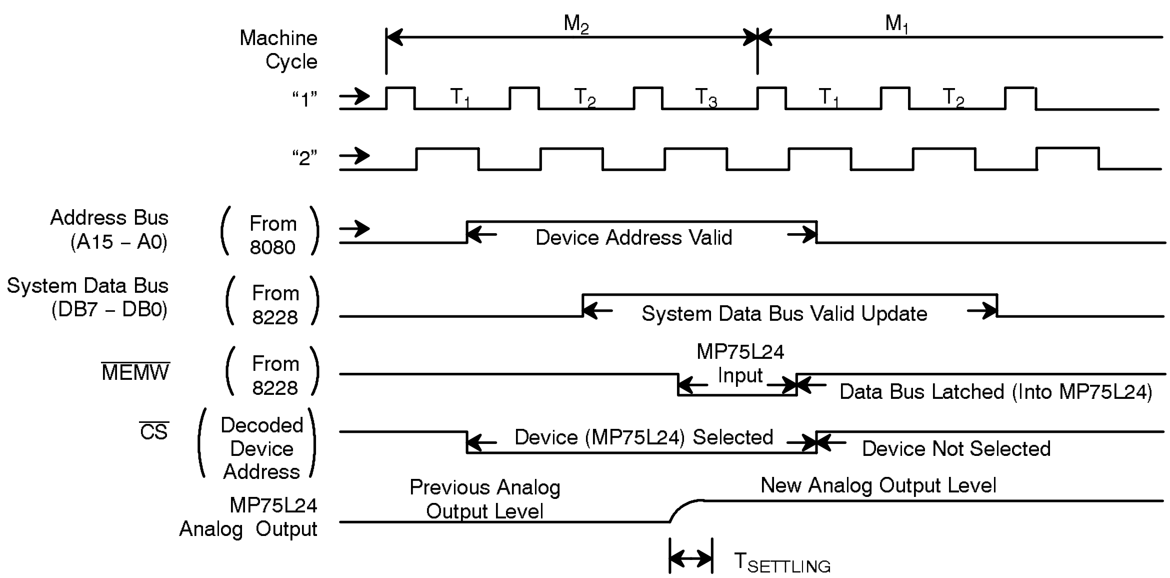


Figure 6. Timing Diagram

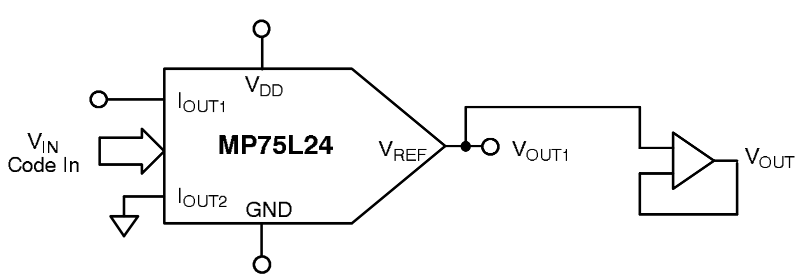
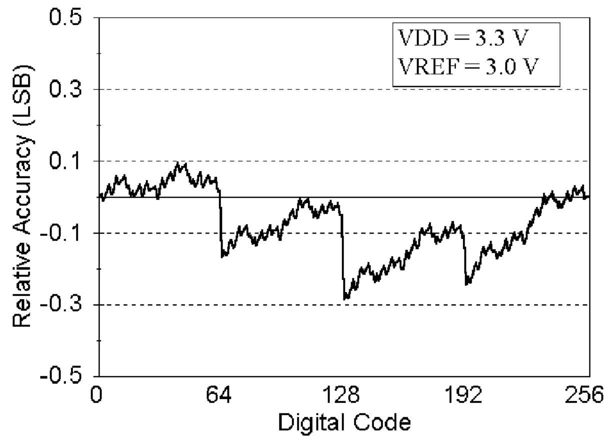


Figure 7. Voltage Mode Operation

PERFORMANCE CHARACTERISTICS



Graph 1. Relative Accuracy vs. Digital Code