XC66D Series

Positive Voltage Regulators with Built - in Voltage Detect Functions

◆CMOS
◆Maximum Output Current : 100mA(VOUT=5.0V)
◆Highly Accurate Output Voltage : ±2%
◆Output Voltage Range : 2.0V~ 6.0V
◆Highly Accurate Voltage Detection : ±2%
◆No Load Supply Current : 3.2μA(5.0V)
◆SOT-25 Package

■Applications

- ●Battery use
- ●Battery life & charge detection
- ●Memory battery back-up circuits
- ●Microprocessor reset circuitry
- ●Power failure detection
- ●Voltage Sources Reference
- ●Cameras, Video Cameras
- ●Various Portable Devices

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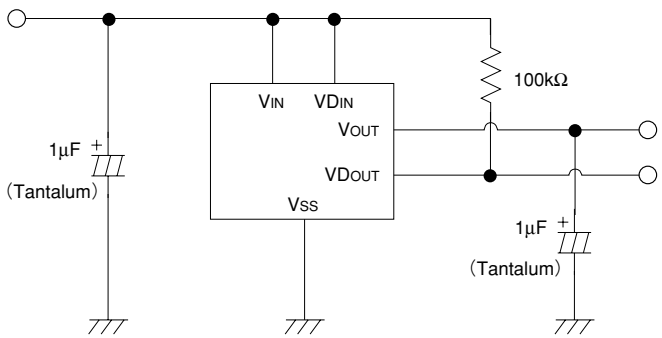
■General Description

The XC66D series consists of a voltage detector and voltage regulator built into the one chip and is, essentially, a voltage regulator with voltage detect capabilities.
Low power consumption and high accuracy is achieved through CMOS and laser trimming technologies.
The detector features an output driver, hysteresis circuit, comparator and extremely accurate standard voltage.
The regulator features an error amplification circuit, output driver with current limiter functions, minimal input-output voltage differential and similary accurate standard voltage.
SOT-25 (150mW) package is available.

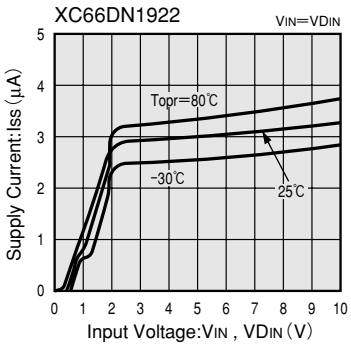
■Features

Maximum Output Current	: 100mA (Within max. continuous total power dissipation, VOUT=5.0V)
Output Voltage Range	: 2.0V ~ 6.0V (0.1V steps, Standard 5.0V)
Highly Accurate Output Voltage	: Fixed voltage accuracy ±2%
Output Voltage Temperature Characteristics	: Typ. ±100ppm/°C
Detect Voltage Range	: 1.8V ~ 6.0V (0.1V steps)
Highly Accurate Detect Voltage	: Fixed voltage accuracy ±2%
Low Power Consumption	: Typ. 3.2μA (VOUT= 5.0V)
Detect Voltage Temperature Characteristics	: Typ. ±100ppm/°C
Detect Voltage Output Configuration	: N-ch open drain CMOS (High level =VOUT)
Input Stability	: Typ. 0.1%/V
Ultra Small Packages	: SOT- 25 (150mW) mini-mold

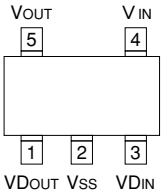
■Typical Application Circuit



■Typical Performance Characteristic



■Pin Configuration



SOT-25
(TOP VIEW)

■Pin Assignment

PIN NUMBER	PIN NAME	FUNCTION
1	VDOUT	Voltage Detect Output
2	VSS	Ground
3	VDIN	Voltage Detect Input
4	VIN	Power Supply
5	VOUT	Voltage Regulator Output

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■Product Classification

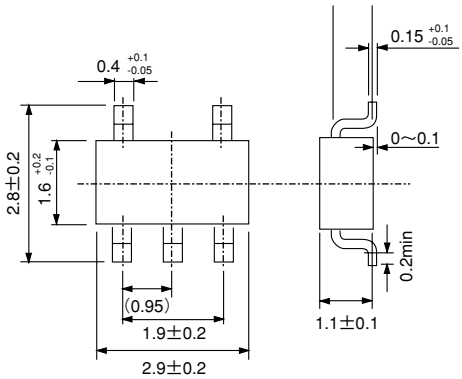
●Ordering Information

X C 6 6 D X X X X X X X
a b c d e f

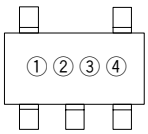
DESIGNATOR	DESCRIPTION	DESIGNATOR	DESCRIPTION
a	Detector Output Configuration C=CMOS(High level=VOUT) N=N-ch open drain	d	Package Type M=SOT-25
b	Detect Voltage (VDF) 25=2.5V 38=3.8V	e	Device Orientation R=Embossed Tape (Standard Feed) L=Embossed Tape (Reverse Feed)
c	Regulator Output Voltage (VOUT) 33=3.3V 50=5.0V		

■Packaging Information

●SOT-25



■Marking



SOT-25
(TOP VIEW)

① Represents the Product Series, Type, and the integer of the Detect Voltage

PRODUCT SERIES TYPE	DETECT VOLTAGE			
	DESIGNATOR	VOLTAGE (V)	DESIGNATOR	VOLTAGE (V)
N-ch XC66DN Series	A	0.X	F	5.X
	B	1.X	H	6.X
	C	2.X	K	7.X
	D	3.X	L	8.X
	E	4.X	M	9.X
CMOS High level V_{OUT} XC66DC Series	*A*	0.X	*F*	5.X
	B	1.X	*H*	6.X
	C	2.X	*K*	7.X
	D	3.X	*L*	8.X
	E	4.X	*M*	9.X
CMOS High level V_{IN} XC66DD Series	*N*	0.X	*U*	5.X
	P	1.X	*V*	6.X
	R	2.X	*X*	7.X
	S	3.X	*Y*	8.X
	T	4.X	*Z*	9.X

② Represents the decimal number of the Detect Voltage and the Off-set of the Output Voltage

OFF-SET OF THE OUTPUT VOLTAGE	DETECT VOLTAGE			
	DESIGNATOR	VOLTAGE (V)	DESIGNATOR	VOLTAGE (V)
0V	0	X.0	5	X.5
	1	X.1	6	X.6
	2	X.2	7	X.7
	3	X.3	8	X.8
	4	X.4	9	X.9
5V	A	X.0	F	X.5
	B	X.1	H	X.6
	C	X.2	K	X.7
	D	X.3	L	X.8
	E	X.4	M	X.9

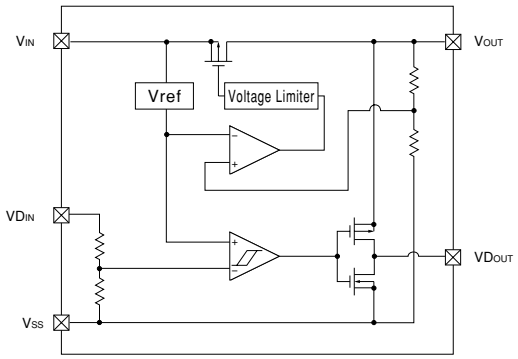
③ Represents the Output Voltage

INTEGER OF THE OUTPUT VOLTAGE	DETECT VOLTAGE			
	DESIGNATOR	VOLTAGE (V)	DESIGNATOR	VOLTAGE (V)
0V + Off-set	0	X.0	5	X.5
	1	X.1	6	X.6
	2	X.2	7	X.7
	3	X.3	8	X.8
	4	X.4	9	X.9
1V + Off-set	A	X.0	F	X.5
	B	X.1	H	X.6
	C	X.2	K	X.7
	D	X.3	L	X.8
	E	X.4	M	X.9
2V + Off-set	N	X.0	U	X.5
	P	X.1	V	X.6
	R	X.2	X	X.7
	S	X.3	Y	X.8
	T	X.4	Z	X.9
3V + Off-set	*A*	X.0	*F*	X.5
	B	X.1	*H*	X.6
	C	X.2	*K*	X.7
	D	X.3	*L*	X.8
	E	X.4	*M*	X.9
4V + Off-set	*N*	X.0	*U*	X.5
	P	X.1	*V*	X.6
	R	X.2	*X*	X.7
	S	X.3	*Y*	X.8
	T	X.4	*Z*	X.9

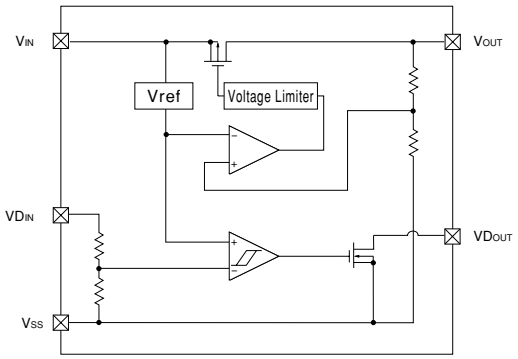
④ Denotes the production lot number
0 to 9, A to Z repeated(G.I.J.O.Q.W excepted)
* Italic type : Character inversion

■Block Diagram

(1) XC66DC CMOS output (High level =VOUT)



(2) XC66DN N-ch open drain



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■Absolute Maximum Ratings

Ta=25°C

PARAMETER		SYMBOL	RATINGS	UNITS
Regulator Input Voltage		VIN	VSS -0.3 ~ 12	V
Regulator Output Current		IOUT	150	mA
Regulator Output Voltage		VOUT	VSS -0.3 ~ VIN +0.3	V
Detector Input Voltage		VDIN	VSS -0.3 ~ 12	V
Detector Output Current		IDOUT	50	mA
Detector Output Voltage	N-ch open drain output	VDOUT	VSS -0.3 ~ 12	V
	CMOS output (High level =VOUT)		VSS -0.3 ~ VIN +0.3	
Continuous Total Power Dissipation		Pd	150	mW
Operating Ambient Temperature		Topr	-30 ~ +80	°C
Storage Temperature		Tstg	-40 ~ +125	°C

Note: Please ensure that {(VIN -VOUT) x IOUT} + {IDOUT x VDOUT} + {VIN x ISS} does not exceed the stated Pd values.

■Electrical Characteristics

V_{DF} =1.8V ~ 6.0V, $V_{OUT}(T)$ (Note1) =5V

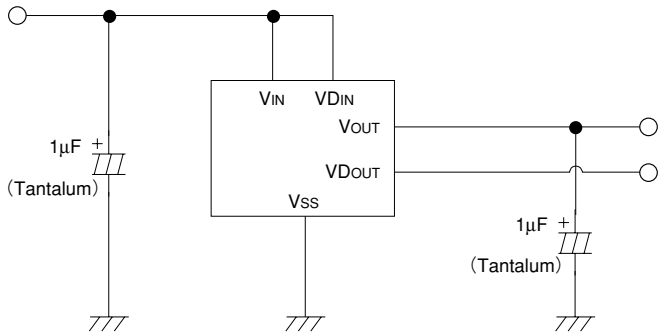
Ta=25°C

	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	CIRCUIT
DETECTOR	Detect Voltage	V_{DF}	V_{IN} = VD_{IN}	(V_{DF}) x 0.98	V_{DF}	(V_{DF}) x 1.02	V	1
	Hysteresis Range	V_{HYS}	V_{IN} = VD_{IN}	(V_{DF}) x 0.02	(V_{DF}) x 0.05	(V_{DF}) x 0.08	V	1
	Operating Voltage	V_{IN}		1.5	–	10.0	V	–
	Output Current	ID_{OUT}	N-ch V_{DS}=0.5V V_{SS}=1.5V =2.0V =3.0V =4.0V =5.0V	0.3 3.0 5.0 6.0 7.0	2.2 7.7 10.1 11.5 10.3	– – – – –	mA	2
			P-ch V_{DS}=0.9V V_{IN}=VD_{IN}=V_{OUT}=8V (CMOS)	–	-5	-2		6
	VD_{IN} Input Current	ID_{IN}	VD_{IN}=10V	–	0.4	1.0	µA	3
	Detect Voltage Temp. Characteristics	$\frac{\Delta V_{OUT}}{\Delta Topr \cdot V_{DF}}$	-30°C ≤ Topr ≤ 80°C	–	±100	–	ppm/°C	1
REGULATOR	Output Voltage	V_{OUT} (E) (Note2)	I_{OUT}=10mA V_{IN} = $V_{OUT}(T)$ + 1V	4.9	5	5.1	V	4
	Maximum Output Current	I_{OUT}max	V_{IN}= $V_{OUT}(T)$ + 1V $V_{OUT}(E)$ ≥ $V_{OUT}(T)$ x0.9	100	–	–	mA	4
	Load Stability	ΔV_{OUT}	V_{IN}= $V_{OUT}(T)$ + 1V 1mA ≤ I_{OUT} ≤ 80mA	–	20	80	mV	4
	Input - Output Voltage Differential	Vdif (Note3)	I_{OUT} =60mA	–	260	520	mV	4
	Input Stability	$\frac{\Delta V_{OUT}}{\Delta V_{IN} \cdot V_{OUT}}$	I_{OUT}=10mA $V_{OUT}(T)$ + 1V ≤ V_{IN} ≤ 10V	–	0.1	0.3	%/V	4
	Output Voltage Temp. Characteristics	$\frac{\Delta V_{OUT}}{\Delta Topr \cdot V_{OUT}}$	I_{OUT} =10mA -30°C ≤ Topr ≤ 80°C	–	±100	–	ppm/°C	4
	Input Voltage	V_{IN}		–	–	10.0	V	–
	Supply Current	I_{SS}	V_{IN} = $V_{OUT}(T)$ +1V	–	3.2	8.6	mA	5

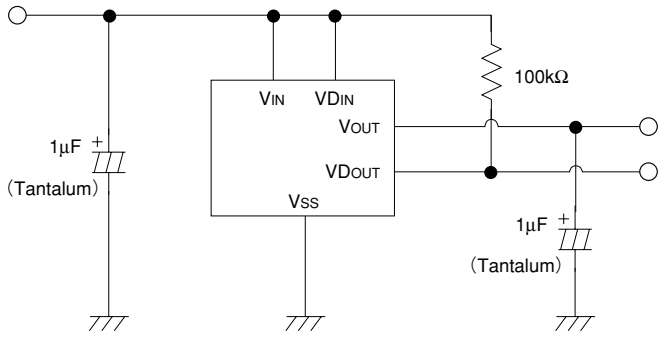
Note: 1. $V_{OUT}(T)$: User specified output voltage.
2. $V_{OUT}(E)$: Effective output voltage.
(i.e. the output voltage when a stable ($V_{OUT}(T)$ + 1.0V) is provided, while maintaining a certain I_{OUT} value.)
3. Vdif : Vdif = {$V_{IN}1$ - $V_{OUT}1$}
$V_{OUT}1$: The voltage equal to 98% of the output voltage whenever a stable ($V_{OUT}(T)$ +1.0V) is provided at I_{OUT}.
$V_{IN}1$: The input voltage when the output is equal to $V_{OUT}(E)$ x 98%.

■Typical Application Circuits

CMOS Output (High Level =VOUT)



N-ch Open Drain



■Directions for use

●Notes on Use

1. In cases where there is no capacitance (C_L), or the capacitance is small, or where a capacitor with an extremely low ESR value is used (e.g. ceramic), please use a capacitor (C_L = 1.0μF [Tantalum]) in order to stop oscillation that may occur as the phase margin becomes smaller.

2. To reduce impedance between the power supply and the IC's input pin, which in turn will stop oscillation resulting from input voltage changes, connect a capacitor (C_{IN} = more than 1.0μF, ESR low) to the input side of the IC. Further, operation may become unstable and oscillation may occur shoud impedance up to the IC's input be high (a state which could be brought about by several factors including which devices are added to the input side, the surrounding wiring and/or the input power supply.)
   Stability can be improved by regulating increases in input capacitance and by reducing impedance.

3. The regulator's input pin (V_{IN}) and power supply pin are the same. Also, the voltage detector's power supply and the voltage regulator's power supply are the same. Therefore, to have the voltage detector operating normally, it is necessary to apply a voltage larger than the minimum operating voltage (1.5V) to the power supply input pin (V_{IN}).

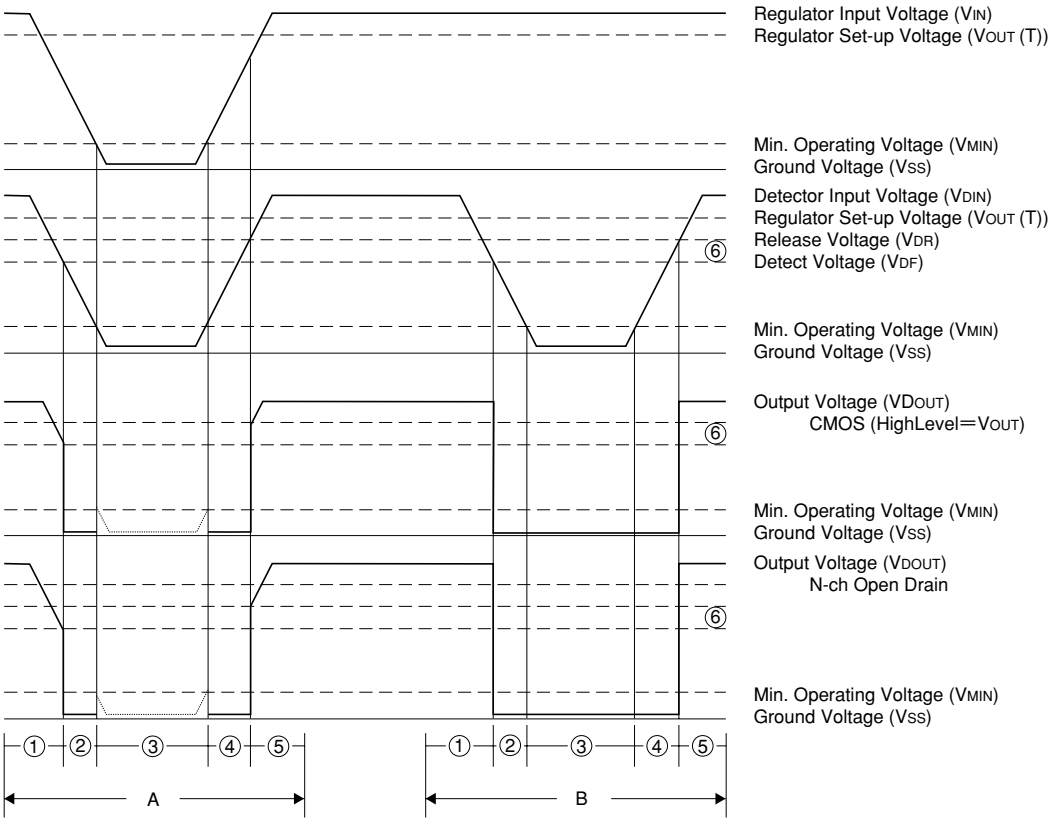
4. With CMOS output, the detector's output voltage equals the regulator's output voltage following release. Possible changes in the regulator's output voltage (V_{ROUT}), following regulator load changes, will be output at the detector's output pin (VD_{OUT}).

5. As the operations of the detector will momentarily respond when steep rise and fall time voltages are input at the power supply pin (V_{IN}), please ensure that the V_{IN}(VD_{IN}) pin's input frequency's rise and fall time is more than 5μ sec/V.

6. When using with the detector input pin (VD_{IN}) connected to the regulator output pin (V_{OUT}), the detector will momentarily respond as a result of transient output voltage changes brought about by the regulator's load changes. With large load currents and/or large load transitions from 1mA to 80mA for example, output voltage will momentarily drop, so please add a capacitor where C_L=more than 4.7mF.

■Operational Explanation

●Timing Chart (N-ch open drain pull up voltage =Input voltage V_{IN})



●Operational Notes [Detector : CMOS Output ('High' level = V_{OUT})]

Timing Chart A (V_{IN}=VD_{IN})

1. When a voltage greater than the release voltage (V_{DR}) is applied to the voltage input pin (V_{IN}, VD_{IN}), input voltage (V_{IN}, VD_{IN}) will gradually fall. When a voltage greater than the detect voltage (V_{DF}) is applied to the voltage input pin (V_{IN}, VD_{IN}), the output pin(VD_{OUT}) voltage will be equal to the regulator's output voltage (V_{OUT}).
   * With N-ch open drain configurations a state of high impedance means that should the pin be pulled up, voltage will be equal to pull up voltage.

2. When input voltage (V_{IN}, VD_{IN}) fall below detect voltage (V_{DF}), output voltage (VD_{OUT}) will be equal to ground level (V_{SS}).

3. Should input voltage (V_{IN}, VD_{IN}) fall below the minimum operational voltage (V_{MIN}), output will become unstable.
   Should VD_{IN} fall below V_{MIN}, voltage at the output pin (VD_{OUT}) will be equal to ground level (V_{SS}) .
   *With N-ch open drain configurations output will equal pull up voltage as the output pin is generally pulled up.

4. Should input voltage (V_{IN}, VD_{IN}) rise above ground voltage (V_{SS}), output voltage (VD_{OUT}) will equal ground level until the release voltage level (V_{DR}) is reached.

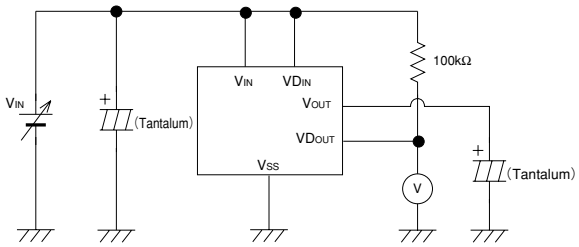
5. The output pin voltage (VD_{OUT}) will be equal to the regulator output voltage (V_{OUT}) when input voltage (V_{IN}, VD_{IN}) rises above release voltage.
   *With N-ch open drain configurations it will be equal to the voltage dependent on pull up.

Timing Chart B (V_{IN}=voltages above set-up voltage + input/output voltage differential, VD_{IN} = sweep voltage)
Because a voltage higher than the minimum operating voltage is applied to the voltage input pin (V_{IN}), ground voltage will be output at the output pin (VD_{OUT}) during stage 3. (Stages 1, 2, 4, 5 are the same as in A above).

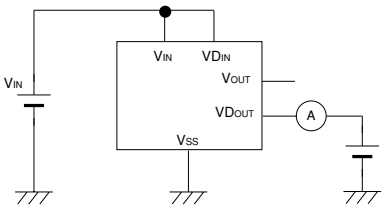
Note : The difference between release voltage (V_{DR}) and detect voltage (V_{DF}) is the Hysteresis Range (6).

■Test Circuits

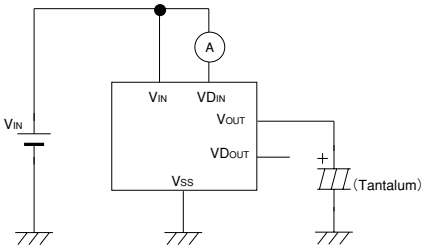
Circuit 1



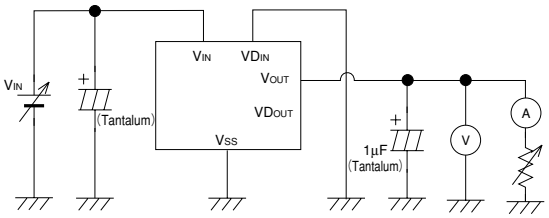
Circuit 2



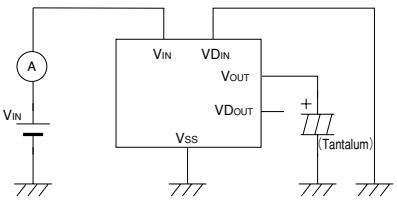
Circuit 3



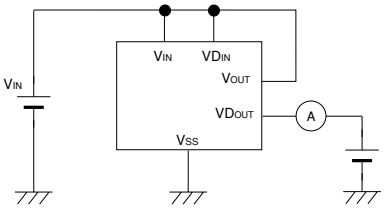
Circuit 4



Circuit 5

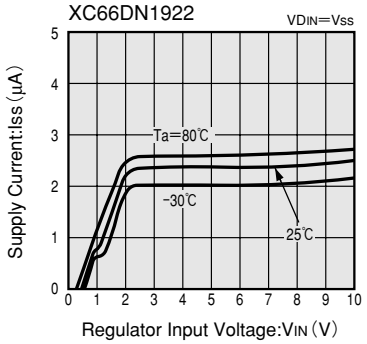


Circuit 6

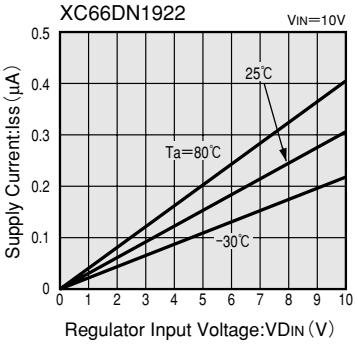


■Typical Performance Characteristics

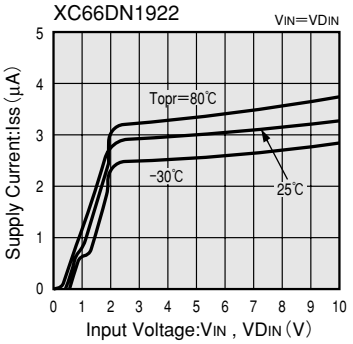
(1) SUPPLY CURRENT vs. REGULATOR INPUT VOLTAGE



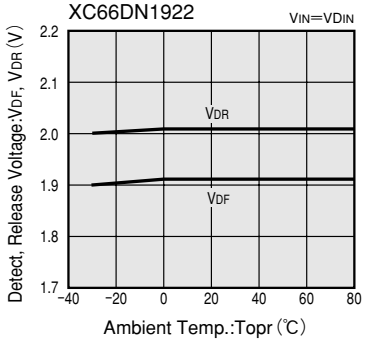
(2) SUPPLY CURRENT vs. DETECTOR INPUT VOLTAGE



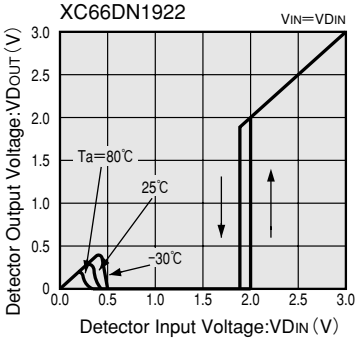
(3) SUPPLY CURRENT vs. REGULATOR, DETECTOR INPUT VOLTAGE



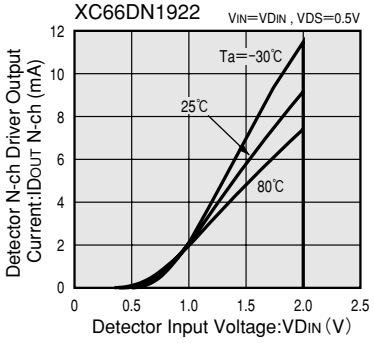
(4) DETECT VOLTAGE, RELEASE VOLTAGE vs. AMBIENT TEMPERATURE



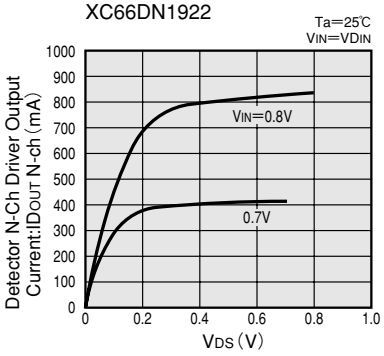
(5) DETECTOR OUTPUT VOLTAGE vs. DETECTOR INPUT VOLTAGE

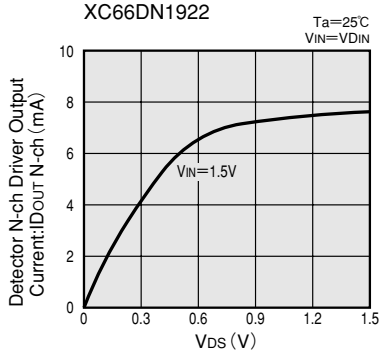


(6) DETECTOR N-ch DRIVER OUTPUT CURRENT vs. VDS

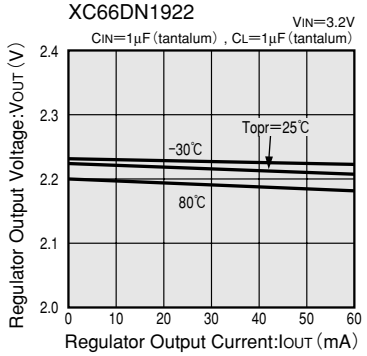


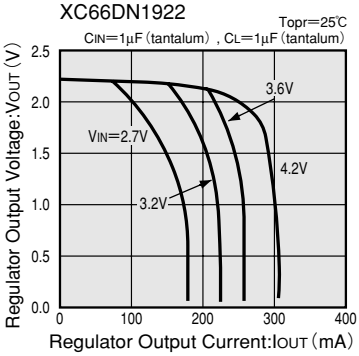
(7) DETECTOR N-ch DRIVER OUTPUT CURRENT vs. DETECTOR INPUT VOLTAGE





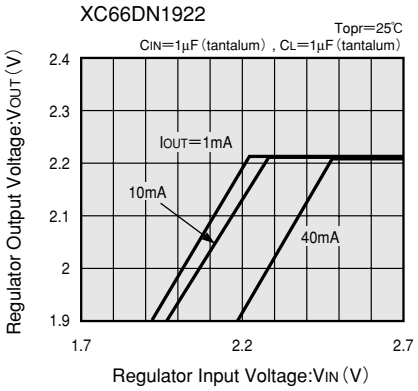
(8) REGULATOR OUTPUT VOLTAGE vs. REGULATOR OUTPUT CURRENT

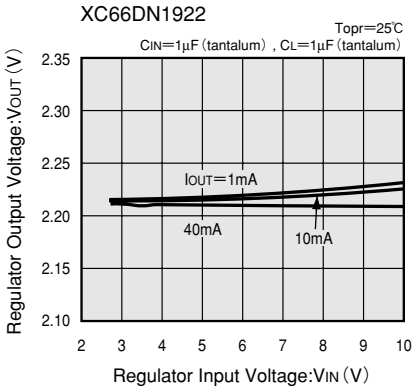




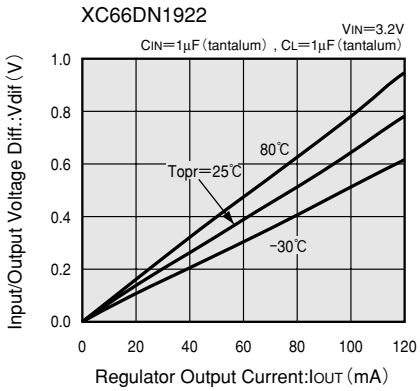
3

(9) REGULATOR OUTPUT VOLTAGE vs. REGULATOR INPUT VOLTAGE

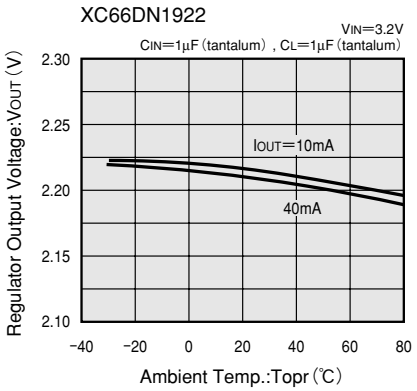




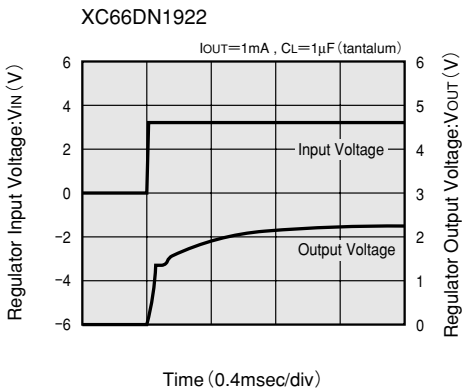
(10) INPUT/OUTPUT VOLTAGE DIFFERENTIAL vs. REGULATOR OUTPUT CURRENT

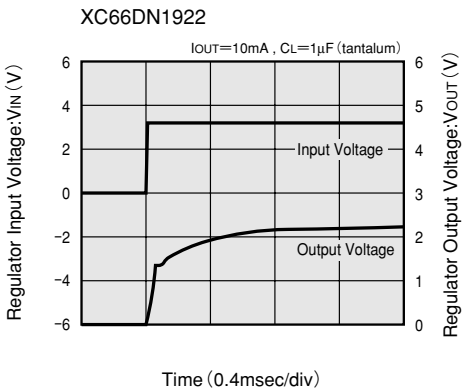


(11) REGULATOR OUTPUT VOLTAGE vs. AMBIENT TEMPERATURE



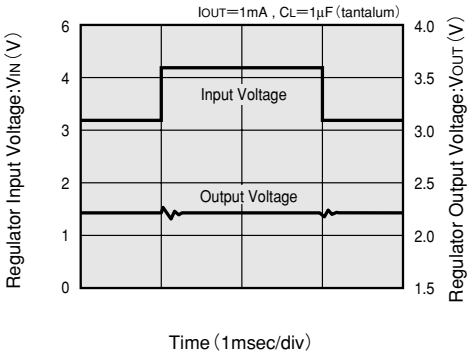
(12) INPUT TRANSIENT RESPONSE 1





(13) INPUT TRANSIENT RESPONSE 2

XC66DN1922



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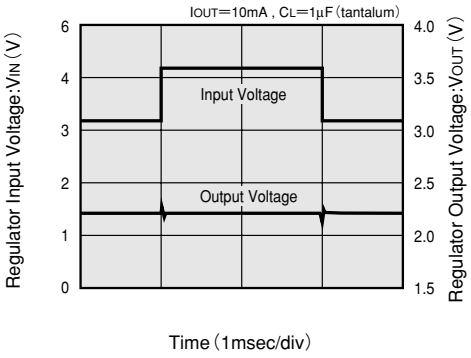
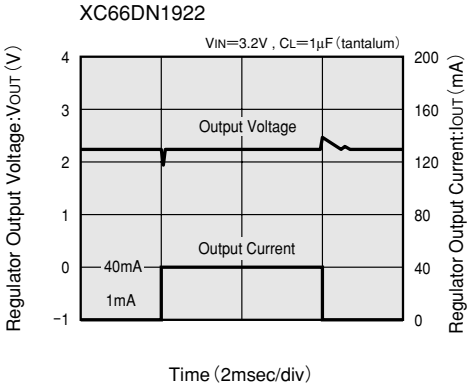


(14) LOAD TRANSIENT RESPONSE

XC66DN1922



(15) RIPPLE REJECTION RATE

XC66DN1922