3965

PRELIMINARY DATASHEET - 12/4/2002
(Subject to change without notice)

DMOS DUAL FULL-BRIDGE PWM MOTOR DRIVER

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

Load Supply Voltage, VBB ..... **20 V**
Output Current, I_{OUT}..... **±500 mA***
Logic Supply Voltage, V_{DD}..... **7.0 V**
Logic Input Voltage Range,
V_{IN} ..... **-0.3 V to V_{DD} + 0.3 V**
(t_W<30ns) ..... **-1.0V to V_{DD} +1V**
Sense Voltage, V_{SENSE}..... **0.5 V**
Reference Voltage, V_{REF} ..... **3 V**
Package Power Dissipation (T_A = +25°C), P_D
A3965SLB..... **50°C/W****

Operating Temperature Range,
T_A ..... **-20°C to +85°C**
Junction Temperature, T_J ..... **+150°C**
Storage Temperature Range,
T_S..... **-55°C to +150°C**

***** Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current rating or a junction temperature of 150°C.

*Measured with 062" thick FR4, two sided PCB with 1 sq inch copper area.

Designed for Pulse Width Modulated (PWM) current control of low voltage stepper motors, the A3965S is capable of output currents to ± 500 mA and operating voltages to 20 V.

The A3965 is particularly attractive for low power or battery operated motors where minimal power consumption is desired. A SLEEP mode disables all circuitry and typically draws less than 1μA supply current from motor and logic supply. During operation the fixed frequency ON pulses of each H-bridge are 180 degrees out of phase to minimize the peak demand required of the motor supply allowing savings in size and cost of external power supply components.

PHASE and ENABLE input terminals are provided for use in controlling the speed and direction of a stepper motor with externally applied PWM control signals.

Internal circuit protection includes thermal shutdown with hysteresis, undervoltage monitoring of V_{DD} and charge pump, and crossover current protection. Special power up sequencing is not required.

The A3965 is supplied in a 24-lead plastic SOIC with a copper batwing tab (suffix 'LB').

FEATURES

- ±500 mA, 20 V Output Rating
- 2.85 to 5.5V Logic Supply Operation
- Sleep Mode for Minimum Power Consumption
- Fixed Frequency PWM
- Offset On Pulses to Minimize Peak Supply Transient Currents
- Internal UVLO and Thermal Shutdown Circuitry
- Crossover-Current Protection

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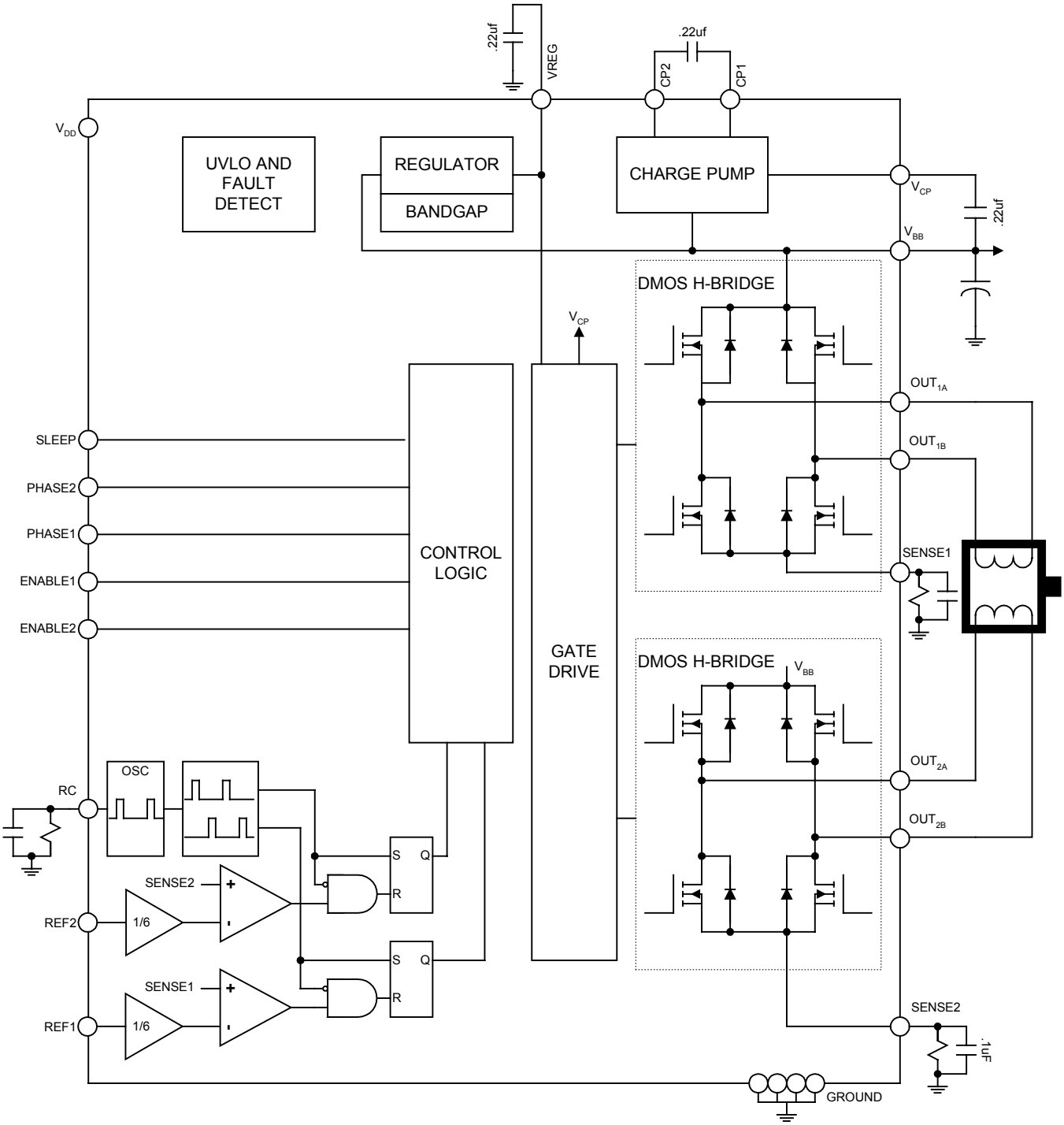
Functional Block Diagram



ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 20 V, V_{DD} = 3.0 V, V_{SENSE} = 0.5 V, f_{PWM} < 50KHz (unless noted otherwise)

Characteristics	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Drivers						
Load Supply Voltage Range	VBB	Operating, I_{OUT} = ±500 mA	6	–	20	V
		During Sleep Mode	0		20	V
Output Leakage Current	I_{DSS}	V_{OUT} = V_{BB}	–	<1.0	20	µA
		V_{OUT} = 0 V	–	<–1.0	-20	µA
Output On Resistance	R_{DSON}	Source Driver, I_{OUT} = -500 mA	–	1.2	1.35	Ω
		Sink Driver, I_{OUT} = 500 mA	–	.75	.9	Ω
		Source Driver, I_{OUT} = -500 mA; VBB=6V		1.3	1.5	Ω
		Sink Driver, I_{OUT} = 500 mA, VBB=6V		.85	1.0	Ω
Body Diode Forward Voltage	V_F	Source Diode, I_F = -500 mA	–	1	–	V
		Sink Diode, I_F = 500mA	–	1	–	V
Motor Supply Current	I_{BB}	f_{PWM} < 50 kHz	–	3.5	7	mA
		Charge Pump On, Outputs Disabled	–	1.5	3	mA
		Sleep Mode	–	–	10	uA
Logic Supply Current	I_{DD}	f_{PWM} < 50 kHz			4.5	mA
		Outputs Off			3.6	mA
		Sleep Mode (Inputs below .5V)		<1	10	µA
Control Logic						
Logic Supply Voltage Range	V_{DD}	Operating	2.85		5.5	V
Logic Input Voltage	$V_{IN(1)}$		V_{DD}*.7	–		V
	$V_{IN(0)}$			–	V_{DD}*.3	V
Logic Input Current	$I_{IN(1)}$	V_{IN} = V_{DD}*.7	-20	<1.0	20	µA
	$I_{IN(0)}$	V_{IN} = V_{DD}*.3	-20	<1.0	20	µA

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Characteristics	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Control Logic						
Reference Input Current	I_{REF}	$V_{REF} = V_{DD}$	-1	0	1	µA
VREF input voltage range	V_{REF}		0		V_{DD}- .1	
Reference Divider Ratio	V_{REF}/V_S			6		
G_M Error	V_{ERR}	V_{REF} = 1.5V	-5		5	%
	(Note 3)	V_{REF} = .5V	-10		10	%
Propagation Delay	t_{PD}	PWM CHANGE TO SOURCE OFF	–	150	–	ns
		PWM CHANGE TO SINK OFF	–	150	–	ns
		PWM CHANGE TO SOURCE ON	–	1000	–	ns
		PWM CHANGE TO SINK ON	–	1000	–	ns
		DISABLE TO SOURCE ON	–	200	–	ns
		DISABLE TO SINK ON	–	200	–	ns
	t_{COD}		300	850	1200	ns
PWM RC Frequency	f_{OSC}	R = 1000pf, C = 20K		47.4		Khz
Blank Time	t_{BLANK}	R = 1000pf, C = 20K	.8	1.21	1.6	µs
Thermal Shutdown Temp.	T_J		–	165		°C
Thermal Shutdown Hysteresis	ΔT_J		–	15	–	°C
UVLO Enable Threshold		Rising V_{DD}		2.5	2.8	V
UVLO Hysteresis			0.05	0.10	–	V

NOTES: 1. Typical Data is for design information only.
2. Negative current is defined as coming out of (sourcing) the specified device pin.
3. $V_{ERR} = ((V_{REF}/6) – V_{SENSE})/(V_{REF}/6)$

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Functional Description

Sleep Mode. The input pin SLEEP is dedicated to put the device into a minimum current draw mode. All circuits are disabled including the VDD undervoltage monitor.

Shutdown. In the event of a fault due to excessive junction temperature, or low voltage on V_{CP} or V_{REG}, the outputs of the device are disabled until the fault condition is removed. At power up, and in the event of low V_{DD}, the UVLO circuit disables the drivers

Current Regulation. Load current is regulated by a fixed frequency PWM control circuit. When the outputs of the DMOS H-bridge are turned on, current increases in the motor winding until it reaches a value given by:

$$I_{TRIP} = V_{REF}/(6*R_{SENSE})$$

At the trip point, the sense comparator resets the source enable latch, turning off the source. At this point, load inductance causes the current to recirculate until the end fixed frequency cycle. (see timing diagram)

VREF. The V_{REF} voltage is divided down by 6 and compared to the voltage across the sense resistor to set the value of bridge current that will trip the PWM comparator. The V_{REF} input is a high impedance input and can be connected to V_{DD}, if desired, as well as via resistor divider. Note: When connected to V_{DD}, the V_{BB} voltage must be 1.8V greater than V_{DD} to allow proper headroom for the buffer output.

Fixed Frequency PWM. Selection of an external RC sets the oscillator frequency as follows:

$$f_{OSC} = 1/ (850ns + t_{BLANK}+R_TC_T))$$

Blank Time. When a source driver turns on, a current spike occurs due to the reverse recovery currents of the clamp diodes and/or switching transients related to distributed capacitance in the load. To prevent this current spike from erroneously resetting the source enable latch, the sense comparator is blanked. The blank duration is determined by the time it takes to charge the external RC $.38*V_{DD}$ volts with a 1mA current source.

$$t_{BLANK} = C_T*.38*V_{DD}/ (1mA – (.41*V_{DD}/R_T))$$

VREG. This supply voltage is used to run the sink side DMOS outputs. VREG is internally monitored and in the case of a fault condition, the outputs of the device are disabled. The VREG pin should be decoupled with a 0.22 µF capacitor to ground.

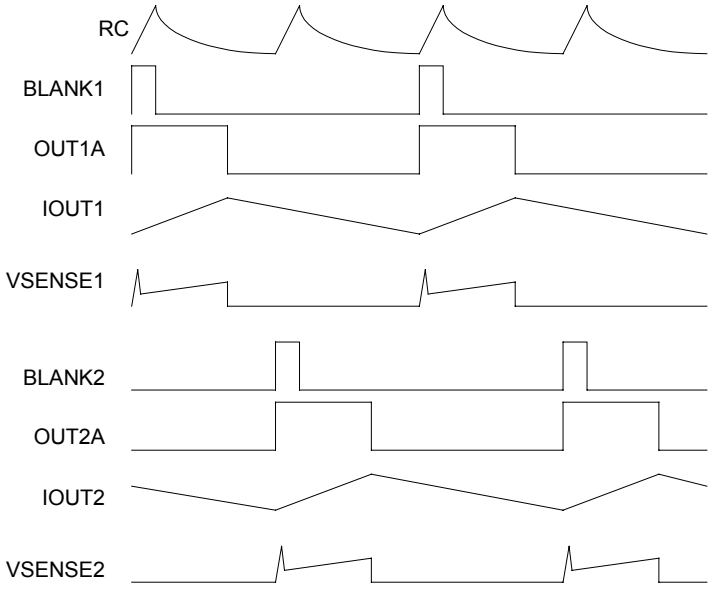
Charge Pump. The Charge Pump is used to generate a supply above VBB to drive the source side DMOS gates. A 0.22 uF ceramic monolithic capacitor should be connected between CP_1 and CP_2 for pumping purposes. A 0.22 uF ceramic monolithic capacitor should be connected between V_{CP} and VBB to act as a reservoir to run the high side DMOS devices. The V_{CP} Voltage is internally monitored and in the case of a fault condition the outputs of the device are disabled.

Thermal protection. Circuitry turns OFF all drivers when the junction temperature reaches 165°C typically. It is intended only to protect the device from failures due to excessive junction temperatures and should not imply that output short circuits are permitted. Thermal shutdown has a hysteresis of approximately 15°C.

Control Logic

Phase	Enable	Sleep	Chopping ($Vs>V_{REF}/6$)	OUT_A	OUT_B	Function
X	X	0	X	Off	Off	Sleep
X	1	1	X	Off	Off	Fast Decay
0	0	1	0	L	H	Forward
0	0	1	1	L	L	Slow Decay Chop
1	0	1	0	H	L	Reverse
1	0	1	1	L	L	Slow Decay Chop

Typical PWM Waveforms (Phase = 1)



Terminal List

Pin Name	Pin Description	SOIC 24
VREG	Regulator decoupling Terminal	1
RC	Analog Input for fixed frequency	2
SLEEP	Logic input for SLEEP mode	3
VDD	Logic Supply Voltage	4
OUT1B	DMOS H – Bridge 1 Output B	5
GND	Ground	6,7
SENSE1	Sense Resistor Terminal for Bridge 2	8
OUT1A	DMOS H – Bridge 1 Output A	9
ENABLE1	Logic Input for Bridge 1 Enable Control	10
PHASE1	Logic Input for Bridge 1 PHASE Control	11
REF1	G_m Reference Input Voltage Bridge 2	12
REF2	G_m Reference Input Voltage Bridge 1	13
PHASE2	Logic Input for Bridge 2 PHASE Control	14
ENABLE2	Logic Input for Bridge 2 Enable Control	15
OUT2B	DMOS H – Bridge 2 Output B	16
SENSE2	Sense Resistor Terminal for Bridge 1	17
GND	Ground	18,19
OUT2A	DMOS H – Bridge 2 Output A	20
VCP	Reservoir Capacitor Terminal	21
CP2	Charge Pump Capacitor Terminal	22
CP1	Charge Pump Capacitor Terminal	23
VBB	Load Supply	24