LSH33
32-bit Barrel Shifter with Registers

FEATURES

- 32-bit Input, 32-bit Output Multiplexed to 16 Lines
- Full 0-31 Position Barrel Shift Capability
- Integral Priority Encoder for 32-bit Floating Point Normalization
- Sign-Magnitude or Two's Complement Mantissa Representation
- 32-bit Linear Shifts with Sign or Zero Fill
- Independent Priority Encoder Outputs for Block Floating Point
- 68-pin PLCC, J-Lead

DESCRIPTION

The **LSH33** is a 32-bit high speed shifter designed for use in floating point normalization, word pack/unpack, field extraction, and similar applications. It has 32 data inputs, and 16 output lines. Any shift configuration of the 32 inputs, including circular (barrel) shifting, left shifts with zero fill, and right shifts with sign extension are possible. In addition, a built-in priority encoder is provided to aid floating point normalization.

Input/Output registers provide complete pipelined operation. Both have independent bypass paths for complete flexibility. When FTI = 1, the input registers are bypassed. Likewise, when FTO= 1, the output registers are bypassed.

SHIFT ARRAY

The 32 inputs, which can be registered, to the LSH33 are applied to a 32-bit shift array. The 32 outputs, which can also be registered, of this array are then multiplexed down to 16 lines for presentation at the device outputs. The array may be configured such that any contiguous 16-bit field (including wraparound of the 32 inputs) may be presented to the output pins under control of the shift code field (wrap mode). Alternatively, the wrap feature may be disabled, resulting in zero or sign bit fill, as appropriate (fill mode). The shift code control assignments and the resulting input to output mapping for the wrap mode are shown in Table 1.

Essentially the LSH33 is configured as a left shift device. That is, a shift code of 00000_2 results in no shift of the input field. A code of 00001_2 provides an effective left shift of 1 position, etc. When viewed as a right shift, the shift code corresponds to the two's complement of the shift distance, i.e., a shift code of 11111_2 (-1_{10}) results in a right shift of one position, etc.

When not in the wrap mode, the LSH33 fills bit positions for which there is no corresponding input bit. The fill value and the positions filled depend on the RIGHT/$\overline{\text{LEFT}}$ (R/$\overline{\text{L}}$) direction pin. This pin is a don't care input when in wrap mode. For left shifts in fill mode, lower bits are filled with zero as shown in Table 2. For right shifts, however, the SIGN input is used as the fill value. Table 3 depicts the bits to be filled as a function of shift code for the right shift case. Note that the R/$\overline{\text{L}}$ input changes only the fill convention, and does not affect the definition of the shift code.

LSH33 BLOCK DIAGRAM

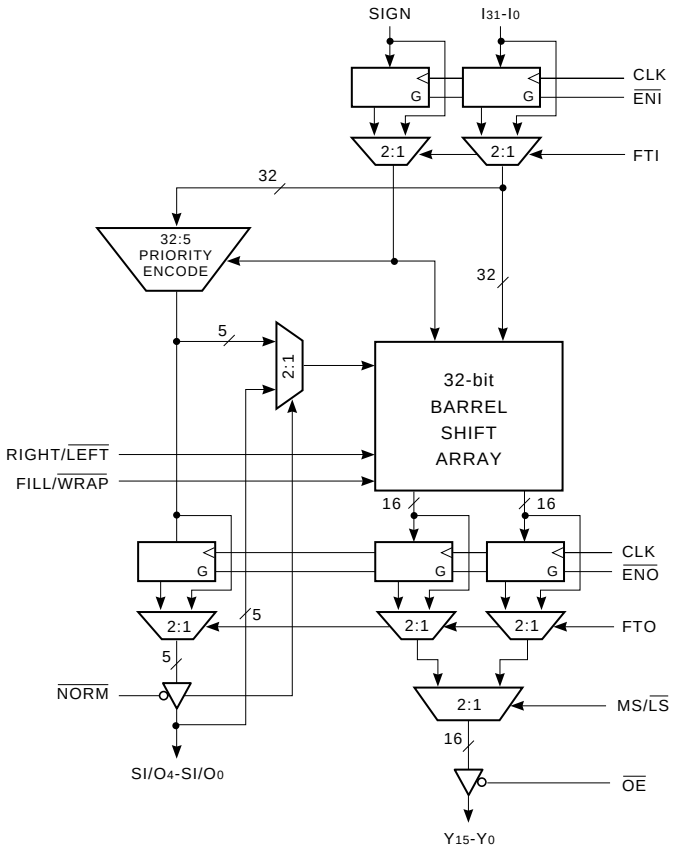


TABLE 1. WRAP MODE SHIFT CODE DEFINITIONS

Shift Code	Y31	Y30	Y29	•••	Y16	Y15	•••	Y2	Y1	Y0
00000	I31	I30	I29	•••	I16	I15	•••	I2	I1	I0
00001	I30	I29	I28	•••	I15	I14	•••	I1	I0	I31
00010	I29	I28	I27	•••	I14	I13	•••	I0	I31	I30
00011	I28	I27	I26	•••	I13	I12	•••	I31	I30	I29
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
01111	I16	I15	I14	•••	I1	I0	•••	I19	I18	I17
10000	I15	I14	I13	•••	I0	I31	•••	I18	I17	I16
10001	I14	I13	I12	•••	I31	I30	•••	I17	I16	I15
10010	I13	I12	I11	•••	I30	I29	•••	I16	I15	I14
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
11100	I3	I2	I1	•••	I20	I19	•••	I5	I5	I4
11101	I2	I1	I0	•••	I19	I18	•••	I5	I4	I3
11110	I1	I0	I31	•••	I18	I17	•••	I4	I3	I2
11111	I0	I31	I30	•••	I17	I16	•••	I3	I2	I1

TABLE 2. FILL MODE SHIFT CODE DEFINITIONS — LEFT SHIFT

Shift Code	Y31	Y30	Y29	•••	Y16	Y15	•••	Y2	Y1	Y0
00000	I31	I30	I29	•••	I16	I15	•••	I2	I1	I0
00001	I30	I29	I28	•••	I15	I14	•••	I1	I0	0
00010	I29	I28	I27	•••	I14	I13	•••	I0	0	0
00011	I28	I27	I26	•••	I13	I12	•••	0	0	0
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
01111	I16	I15	I14	•••	I1	I0	•••	0	0	0
10000	I15	I14	I13	•••	I0	0	•••	0	0	0
10001	I14	I13	I12	•••	0	0	•••	0	0	0
10010	I13	I12	I11	•••	0	0	•••	0	0	0
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
11100	I3	I2	I1	•••	0	0	•••	0	0	0
11101	I2	I1	I0	•••	0	0	•••	0	0	0
11110	I1	I0	0	•••	0	0	•••	0	0	0
11111	I0	0	0	•••	0	0	•••	0	0	0

In fill mode, as in wrap mode, the shift code input represents the number of shift positions directly for left shifts, but the two's complement of the shift code results in the equivalent right shift. However, for fill mode the R/$\overline{L}$ input can be viewed as the most significant bit of a 6-bit two's complement shift code, comprised of R/$\overline{L}$ concatenated with the SI4–SI0 lines. Thus, a positive shift code (R/$\overline{L}$ = 0) results in a left shift of 0–31 positions, and a negative code (R/$\overline{L}$ = 1) a right shift of up to 32 positions. The LSH33 can thus effectively select any contiguous 32-bit field out of a (sign extended and zero filled) 96-bit "input."

OUTPUT MULTIPLEXER

The shift array outputs can be registered and then applied to a 2:1 multiplexer controlled by the MS/$\overline{LS}$ select line. This multiplexer makes available at the output pins either the most significant or least significant 16 outputs of the shift array.

PRIORITY ENCODER

The 32-bit input bus drives a priority encoder which is used to determine the first significant position for purposes of normalization. The priority encoder produces a five-bit code representing the location of the first non-zero bit in the input word. Code assignment is such that the priority encoder output represents the number of shift positions required to left align the first non-zero bit of the input word. Prior to the priority encoder, the input bits are individually exclusive OR'ed with the SIGN input. This allows normalization in floating point systems using two's complement mantissa representation. A negative value in two's complement representation will cause the exclusive OR gates to invert the input data to the encoder. As a result, the leading significant digit will always be "1."

TABLE 3. FILL MODE SHIFT CODE DEFINITIONS — RIGHT SHIFT

Shift Code	Y_{31}	Y_{30}	Y_{29}	•••	Y_{16}	Y_{15}	•••	Y_2	Y_1	Y_0
00000	S	S	S	•••	S	S	•••	S	S	S
00001	S	S	S	•••	S	S	•••	S	S	I_{31}
00010	S	S	S	•••	S	S	•••	S	I_{31}	I_{30}
00011	S	S	S	•••	S	S	•••	I_{31}	I_{30}	I_{29}
.	.	.	.	•••	.	.	•••	.	.	.
.	.	.	.	•••	.	.	•••	.	.	.
.	.	.	.	•••	.	.	•••	.	.	.
01111	S	S	S	•••	S	S	•••	I_{19}	I_{18}	I_{17}
10000	S	S	S	•••	S	I_{31}	•••	I_{18}	I_{17}	I_{16}
10001	S	S	S	•••	I_{31}	I_{30}	•••	I_{17}	I_{16}	I_{15}
10010	S	S	S	•••	I_{30}	I_{29}	•••	I_{16}	I_{15}	I_{14}
.	.	.	.	•••	.	.	•••	.	.	.
.	.	.	.	•••	.	.	•••	.	.	.
.	.	.	.	•••	.	.	•••	.	.	.
11100	S	S	S	•••	I_{20}	I_{19}	•••	I_5	I_5	I_4
11101	S	S	S	•••	I_{19}	I_{18}	•••	I_5	I_4	I_3
11110	S	S	I_{31}	•••	I_{18}	I_{17}	•••	I_4	I_3	I_2
11111	S	I_{31}	I_{30}	•••	I_{17}	I_{16}	•••	I_3	I_2	I_1

TABLE 4. PRIORITY ENCODER FUNCTION TABLE

I_{31}	I_{30}	I_{29}	•••	I_{16}	I_{15}	•••	I_2	I_1	I_0	Shift Code
1	X	X	•••	X	X	•••	X	X	X	00000
0	1	X	•••	X	X	•••	X	X	X	00001
0	0	1	•••	X	X	•••	X	X	X	00010
.	.	.	•••	.	.	•••	.	.	.	.
.	.	.	•••	.	.	•••	.	.	.	.
0	0	0	•••	1	X	•••	X	X	X	01111
0	0	0	•••	0	1	•••	X	X	X	10000
0	0	0	•••	0	0	•••	X	X	X	10001
.	.	.	•••	.	.	•••	.	.	.	.
.	.	.	•••	.	.	•••	.	.	.	.
0	0	0	•••	0	0	•••	0	1	X	11110
0	0	0	•••	0	0	•••	0	0	1	11111
0	0	0	•••	0	0	•••	0	0	0	11111

This affects only the encoder inputs; the shift array always operates on the raw input data. The priority encoder function table is shown in Table 4.

NORMALIZE MULTIPLEXER

The $\overline{\text{NORM}}$ input, when asserted, results in the priority encoder output driving the internal shift code inputs directly. When using the $\overline{\text{NORM}}$ function, the LSH33 should be placed in fill mode, with the R/$\overline{\text{L}}$ input low.

When $\overline{\text{NORM}}$ is high (not asserted), the SI/O_4–SI/O_0 port acts as the shift code input to the shifter.

APPLICATIONS EXAMPLES

Normalization of mantissas up to 32 bits can be accomplished directly by a single LSH33. To do this, the $\overline{\text{NORM}}$ input is asserted, and fill mode and left shift are selected. The normalized mantissa is then available at the device output in two 16-bit segments, under the control of the output data multiplexer select, the MS/$\overline{\text{LS}}$ signal.

If it is desirable to avoid the necessity of multiplexing output data in 16-bit segments, two LSH33 devices can be used in parallel. Both devices receive the same input word, with the MS/$\overline{\text{LS}}$ select line of one wired high, and the other low. Each device will then independently determine the shift distance required for normalization, and the full 32 bits of output data will be available simultaneously.

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature ..... –65°C to +150°C
Operating ambient temperature ..... –55°C to +125°C
VCC supply voltage with respect to ground ..... –0.5 V to +7.0 V
Input signal with respect to ground ..... –3.0 V to +7.0 V
Signal applied to high impedance output ..... –3.0 V to +7.0 V
Output current into low outputs ..... 25 mA
Latchup current ..... > 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	**Temperature Range** (Ambient)	**Supply Voltage**
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ **V**CC ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ **V**CC ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	**Parameter**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**
VOH	Output High Voltage	**V**CC = Min., **I**OH = –2.0 mA	2.4			V
VOL	Output Low Voltage	**V**CC = Min., **I**OL = 8.0 mA			0.4	V
VIH	Input High Voltage		2.0		**V**CC	V
VIL	Input Low Voltage	(Note 3)	0.0		0.8	V
IIX	Input Current	Ground ≤ **V**IN ≤ **V**CC (Note 12)			±20	µA
IOZ	Output Leakage Current	Ground ≤ **V**OUT ≤ **V**CC (Note 12)			±20	µA
ICC1	**V**CC Current, Dynamic	(Notes 5, 6)		10	30	mA
ICC2	**V**CC Current, Quiescent	(Note 7)			1.5	mA

SWITCHING CHARACTERISTICS — COMMERCIAL OPERATING RANGE (0°C to +70°C)

GUARANTEED MAXIMUM COMBINATIONAL DELAYS *Notes 9, 10 (ns)*

To Output / From Input	LSH33-40*		LSH33-30		LSH33-20*	
	Y_{15}-Y_0	SO_4-SO_0	Y_{15}-Y_0	SO_4-SO_0	Y_{15}-Y_0	SO_4-SO_0
FTI = 0, FTO = 0						
CLK	28	28	24	24	15	15
MS/$\overline{LS}$	28	—	24	—	15	—
FTI = 0, FTO= 1						
CLK ($\overline{NORM}$ = 0/1)	73 / 40	55 / —	58 / 30	42 / —	20 / 20	20 / —
SI_4-SI_0	52	—	40	—	20	—
R/$\overline{L}$, F/$\overline{W}$	52	—	40	—	20	—
MS/$\overline{LS}$	28	—	24	—	15	—
FTI = 1, FTO = 0						
CLK	28	28	24	24	15	15
MS/$\overline{LS}$	28	—	24	—	15	—
FTI = 1, FTO = 1						
I_{31}-I_0, SIGN ($\overline{NORM}$ = 0/1)	73 / 40	55 / —	58 / 30	42 / —	20 / 20	20 / —
SI_4-SI_0	52	—	40	—	20	—
R/$\overline{L}$, F/$\overline{W}$	52	—	40	—	20	—
MS/$\overline{LS}$	28	—	24	—	15	—

GUARANTEED MINIMUM SETUP AND HOLD TIMES WITH RESPECT TO CLOCK RISING EDGE *Notes 9, 10 (ns)*

	LSH33-40*				LSH33-30				LSH33-20*			
	FTI = 0		FTI = 1		FTI = 0		FTI = 1		FTI = 0		FTI = 1	
Input	**Setup**	**Hold**	**Setup**	**Hold**	**Setup**	**Hold**	**Setup**	**Hold**	**Setup**	**Hold**	**Setup**	**Hold**
I_{31}-I_0, SIGN	12	3	20	2	10	3	15	2	8	0	8	2
SI_4-SI_0	17	0	17	0	15	0	15	0	8	0	8	0
R/$\overline{L}$, F/$\overline{W}$	12	0	12	0	10	0	10	0	8	0	8	0
$\overline{ENI}$, $\overline{ENO}$	12	0	12	0	10	0	10	0	8	0	8	0

TRI-STATE ENABLE/DISABLE TIMES *Notes 9, 10, 11 (ns)*

	LSH33-40*	LSH33-30	LSH33-20*
t_{ENA}	20	17	15
t_{DIS}	20	17	15

CLOCK CYCLE TIME AND PULSE WIDTH *Notes 9, 10 (ns)*

	LSH33-40*	LSH33-30	LSH33-20*
Minimum Cycle Time	30	20	15
Highgoing Pulse	12	9	7
Lowgoing Pulse	12	9	7

*DISCONTINUED SPEED GRADE

SWITCHING CHARACTERISTICS — MILITARY OPERATING RANGE (–55°C to +125°C)

GUARANTEED MAXIMUM COMBINATIONAL DELAYS *Notes 9, 10 (ns)*

To Output / From Input	LSH33-50*		LSH33-40*		LSH33-30*	
	Y_{15}-Y_0	SO_4-SO_0	Y_{15}-Y_0	SO_4-SO_0	Y_{15}-Y_0	SO_4-SO_0
FTI = 0, FTO = 0						
CLK	32	32	28	28	24	24
MS/$\overline{LS}$	32	—	28	—	24	—
FTI = 0, FTO= 1						
CLK ($\overline{NORM}$ = 0/1)	80 / 50	65 / —	73 / 40	55 / —	58 / 30	42 / —
SI_4-SI_0	62	—	52	—	40	—
R/$\overline{L}$, F/$\overline{W}$	62	—	52	—	40	—
MS/$\overline{LS}$	32	—	28	—	24	—
FTI = 1, FTO = 0						
CLK	32	32	28	28	24	24
MS/$\overline{LS}$	32	—	28	—	24	—
FTI = 1, FTO = 1						
I_{31}-I_0, SIGN ($\overline{NORM}$ = 0/1)	80 / 50	65 / —	73 / 40	55 / —	58 / 30	42 / —
SI_4-SI_0	62	—	52	—	40	—
R/$\overline{L}$, F/$\overline{W}$	62	—	52	—	40	—
MS/$\overline{LS}$	62	—	28	—	24	—

GUARANTEED MINIMUM SETUP AND HOLD TIMES WITH RESPECT TO CLOCK RISING EDGE *Notes 9, 10 (ns)*

	LSH33-50*				LSH33-40*				LSH33-30*			
	FTI = 0		FTI = 1		FTI = 0		FTI = 1		FTI = 0		FTI = 1	
Input	**Setup**	**Hold**	**Setup**	**Hold**	**Setup**	**Hold**	**Setup**	**Hold**	**Setup**	**Hold**	**Setup**	**Hold**
I_{31}-I_0, SIGN	15	3	20	2	12	3	20	2	10	0	15	2
SI_4-SI_0	20	0	20	0	17	0	17	0	15	0	15	0
R/$\overline{L}$, F/$\overline{W}$	15	0	15	0	12	0	12	0	10	0	10	0
$\overline{ENI}$, $\overline{ENO}$	15	0	15	0	12	0	12	0	10	0	10	0

TRI-STATE ENABLE/DISABLE TIMES *Notes 9, 10, 11 (ns)*

	LSH33-50*	LSH33-40*	LSH33-30*
t_{ENA}	22	20	17
t_{DIS}	22	20	17

CLOCK CYCLE TIME AND PULSE WIDTH *Notes 9, 10 (ns)*

	LSH33-50*	LSH33-40*	LSH33-30*
Minimum Cycle Time	35	30	20
Highgoing Pulse	15	12	9
Lowgoing Pulse	15	12	9

*DISCONTINUED SPEED GRADE

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

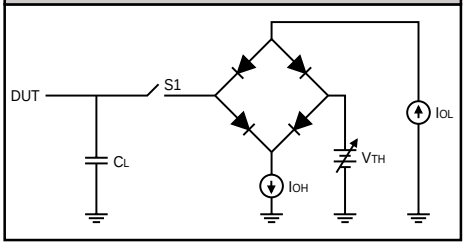
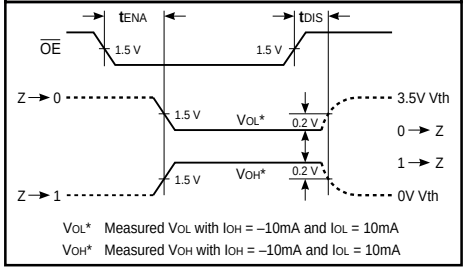
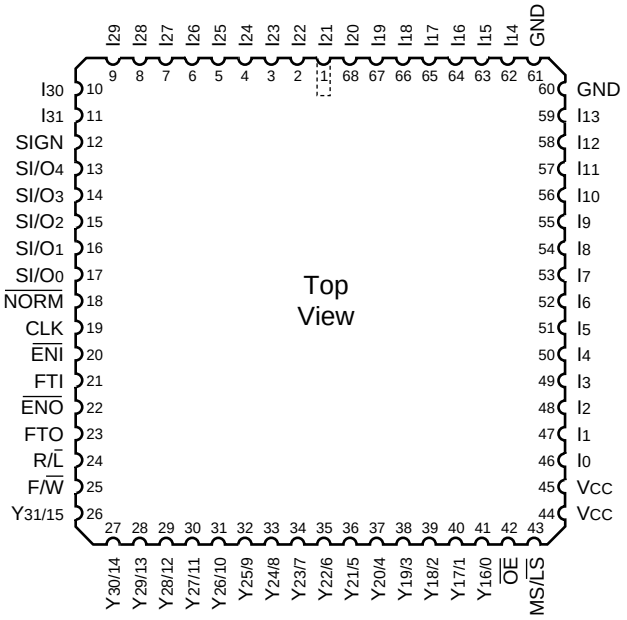


FIGURE B. THRESHOLD LEVELS

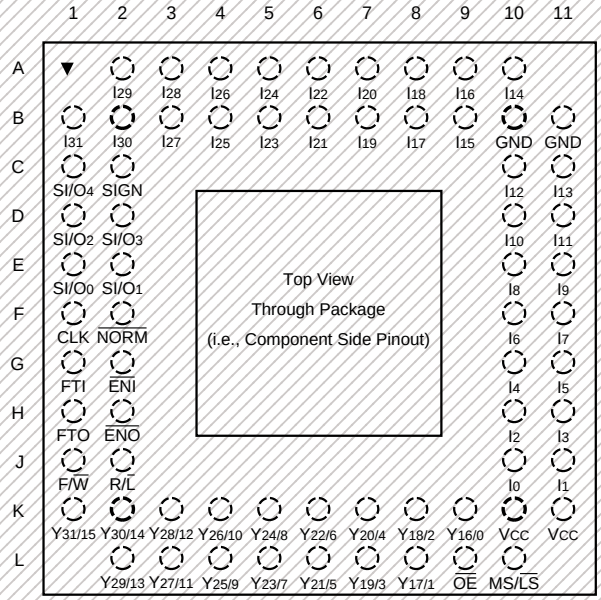


ORDERING INFORMATION

68-pin



68-pin



Discontinued Package

Speed	Plastic J-Lead Chip Carrier (J2)		Ceramic Pin Grid Array (G1)
	0°C to +70°C — COMMERCIAL SCREENING		
30 ns	LSH33JC30		
	–55°C to +125°C — COMMERCIAL SCREENING		
	–55°C to +125°C — MIL-STD-883 COMPLIANT		