4.   DSP RAM ACCESS

The modem DSP contains a 16-bit wide random access memory (RAM). The host processor can access (read or write) the RAM through a 12-bit memory address in registers 1D and 1C.

4.1.   INTERFACE MEMORY ACCESS TO DSP RAM

The interface memory acts as an intermediary during host to DSP RAM or DSP RAM to host data exchanges. The address stored in interface memory RAM address registers MEADDH and MEADDL by the host is the DSP RAM address for data access. The data is transferred through data registers MEDAM and MEDAL.

One or two bytes (1 byte = 8 bits) are transferred between DSP RAM and DSP interface memory once each device cycle. The DSP operates at a 7200 Hz sample rate.

The RAM access bit (MEACC) in the interface memory instructs the DSP to access the RAM. The transfer is initiated by the host setting the MEACC bit. The DSP tests this bit each sample period.

RAM can be accessed using one of four methods:

1.   8-bit read - 8-bit write.

2.   16-bit read - 8-bit write.

3.   16-bit read - 16-bit write.

4.   16-bit read only (modem diagnostics).

Parameters transferred under the first method have only 8 bits of significance. The data is written to and read from MEDAL. Data in MEDAM is ignored.

Parameters transferred using the second method have 16 bits of significance but can be written only 8 bits at a time. These parameters have two access codes associated with them, one for the least significant 8-bits and one for the most significant 8 bits. The host need read only the low address to obtain both the most significant and the least significant bytes of the data if the two access codes are in consecutive order.

Parameters transferred using the third method involve 16-bit read or write operations using one access code.

Finally, all diagnostic read operations using the fourth method use only one access code. Data is read from MEDAM and MEDAL.

The parameters available in DSP RAM are listed in Table 4-1.

4.2.   HOST DSP READ AND WRITE PROCEDURES

DSP RAM Write Procedure

1.   Set MEMW to inform the DSP that a RAM write will occur when MEACC is set.

2.   Load the RAM address into the MEADDH and MEADDL registers.

3.   Write the desired data into the interface memory RAM data registers MEDAM and/or MEDAL.

4.   Set MEACC to signal the DSP to perform the RAM write.

5.   When the DSP has transferred the contents of the interface memory RAM data registers into RAM, the modem resets the MEACC bit and sets the NEWS bit to indicate DSP RAM write completion. If the NSIE bit is a 1, IRQ is asserted and NSIA is set to inform the host that setting of the NEWS bit is the source of the interrupt request.

6.   Upon the completion of IRQ servicing, write a 0 into the NEWS bit to clear the NSIA bit and to negate IRQ if no other interrupt requests are pending.

DSP RAM Read Procedure

1.   Reset MEMW to inform the DSP that a RAM read will occur when MEACC is set.

2.   Load the RAM address code into the MEADDH and MEADDL registers.

3.   Set MEACC to signal the DSP to perform the RAM read.

4.   When the DSP has transferred the contents of RAM into the interface memory RAM data registers MEDAM and/or MEDAL, the modem resets the MEACC bit and sets the NEWS bit to indicate DSP RAM read completion. If the NSIE bit is a 1, IRQ is asserted and NSIA is set to inform the host that setting of the NEWS bit is the source of the interrupt request.

6.   Upon the completion of IRQ servicing, write a 0 into the NEWS bit to clear the NSIA bit and to negate IRQ if no other interrupt requests are pending.

4.3.   RAM READ AND WRITE EXAMPLES

Figure 4-1 shows a flowchart of a procedure to change the DTMF tone duration using method 1.

Figure 4-2 shows a flowchart of a procedure to change the RTS-CTS delay using method 2.

Figure 4-3 shows a flowchart of a procedure to change the THRESHU value for TONEA using method 3.

Figure 4-4 shows a flowchart of a procedure to read EQM using method 4.

Table 4-1.   Interface Memory RAM Addresses

No.	Function	Method	Address (Hex)
1	Transmitter Compromise Equalizer Coefficients		
	First Coefficient Tap	3	AE8
	Last Coefficient Tap	3	AD0
	Number of Taps	3	B47
2	Rate Sequence		
	Received R	4	208
	Received E	4	20A
	Transmitted R	2 (RO)	204, 205 (see Note 1)
	Transmitted E	2 (RO)	206, 207 (see Note 1)
	V.32/V.32 bis R1 Mask	2	2C0, 2C1 (see Note 1)
	V.32/V.32 bis R2 Mask	2	2C2, 2C3 (see Note 1)
	V.32 bis R4 Mask	2	2C4, 2C5 (see Note 1)
	V.32 bis R5 Mask	2	2C6, 2C7 (see Note 1)
	V.33 R33 Mask	2	2C8, 2C9 (see Note 1)
3	DTMF Tone Duration	2	218, 2DB (see Note 1)
4	DTMF Interdigit Delay	2	219, 2DC (see Note 1)
5	DTMF Low Band Power Level	2	29B, 29C (see Note 1)
6	DTMF High Band Power Level	2	29D, 29E (see Note 1)
7	Pulse Relay Make Time	1	22C
8	Pulse Relay Break Time	1	21C
9	Pulse Interdigit Delay	2	21A, 21B
10	Calling Tone On Time	2	290, 2D9 (see Note 1)
11	Calling Tone Off Time	2	291, 2DA (see Note 1)
12	Transmitter Output Level Gain (G)		
	Transmitter Output Level Gain (G) - All Modes	3	A48
	Transmitter Output Level Gain (G) - FSK Modes	3	B57
13	Dual Tone 1 Frequency	2	280, 281 (see Note 1)
14	Dual Tone 2 Frequency	2	282, 283 (see Note 1)
15	Dual Tone 1 Power Level	2	284, 285 (see Note 1)
16	Dual Tone 2 Power Level	2	286, 287 (see Note 1)
17	New Status (NEWS) Masking Registers		
	Masking Register for 01	1	247
	Masking Register for 0A and 0B	2	246, 245
	Masking Register for 0C and 0D	2	244, 243
	Masking Register for 0E and 0F	2	242, 241
	Masking Register for 12 (set bit 7 to enable interrupt)	1	089 (bit 7)
	Masking Register for 14	1	38A
	Masking Register for 16	1	370
	Masking Register for 17	1	371
	Masking Register for 1A and 1B	2	27D, 27C
	Masking Register for Memory Access		
	(Set bit 6 to disable interrupt)	1	089 (bit 6)
22	Far-End Echo Frequency Offset	4	852
23	Far-End Echo Level	4	B52
24	CTS OFF-to-ON Response Time (RTS–CTS Delay)	2	202, 203 (see Note 1)
25	Answer Tone Length	2	228, 229 (see Note 1)
26	Silence after Answer Tone Period	2	22A, 22B (see Note 1)
27	Tone Detector A Bandpass Filter Coefficients	3	See Table 4-6
28	Tone Detector B Bandpass Filter Coefficients	3	See Table 4-6
29	Tone Detector C Bandpass Filter Coefficients	3	See Table 4-6
30	RLSD Drop Out Timer	1	270 and 271
31	RLSD Turn-On Threshold (RLSD_ON)	2	134, 135
32	RLSD Turn-Off Threshold (RLSD_OFF)	2	136, 137
	RLSD Threshold Offset	2	138, 139
	RLSD Overwrite Control	1	10D (Bit 2)
	Extended RTH Control	1	10D (Bit 6)
	Receiver Gain	1	A03
	Receiver Threshold	3	A04, A05
	RTH0 Offset	2	2D0, 2D1 (see Note 1)
	RTH1 Offset	2	2D2, 2D3 (see Note 1)
	RTH2 Offset	2	2D4, 2D5 (see Note 1)
	RTH3 Offset	2	2D6, 2D7 (see Note 1)

Table 4-1.   Interface Memory RAM Addresses (Cont'd)

No.	Function	Method	Address (Hex)
34	V.32 PN Length	2	288, 289 (see Note 1)
36	AGC Gain Word	4	A00
37	Round Trip Far Echo Delay	4	239
45	Equalizer Frequency Correction	4	811
46	Eye Quality Monitor (EQM)	4	20C
47	Maximum Period of Valid Ring Signal	1	21F
48	Minimum Period of Valid Ring Signal	1	21E
49	Phase Jitter Frequency	4	80E
50	Phase Jitter Amplitude	4	80D
51	Guard Tone Level	3	B46
52	CCITT CRC 32 Select	1	0B3
53	Secondary Channel Transmitter Speed Select	1	28E
	Secondary Channel Receiver Speed Select	1	28B
58	V.FC Automatic Carrier Select (ACS)	1	13F (bit 4)
	V.FC Carrier Deviation Negotiation (CDN)	1	100 (bit 4)
	V.FC Carrier Deviation Offset	1	10A
59	V.FC Carrier Bias	1	212
60	V.34/V.FC Symbol Rate Value	1	2E3
61	V.34/V.FC Baud Rate Mask (BRM)	1	101
62	V.34/V.FC Pre-Emphasis Value	4	B44
63	V.34/V.FC Pre-Emphasis Override	1	0E6
	V.34/V.FC Pre-Emphasis Disable (PREDIS)	1	100 (bit 1)
64	V.34/V.FC Transmit Level Deviation Disable (TLDDIS)	1	100 (bit 3)
65	V.FC Transmit Level Deviation Bias	1	216
68	EQM Above Threshold	1	133
69	EQM Scale Factor (Gain)	3	A29
	EQM ARA Bias (Offset)	2	2A4, 2A5
70	V.21/V.23 CTS Mark Qualify	1	10D (bit 3)
71	V.FC Symbol Rate Offset	1	13B and 13C
72	V.FC Data Rate Sequence Mask	2	116, 117
73	No Automode to FSK	1	13F (bit 0)
74	Receive FIFO Trigger Level	1	32C
75	V.FC GSTN Cleardown Option	1	10D (bit 4)
81	V.34 Spectral Parameters Control	1	105
82	V.34 Phase 2 Power Reduction	1	0E2
83	V.34 Low Band Symbol Rate Edge Estimate Offset	1	13B
	V.34 High Band Symbol Rate Edge Estimate Offset	1	13C
84	V.34 Receiver Speed Indication	1	384
85	V.34 Data Rate Mask	2	382, 383
86	V.34 Asymmetric Data Rates Enable	1	13F Bit 6
87	V.34 Remote Mode Data Rate Capability	2 (RO)	208, 209
	V.34 Remote Modem Asymmetric Data Rate Indicator	1 (RO)	209 Bit 7

■ 7811073 0024603 22T ■

Table 4-1.   Interface Memory RAM Addresses (Cont'd)

No.	Function	Method	Address (Hex)
88	V.8 Status Registers - See Section 9		
	V.8 Status Register 1	1	301
	V.8 Status Register 2	1	302
	V.8 Status Register 3	1	303
89	V.8 Control Registers - See Section 9		
	V.8 Control Register 1	1	304
	V.8 Control Register 2	1	305
	V.8 Control Register 3	1	306
	V.8 Control Register 4	1	307
	V.8 Control Register 5	1	308
90	Modulation Modes- See Section 9		
	V.34 Full-Duplex configuration - See Section 9	1	309
	V.32bis configuration	1	30B
	V.22 bis configuration	1	30C
	V.17 configuration	1	30D
	V.29 configuration	1	30E
	V.27 configuration	1	30F
	V.26 ter configuration	1	310
	V.26 bis configuration	1	311
	V.23 Full-Duplex configuration	1	312
	V.23 Half-Duplex configuration	1	313
	V.21 configuration	1	314
	V.FC configuration	1	315
91	V.8 MaxFrameByteCount- See Section 9	1	31C
92	V.8 Call Functions- See Section 9	1	32A
93	CM/JM/CI Frame - See Section 9		
	SYNC CM/JM/CI	1	32D
	Data Call Function	1	32E
	modulation 0	1	32F
	modulation 1	1	330
	modulation 2	1	331
	Protocol (optional)	1	332
	GSTN (optional)	1	333
	Frame End	1	334
100	Minimum On Time (DTMF)	3	A78
101	Minimum Off Time (DTMF)	3	878
102	Minimum Cycle Time (DTMF)	3	978
103	Minimum Dropout Time (DTMF)	3	B78
104	Maximum Speech Energy (DTMF	3	A77
105	Frequency Deviation, Low Group (DTMF)	3	876
106	Frequency Deviation, High Group (DTMF)	3	A76
107	Negative Twist Control, TWIST4 (DTMF)	3	977
108	Positive Twist Control, TWIST8 (DTMF)	3	877
109	Maximum Energy Hit Time (DTMF)	3	A67
110	ADC Speech Sample Scaling Parameter, ADCS (ADPCM)	3	BD1
111	White Noise Output Scaling Parameter, RANOISE (ADPCM)	3	A35
112	Minimum Silence Magnitude Threshold, MTHRESH (ADPCM)	3	A36
113	Detecting Silence in Speech Parameter, SILSPE (ADPCM)	3	B37
114	Detecting Speech in Silence Parameter, SPESIL (ADPCM)	3	B38
115	Minimum Silence Magnitude Adaptation Parameter, MADAPT (ADPCM)	3	B39

Notes:

1.   High address = MSB of data; low address = LSB of data.

2.   The host may access only the X or Y data on any given read cycle, i.e., X and Y data cannot be accessed simultaneously.
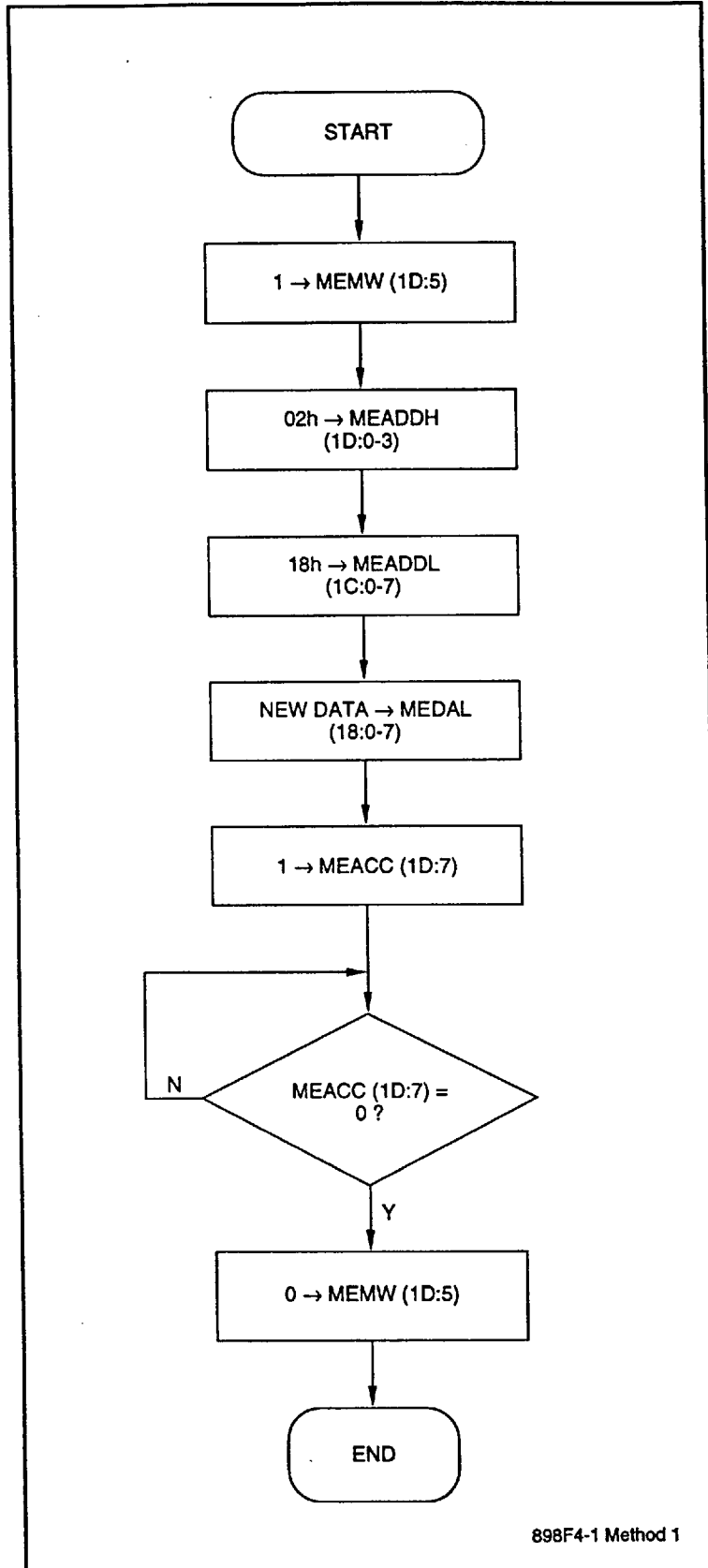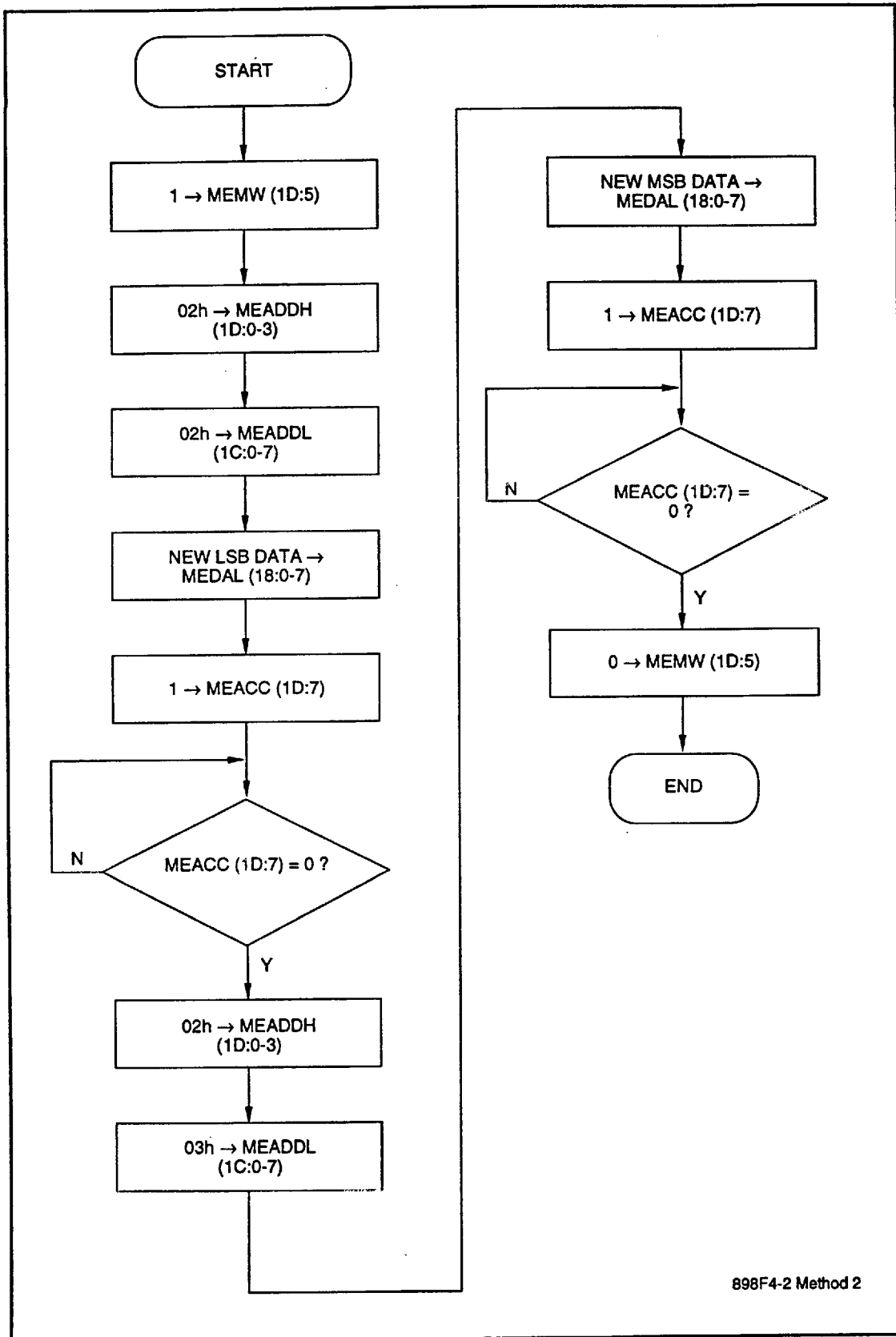
3.   RO = read-only.

```
                    ╭──────────────╮
                    │    START     │
                    ╰──────┬───────╯
                           │
                           ▼
               ┌───────────────────────┐
               │    1 → MEMW (1D:5)     │
               └───────────┬───────────┘
                           │
                           ▼
               ┌───────────────────────┐
               │    02h → MEADDH        │
               │      (1D:0-3)          │
               └───────────┬───────────┘
                           │
                           ▼
               ┌───────────────────────┐
               │    18h → MEADDL        │
               │      (1C:0-7)          │
               └───────────┬───────────┘
                           │
                           ▼
               ┌───────────────────────┐
               │  NEW DATA → MEDAL      │
               │      (18:0-7)          │
               └───────────┬───────────┘
                           │
                           ▼
               ┌───────────────────────┐
               │    1 → MEACC (1D:7)    │
               └───────────┬───────────┘
                           │
         ┌─────────────────┤
         │                 ▼
         │            ╱─────────╲
         │           ╱  MEACC    ╲
         │ N        ╱  (1D:7) =    ╲
         └─────────│     0 ?        │
                    ╲             ╱
                     ╲           ╱
                      ╲─────────╱
                           │ Y
                           ▼
               ┌───────────────────────┐
               │    0 → MEMW (1D:5)     │
               └───────────┬───────────┘
                           │
                           ▼
                    ╭──────────────╮
                    │     END      │
                    ╰──────────────╯
```

898F4-1 Method 1

Figure 4-1.   Method 1 Example - Changing DTMF Tone Duration (LSB)

Figure 4-2. Method 2 Example - Changing RTS-CTS Delay

START

1 → MEMW (1D:5)
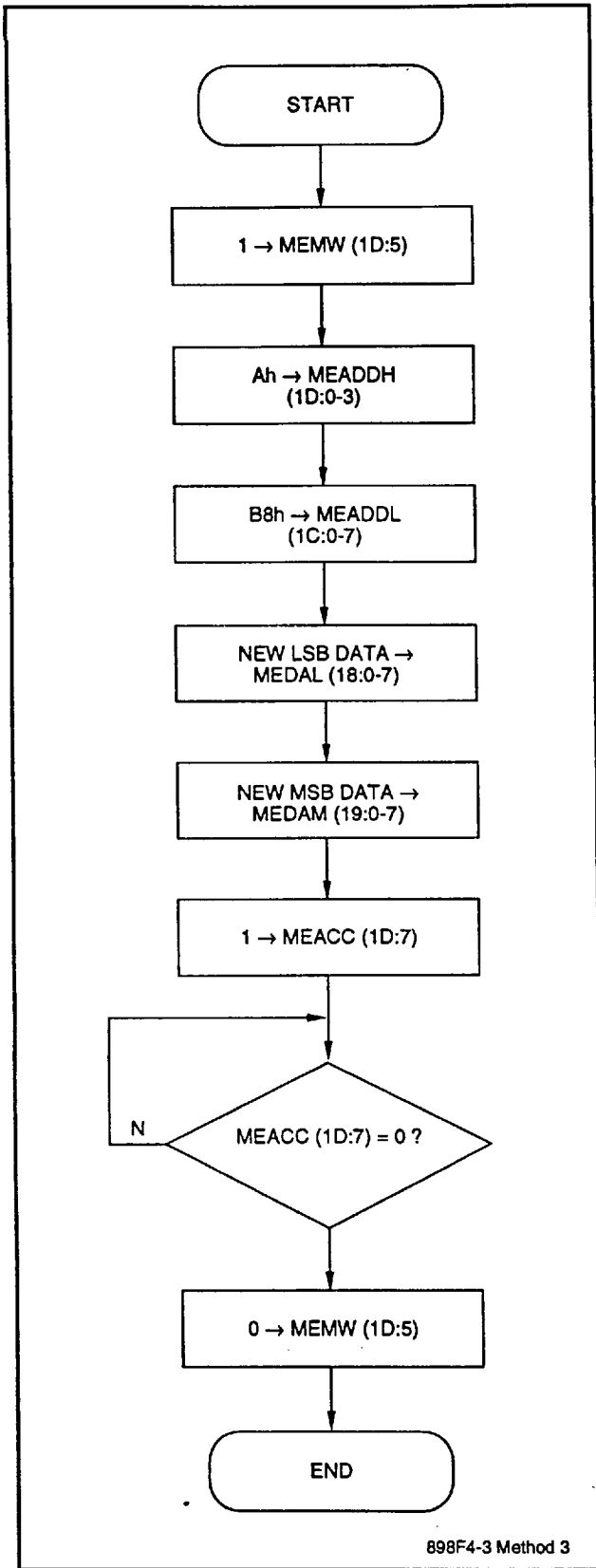
02h → MEADDH (1D:0-3)

02h → MEADDL (1C:0-7)

NEW LSB DATA → MEDAL (18:0-7)

1 → MEACC (1D:7)

MEACC (1D:7) = 0 ?
N
Y

02h → MEADDH (1D:0-3)

03h → MEADDL (1C:0-7)

NEW MSB DATA → MEDAL (18:0-7)

1 → MEACC (1D:7)

MEACC (1D:7) = 0 ?
N
Y

0 → MEMW (1D:5)

END

898F4-2 Method 2

Figure 4-3. Method 3 Example - Changing TONEA
THRESHU

Flowchart (Method 3):

START → 1 → MEMW (1D:5) → Ah → MEADDH (1D:0-3) → B8h → MEADDL (1C:0-7) → NEW LSB DATA → MEDAL (18:0-7) → NEW MSB DATA → MEDAM (19:0-7) → 1 → MEACC (1D:7) → MEACC (1D:7) = 0 ? (N loops back) → 0 → MEMW (1D:5) → END

898F4-3 Method 3
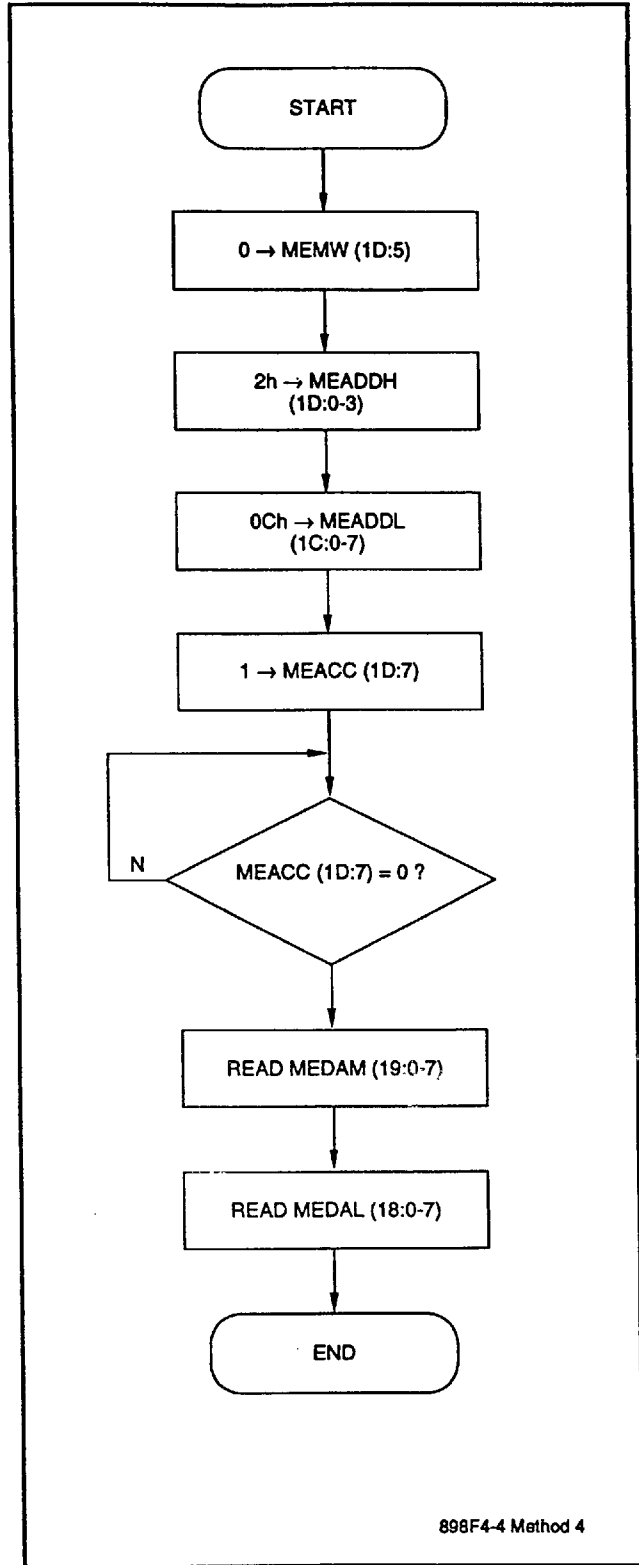
Figure 4-4. Method 4 Example - Reading EQM

Flowchart (Method 4):

START → 0 → MEMW (1D:5) → 2h → MEADDH (1D:0-3) → 0Ch → MEADDL (1C:0-7) → 1 → MEACC (1D:7) → MEACC (1D:7) = 0 ? (N loops back) → READ MEDAM (19:0-7) → READ MEDAL (18:0-7) → END

898F4-4 Method 4

4.4. DSP RAM DATA SCALING

Function 1A: Transmitter Compromise Equalizer Coefficients   **Acc. Method: 3**   **Addr.: AD0-AE8**
Function 1B: Number of Taps   **Acc. Method: 3**   **Addr.: B47**

The transmitter compromise equalizer can be programmed by the host in modes other than V.34, V.FC, V.32 bis/V.32, or FSK. The equalizer is a 25-tap finite impulse response (FIR) digital filter. The first tap is at address AE8h (h denotes a hexadecimal number) and the last tap is at AD0h. The sampling rate for the filter is 7200 Hz. New coefficients should be loaded while the modem is in idle mode before turning on DTR (2-wire full-duplex modes) or RTS (4-wire full-duplex modes). The coefficients have to be loaded only once. They are re-initialized to the default values only if a POR occurs. The user should ensure that the overall gain of any filter designed is 1. Set NEWC after new taps have been loaded.

    Format: 16-bit, signed, 2s complement

Function 2:   V.32 bis and V.33 Rate Sequence   **Acc Method: Table 4-1**   **Addr. 208-2C9**

V.32 bis Rate Sequence Bits. CCITT defines the V.32 bis rate sequence bits as follows:

BIT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DATA	0	0	0	0	1	X	X	1	1	X	X	1	X	0	0	1

B0 = MSB; B15 = LSB

Bit	Description
B0-B3, B7, B11, B15	For synchronizing on rate signal
B4	-A 1 (Note 1)
B8	-A 1 (Note 1)
B5	A 1 denotes the ability to receive at 4800 bps
B6	A 1 denotes the ability to receive at 9600 bps
B9	A 1 denotes the ability to receive at 7200 bps
B10	A 1 denotes the ability to receive at 12000 bps
B12	A 1 denotes the ability to receive at 14400 bps
B13, B14	0,0 (Note 2)
Notes	
1. When B4 or B8 is set to zero in a transmitted or received rate signal, then interworking can proceed only in accordance with Recommendation V.32.	
2. B13 and B14 shall be set to zero when transmitting and ignored during the reception of a rate signal; they are reserved for future definition by the CCITT and must not be used by the manufacturers.	
3. B4-B6, B9-B10, B12 set to zero calls for a GSTN Cleardown.	

V.32 Rate Sequence Bits. CCITT defines the V.32 rate sequence bits as follows:

BIT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DATA	0	0	0	0	1	X	X	1	1	X	X	1	X	0	0	1

B0 = MSB; B15 = LSB

Bit	Description
B0-B3, B7, B11, B15	For synchronizing on the rate sequence
B4	A 1 denotes the ability to receive at 2400 bps
B5	A 1 denotes the ability to receive at 4800 bps
B6	A 1 denotes the ability to receive at 9600 bps
B4-B6	0 0 0 calls for a GSTN clear down
B8	A 1 denotes the ability of trellis encoding and decoding at the highest data rate indicated in B3-B6.
B9-B14	0 0 1 0 0 0 denotes absence of special operational modes.
Note	
When using the modem in a 7200 bps or 12000 bps proprietary configuration, B9 = 1 denotes the ability to receive at 7200 bps and B10 = 1 denotes the ability to receive at 12000 bps.	

V.33 Rate Sequence Bits. CCITT defines the V.33 rate sequence bits as follows:

For B14 = 0:

BIT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DATA	0	0	C	0	X	X	X	1	X	X	X	1	X	X	0	1

B0 = MSB; B15 = LSB

Bit	Description
B0-B3, B7, B11, B15	For synchronizing on the rate sequence
B4-B6, B10, B12, B13	Not defined
B8	A 1 denotes the ability to receive at 12000 bps
B9	A 1 denotes the ability to receive at 14400 bps

For B14 = 1:

BIT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DATA	0	0	0	0	X	X	X	1	X	X	X	1	X	X	1	1

B0 = MSB; B15 = LSB

Bit	Description
B0-B3, B7, B11, B15	For synchronizing on the rate sequence
B4, B5	A 00 denotes that B6, B10, B12, and B13 define multiplexer configuration selection
B8	A 1 denotes the ability to transmit and receive at 12000 bps
B9	A 1 denotes the ability to transmit and receive at 14400 bps
B6, B10, B12, B13	Multiplexer configuration selection (see the V.33 specification for multiplexer configurations)

The V.32 and V.33 rate sequences contain undefined codes and/or bits. The user can use these bits to convey information to the remote modem during training (e.g., remote configuration, multiplexer configuration, test mode configuration, etc.).

The 16-bit rate sequence word in the modem's RAM corresponds exactly to the 16-bit rate sequences defined in V.32 and V.33. The MSB of the word in RAM is B0 of the rate sequence and the LSB is B15 of the rate sequence.

V.32/V.32 bis Rate Sequence

The V.32/V.32 bis rate sequence is available in RAM during the handshake when the RSEQ bit is a 1. The RSEQ bit will turn on when the E-sequence is available as well. The rate sequence(s) and E-sequence are read from two different RAM locations (see Table 4-1, Function 2). The RSEQ bit must be reset by the host after reading the rate sequence(s).

The host may modify the rate sequence in one of two ways.

Method 1 Description. The first and simplest method is to use the rate sequence mask (see Table 4-1, function 2). The rate sequence masks are available for R1, R2, R4, and R5. Rate sequences R1 and R2 are used during the initial handshake and retrains; R4 and R5 are used during rate renegotiations. The mask written to the appropriate RAM location will be logically ANDed to the out-going rate sequence. A power-on-reset will clear the masks to FFFFh.

Example of Method 1. To request or limit the modem speed to 9600 bps, the host would write 0B91h (see page 4-8 for rate sequence bit assignments) to address 2C0, 2C1 if R1 is to be modified. The same value could be written to address 2C4, 2C5 if R4 is to be modified to limit the speed during a rate renegotiation. The available rates of the remote must be considered by the host before limiting speeds. If the modem determines no common rate is available between both modems during a rate change, the modem will send a clear down and turn off RLSD.

Method 2 Description. The second method for modifying the rate sequence is compatible with the RC144DP and is accomplished through address 204, 205. R1 and R3 are sent by the answering modem and R2 is sent by the originating modem.

To modify R1, the host must write a 0 at this address then wait for the value to equal non-zero. The host then has 1.5 seconds to change R1 (through address 204, 205) before it is sent.

To modify R2, the host must wait until the RSEQ bit is set to a 1 by the DSP. The host then has 1.5 seconds to modify R2 (through address 204, 205).

To modify R3, the host must wait until the RSEQ bit is set to a 1 by the DSP, then change R3 (through address 204, 205).

In the case of rate renegotiations, R4 (sent by the requesting modem) is modified in the same manner as R3 after setting the RREN bit. R5 (sent by the responding modem) is also modified in the same manner after RREDT is set. The host has approximately 5 ms to modify R4 or R5 after the value in address 204, 205 equals zero.

Typical rate sequences and E sequences shown in Table 4-2 and 4-3. The ARC bit is set on both modems. R1 and R3 are read on the originating modem, R2 is read on the answering modem. Refer to Section 5.3 of CCITT Recommendation V.32/V.32 bis for additional information on the V.32/V.32 bis rate sequence.

Table 4-2. R and E Rate Sequences - V.32 to V.32 (V32BS = 0)

Originate Set at	R1 (Hex)	R2 (Hex)	R3 (Hex)	E (Hex) (ANS and ORG)	Answering Configuration	Resulting Configuration
V.32T/9600	0791	0791	0391	F391	V.32T/9600	V.32T/9600
	0711	0711	0311	F311	V.32/9600	V.32/9600
	0511	0511	0511	F511	V.32/4800	V.32/4800
V.32/9600	0791	0711	0311	F311	V.32T/9600	V.32/9600
	0711	0711	0311	F311	V.32/9600	V.32/9600
	0511	0511	0511	F511	V.32/4800	V.32/4800
V.32/4800	0791	0511	0511	F511	V.32T/9600	V.32/4800
	0711	0511	0511	F511	V.32/9600	V.32/4800
	0511	0511	0511	F511	V.32/4800	V.32/4800

Table 4-3. R and E Rate Sequences - V.32 bis to V.32 bis (V32BS = 1)

Originate Set at	R1 (Hex)	R2 (Hex)	R3 (Hex)	E (Hex) (ANS and ORG)	Answering Configuration	Resulting Configuration
V.32T/14400	0FF9	0FF9	0999	F999	V.32T/14400	V.32T/14400
	0FF1	0FF1	09B1	F9B1	V.32T/12000	V.32T/12000
	0FD1	0FD1	0B91	FB91	V.32T/9600	V.32T/9600
	0DD1	0DD1	09D1	F9D1	V.32T/7200	V.32T/7200
	0D91	0D91	0D91	FD91	V.32/4800	V.32/4800
V.32T/12000	0FF9	0FF1	09B1	F9B1	V.32T/14400	V.32T/12000
	0FF1	0FF1	09B1	F9B1	V.32T/12000	V.32T/12000
	0FD1	0FD1	0B91	FB91	V.32T/9600	V.32T/9600
	0DD1	0DD1	09D1	F9D1	V.32T/7200	V.32T/7200
	0D91	0D91	0D91	FD91	V.32/4800	V.32/4800
V.32T/9600	0FF9	0FD1	0B91	FB91	V.32T/14400	V.32T/9600
	0FF1	0FD1	0B91	FB91	V.32T/12000	V.32T/9600
	0FD1	0FD1	0B91	FB91	V.32T/9600	V.32T/9600
	0DD1	0DD1	09D1	F9D1	V.32T/7200	V.32T/7200
	0D91	0D91	0D91	FD91	V.32/4800	V.32/4800
V.32T/7200	0FF9	0DD1	09D1	F9D1	V.32T/14400	V.32T/7200
	0FF1	0DD1	09D1	F9D1	V.32T/12000	V.32T/7200
	0FD1	0DD1	09D1	F9D1	V.32T/7200	V.32T/7200
	0DD1	0DD1	09D1	F9D1	V.32T/7200	V.32T/7200
	0D91	0D91	0D91	FD91	V.32/4800	V.32/4800
V.32/4800	0FF9	0D91	0D91	FD91	V.32T/14400	V.32T/4800
	0FF1	0D91	0D91	FD91	V.32T/12000	V.32T/4800
	0FD1	0D91	0D91	FD91	V.32T/9600	V.32T/4800
	0DD1	0D91	0D91	FD91	V.32T/7200	V.32T/4800
	0D91	0D91	0D91	FD91	V.32/4800	V.32/4800

■ 7811073 0024610 46T ■

Functions 3-11: Dialing Parameters   **Acc. Method: See Below**   **Addr.: See Below**

For Functions 3, 4, 7, 8, and 9, the time T (in ms) is calculated as follows:

Equation: $N = T \times 2.4$

Where: N is the decimal value of the hex number written to RAM (1-FFh).

A value of 0000 for the DTMF or calling tone on time will cause the modem to transmit the tone continuously until FFh is written into TBUFFER.

For functions 10 and 11, the time (in ms) is calculated as follows:

Equation: $N = T/10$

For Functions 5 and 6, the DTMF low band or high band power level (P) in dBm is calculated as follows

Equation: $N = \log^{-1}(P/20) \times 10143$

Where: N is the decimal value of the hex number written to RAM.

Notes:

1. The compromise equalizer is automatically disabled by the transmitter when sending DTMF tones, single tones, or dual tones. The DTMF levels are not affected by the transmit level bits (TLVL). The calling tones, however, are affected by the TLVL bits.

2. Maximum output power = -0.5 dBm.

The dialing parameters and their default values are:

Function	Parameter	Method	Address	Default (Hex)	Default (Dec)
3	DTMF Tone Duration	2	218, 2DB	00DD	92 ms
4	DTMF Interdigit Delay	2	219, 2DC	00AD	72 ms
5	DTMF Low Band Power Level	2	29B, 29C	19C0	− 4.0 dBm
6	DTMF High Band Power Level	2	29D, 29E	2085	− 2.0 dBm
7	Pulse Relay Make Time	1	22C	56	36 ms
8	Pulse Relay Break Time	1	21C	99	64 ms
9	Pulse Interdigit Delay	2	21A, 21B	0708	750 ms
10	Calling Tone On Time	2	290, 2D9	0032	500 ms
11	Calling Tone Off Time	2	291, 2DA	00C8	2 sec

Some DTMF power level values are:

L (dBm)	N (Hex)
−1	2350
−2	1F78
−3	1C0C
−4	1900
−5	1648
−6	13DB

Function 12: **Transmitter Output Level Gain-All Modes**   **Acc. Method: 3**   **Addr.: A48**

Transmitter Output Level Gain-FSK Modes   Acc. Method: 3   Addr.: B57

a. Transmitter Output Level Gain-All Modes (Addr. A48)

The transmitter output level gain constant (G) in dBm is calculated as follows:

Equation: $N = \log^{-1}[G/20] \times 16384$

   Where: N is the decimal value of the hex number written to RAM.

Range: 0 - 7FFFh

Default: 4000h

The transmitter output level gain constant directly controls the output level of all configurations. It is used for fine tuning the output level which is controlled by the TLVL bits. Therefore,

   Output Level = TLVL Setting + Transmitter Output Gain in dBm

Example gain values are:

G (dBm)	N (Hex)	G (dBm)	N (Hex)
+6	7FB2	-8	197A
+5	71CF	-9	16B5
+4	656E	-10	143D
+3	5A67	-11	1209
+2	5092	-12	1013
+1	47CF	-13	0E53
0	4000	-14	0CC5
-1	390A	-15	0B61
-2	32D6	-16	0A24
-3	2D4E	-17	090A
-4	2861	-18	080E
-5	23FD	-19	072E
-6	2013	-20	0666
-7	1C96	-21	05B4

For example, if TLVL is set for -9 dBm and the required level is -30 dBm, the difference is -21 dBm. Therefore, load address A48 with 5B4h.

The dynamic range of the scale factor is effective from +6 dB down to approximately -60 dB, with a resolution of 0.5E-3 dB.

Setting NEWC to a 1 will reset this parameter to the default value.

b. Transmitter Output Level Gain-FSK Modes (Addr. B57)

Equation: $N = \log^{-1}[PO/20] \times C$

   Where: PO is based on TLVL = 9 and transmit output gain constant (all modes) and A48 = 4000h.

   N is the decimal value of the hex number written to RAM.

   C = See the following table:

Configuration	CEQ	C (Dec) - Answer	C (Dec) -Originate
V.21	CEQ = 1	9728	10608
	CEQ = 0	8448	8448
Bell 103	CEQ = 1	9072	10496
	CEQ = 0	8704	8352
V.23/1200 TX	CEQ = 1	12800	12800
	CEQ = 0	12544	12544
V.23/75 TX	CEQ = 1	10496	10496
	CEQ = 0	8448	8448

Setting NEWC to a 1 will reset this parameter to the default value.

Function 13:	Dual Tone 1 Frequency	Acc. Method: 2	Addr.: 280, 281
Function 14:	Dual Tone 2 Frequency	Acc. Method: 2	Addr.: 282, 283

Frequency F (in Hz) is calculated as follows:

Equation: $N = F/0.109863$

Where: N is the decimal value of the hex number written to RAM.

Default = 0

A single or dual tone is transmitted by writing 80h (single tone) or 83h (dual tone) to the CONF register, programming the tone transmit location in RAM, and then activating RTS. The tone will be transmitted as long as RTS is active.

Example values are:

F (Hz)	N (Hex)	F (Hz)	N (Hex)
400	0E39	2100	4AAB
445	0FD2	2250	5000
600	1555	2400	5555
1200	2AAB	3000	6AAB
1800	4000	3600	8000

Function 15:	Dual Tone 1 Power Level	Acc. Method: 2	Addr.: 284, 285
Function 16:	Dual Tone 2 Power Level	Acc. Method: 2	Addr.: 286, 287

Dual tone power level in dBm (PO) is calculated as follows:

Equation: $N = 22304\,[10^{Po/20}]$ (Based on TLVL = 0 and 600 Ω termination.)

Where: N is the decimal value of the hex number written to RAM.

Range: 0 - 7FFFh (Default = 2000h)

Notes:

1. The modem accepts change only when RTS is off.

2. The Transmit Level bits (TLVL) affect output level.

3. Power out = PO + TLVL setting + transmitter output gain constant.

Function 17A:	New Status (NEWS) Masking Registers	Acc. Method: See Table 4-1	Addr.: See Below
Function 17B:	Memory Access Masking Register	Acc. Method: 1	Addr.: 089 (Bit 6)

Writing a 1 in the bit location corresponding to the desired bit will cause NEWS to go active when a status change occurs for the selected bit. All bits default to 0 at power-on-reset. Figure 4-5 shows the applicable masking register bits.

In addition, address 089 (bit 6) controls memory access interrupt (set bit 6 to disable interrupt; reset bit 6 to enable interrupt).

Register Address	Bit								Mask Address (Hex)
	7	6	5	4	3	2	1	0	
1B	EDET	DTDET	OTS	DTMFD	DTMFW				27C
1A	—	—	—	—	DTMFW	SCOBF	SCIBE	—	27D
17	Secondary Transmit Data Buffer/V.34 Transmit Status(SECTXB)								371
16	Secondary Receive Data Buffer/V.34 Receive Status (SECRXB)								370
14	A3CODE								38A
12	Configuration (CONF)								089, bit 7 = 1
0F	RLSD	FED	CTS	DSR	RI	TM	RTSDT	V54DT	241
0E	RTDET	BRKD	RREDT	V32BDT	SPEED				242
0D	P2DET	PNDET	S1DET	SCR1	U1DET/ECTRN	SADET/DETID	TXFNE	HKAB	243
0C	AADET/PROBED	ACDET/MODEOK	CADET/NEGDET	CCDET/DET800	SDET	SNDET	RXFNE	RSEQ	244
0B	TONEA	TONEB	TONEC	ATV25	ATBEL	—	DISDET	EQMAT	245
0A	PNSUC	FLAGDT	PE	FE	OE	CRCS	FLAGS	SYNCD	246
01	—	—	—	—	TXHF	RXHF	—		247

Figure 4-5. NEWS Masking Registers

Function 22:   Far-End Echo Frequency Offset   **Acc. Method: 4**   **Addr.: 852**

Function 22 provides the far-end echo frequency offset (FO), sometimes known as phase roll, in V.34/V.FC/V.32 configurations.

Equation: $FO = (N * SYMBOL\ RATE)/2^{22}$

Where: SYMBOL RATE = 2400, 2800, 3000, 3200, or 3429 (V.34/V.FC) (See Function 60.)

2400 (V.32 bis)

N is the decimal value of the hex number read from RAM.

Function 22 is a 16-bit 2s complement number. It is not valid until rate sequence R3 is detected in the originate modem, or rate sequence R2 is detected in the answer modem for V.32 or until RLSD = 1 for V.34 and V.FC.

Function 23:   Far-End Echo Level   **Acc. Method: 4**   **Addr.: B52**

Function 23 provides the far-end echo power level at RXA in V.34/V.FC/V.32 configurations.

The following table lists average values read from RAM and the corresponding far end echo level in dBm:

Echo Level (dBm)	V.34/V.FC Average Value (Hex)	V.32 bis Average Value (Hex)
-8	1100	1300
-9	0F00	1100
-10	0D00	0F00
-11	0C00	0D00
-12	0A00	0C00
-13	0900	0A00
-15	0700	0800
-20	0400	0500
-25	0250	0300
-30	0150	0180
-35	00C0	00D0
-40	0070	0080
-45	0045	0040

Note: Function 23 is not valid until RLSD is ON.

Function 24:   CTS OFF-to-ON Response Time (RTS-CTS Delay)   **Acc. Method: 2**   **Addr.: 202, 203**

Function 24 determines the CTS off-to-on response time in 2-wire full-duplex configurations.

The response time equations and default values are:

Configuration	Equation	Default Value (Hex)	Default Value (Dec)
V.34, V.FC, V.32	N = (Response time x 2.4 ms) −1	0000	0.4 ms
V.22 bis, V.22, Bell 212A	N = (Response time x 0.6 ms) −1	0000	3 ms
Bell 103	N = (Response time x 0.298 ms) −1	003F	215 ms
V.21	N = (Response time x 0.298 ms) −1	0098	525 ms
V.23/1200Tx	N = Response time x 1.2 ms	00FC	210 ms
V.23/75Tx	N = Response time x 0.072 ms	0010	235 ms
Where: N is the decimal value of the hex number written to RAM.			

Example: For an RTS-CTS delay of 20 ms in V.22 bis, N = [(20)(0.6)]-1 = 11 = 000Bh.

Note: Response time may vary by ± 2 baud times.

Function 25:   Answer Tone Length   **Acc. Method: 2**   **Addr.: 228, 229**

Function 26:   Silence After Answer Tone Period   **Acc. Method: 2**   **Addr.: 22A 22B**

The CCITT 2100 Hz answer tone length and silence after answer tone are calculated as follows:

Configuration	Equation
V.8, V.FC, V.32, V.21, Bell 103	N = T x 300 (V.32 silence: N = T x 2400)
V.22 bis, V.22, Bell 212	N = T x 600
V.23/75Tx, V.23/1200Rx	N = T x 75
V.23/1200Tx, V.23/75Rx	N = T x 1200
Where: N is the decimal value of the hex number written to RAM and T is the time is seconds.	

The modem will rewrite the default values when DTR is turned off or the NEWC bit is set.

The end of answer tone transmission may be determined by monitoring address 051, bit 3. This bit will be set to a 1 when the answer has finished and the silence period has commenced. Unless a power-on reset is performed, this bit must be reset by the host if it is to be monitored again on the following connection.

Note: Address 228, 229 lengthens individual phase reversal times in V.8, V.FC/V.32 bis/V.32. The answer tone length may be adjusted by increasing or decreasing the number of phase reversals at address 04B. The default value at address 04B is 08h (8 phase reversals). This value may be changed only after DTR is set.

Functions 27 - 29: Tone Detector Bandpass Filter Coefficients   **Acc. Method: 3**   **Addr.: See Table 4-4**

A block diagram of the three tone detectors is shown in Figure 4-6. Tone detector C is preceded by a prefilter and a squarer. The purpose of the prefilter and squarer is to allow dual tones to be detected while rejecting the main channel energy. For example, TONEC can be programmed to detect a difference frequency generated by the squarer for detection of 350 Hz and 440 Hz. The prefilter would be designed to reject the energy in the 600 to 3000 Hz band. If the dual tone pair of 350 and 440 Hz appeared (or any other frequency pair in the range of 300 to 600 Hz with a difference of 90 Hz) TONEC would turn on.

The SQDIS bit (02:6) allows the squarer in front of tone detector C to be disabled. If the squarer is disabled then tone detector C will have four cascaded biquads (since there is a prefilter consisting of two biquads), forming an 8-order IIR filter with user programmable coefficients. To make the prefilter transparent (to use TONEC as a 4th order filter), write 7FFFh in coefficients A1 and write 0000 to all other biquad coefficients.

The implementation of the filters allows user definition of the characteristics of the prefilter and the three tone detectors. Table 4-4 provides the DSP RAM address codes for the filter coefficients. Table 4-5 shows the default values. Figure 4-6 shows that the prefilter and the main filter sections of the tone detectors are fourth order (two second-order biquads in cascade), thereby allowing a wide variety of filter characteristics to be synthesized. The only limitation on these user-definable shapes is that their gain should be around unity at the pass frequencies to avoid problems of saturation at one extreme (gain too high) and digital noise at the other (gain too low). Computation of the filter coefficients can be performed by any infinite impulse response (IIR) filter design program which outputs the coefficients in cascaded second-order sections.

The default sample rate is 7200 Hz, however, in the V.8, V.34, or V.FC modes, the sample rate is changed to 9600 Hz and all filter coefficients are changed by the modem. A soft or hard reset is recommended after a V.34 or V.FC connection to restore default filter coefficients.

The level detector in each of the tone detectors flags the detection of a tone if it is in the tone detector passband and if it is above an upper threshold defined by THRESHU. The tone detected flag will remain set until, or unless, the tone falls below a lower threshold defined by THRESHL.

The tone detectors are preceded by an AGC. The gain of the AGC may be read at address 8B9 (DUGAIN). By default, DUGAIN reaches its maximum gain, at a value of 7FFFh, when the receive level is -26 dBm or lower. Signal levels below -26 dBm are thus not affected by the AGC, therefore, the threshold comparator will see a decreasing signal level as the input signal is lowered. The THRESHU and THRESHL adjustments are limited to signal levels below the AGC cut-off point (-26 dBm). If the THRESHU value is adjusted to try to limit the detection threshold to -20 dBm, the AGC will not allow it.

To raise the AGC cut-off point, decrease the value in address BBB (DAGCRF). The DAGCRF default value is FF00h, which results in the -26 dBm cut-off. Decreasing DAGCRF to FE00h raises the AGC cut-off to -20 dBm, thus allowing THRESHU to be adjusted for a minimum detection level of -20 dBm or lower.

The AGC may be disabled by first writing 0 to address 9BB (DSRATE), then writing a 07FFh to address 8B9 (DUGAIN).

The first-order low pass filter in each level detector, defined by the coefficients LPGAIN and LPFBK, controls the response time of each tone detector. Normally, these coefficients will not require alteration, but if, for example, a rapid cadence must be detected on a tone, then the 3 dB cutoff is approximately the reciprocal of the on-time or off-time of the tone, whichever is shorter. Decreasing LPFBK will speed up the response time. If LPFBK is decremented, then LPGAIN should be increase by the same amount. The gain of the filter should be set to unity (LPGAIN + LPFBK ≈ 7FFFh). The default response time is in the order of 0.01 seconds.
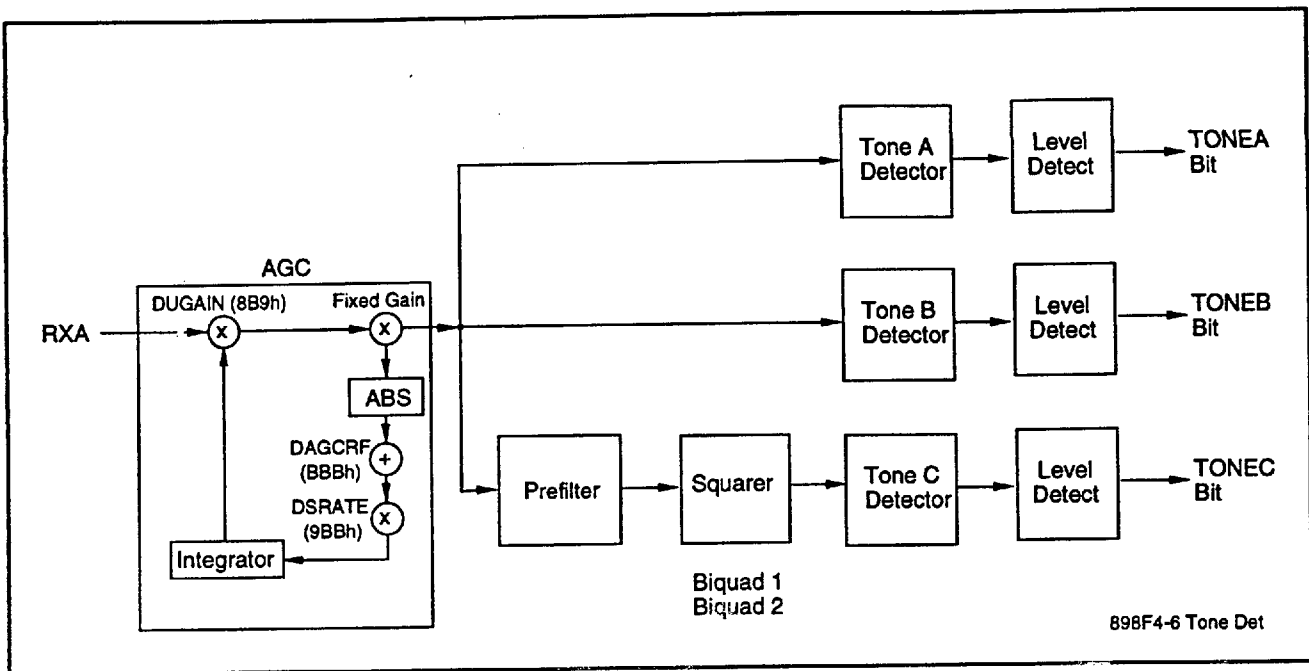
Figure 4-6. Tone Detectors

Table 4-4.   TONEA, TONEB, and TONEC DSP RAM Addresses

Parameter	TONEA		TONEB		TONEC		Prefilter	
	Biquad1	Biquad2	Biquad1	Biquad2	Biquad1	Biquad2	Biquad1	Biquad2
A3	AA1	BA1	AA7	BA7	AAD	BAD	AB2	BB2
A2	AA2	BA2	AA8	BA8	AAE	BAE	AB3	BB3
A1	AA3	BA3	AA9	BA9	AAF	BAF	AB4	BB4
B2	AA4	BA4	AAA	BAA	AB0	BB0	AB5	BB5
B1	AA5	BA5	AAB	BAB	AB1	BB1	AB6	BB6

Table 4-5.   TONEA, TONEB, and TONEC Default Values

Parameter	TONEA		TONEB		TONEC	
	Address	Value (Hex)	Address	Value (Hex)	Address	Value (Hex)
LPFBK	BA0	7F30	BA6	7E67	BAC	7F30
LPGAIN	AA0	00CF	AA6	02DF	AAC	00CF
THRESHU	AB8	0880	AB9	2A00	ABA	1600
THRESHL	BB8	0580	BB9	1C00	BBA	0A00

Example:

A call-progress tone detector is required for the US telephone network to detect appropriate tones that exceed –35 dBm.

Solution:

The requirement can be met by detecting tones in the 245 Hz-650 Hz range. A bandpass filter with a passband of 245 Hz-650 Hz must be designed. Any filter up to fourth order can be implemented and, normally, it is best to choose the highest order available, especially for bandpass designs. A biquad filter design package could carry out this function by defining the passband frequencies, the filter order, the filter gain (chose unity), and the filter sampling rate (7200 Hz). An example of suitable coefficients is:

Function	A1	A2	A3	B1	B2
Biquad 1	0.1368	–0.2736	0.1368	1.8281	–0.8835
Biquad 2	0.1368	0.2736	0.1368	1.5716	–0.7920

These values should first be divided by two because coefficients greater than one are unrealized in the actual filter implementation. This division should be done even if none of the coefficients in the design are greater than one. This is because the biquad sections have been implemented as shown in Figure 4-7. The modified values are, therefore:

Function	A1'	A2'	A3'	B1'	B2'
Biquad 1	0.0684	–0.1368	0.0684	0.9140	–0.4418
Biquad 2	0.0684	0.1368	0.0684	0.7858	–0.3960

Next, convert the above numbers to fractional 2s complement numbers. In this case, the default coefficient values for TONEA:

Function	A1'	A2'	A3'	B1'	B2'
Biquad 1	08C2	EE7C	08C2	74FE	C774
Biquad 2	08C2	1184	08C2	6495	CD4F

The second part of the requirement is to detect tones that exceed –35 dBm. The approximate values of THRESHU and the corresponding tone level detected for TONEA at 500 Hz are:

THRESHU (Hex)	Tone Level Detected (dBm)
1100	–29
0C00	–32
0880	–35
0600	–38

THRESHU should be 0880h. If no hysteresis is required in the tone detector, then set THRESHL to 0880h (see Table 4-5). If hysteresis is required, then make THRESHL < THRESHU. Threshold levels stated in the data sheets are measured at the band edges. Other filter designs may require different values to those shown above. Note that changing threshold coefficients may change the bandwidth response of tone detectors.

Table 4-6 shows the filter coefficient values for specific filters. Adjust THRESHL and THRESHU as necessary (see Table 4-5).
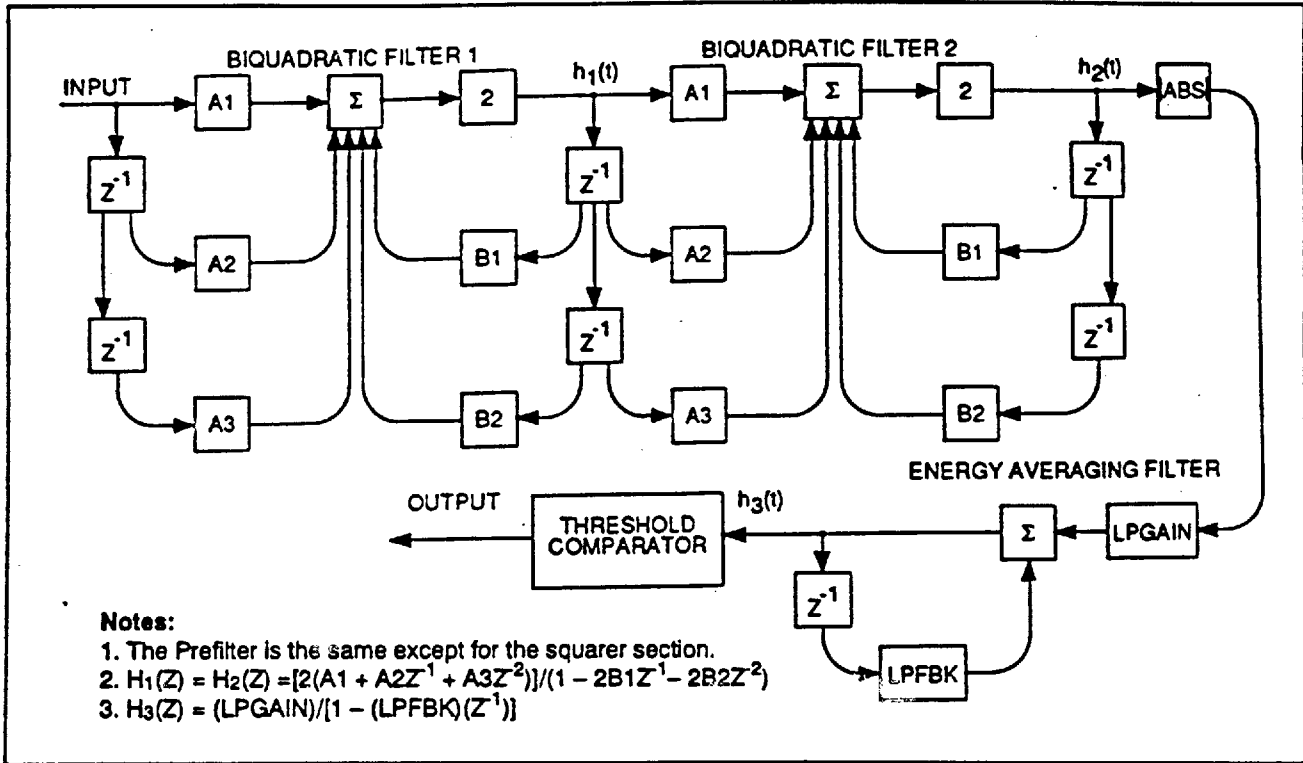
BIQUADRATIC FILTER 1 — BIQUADRATIC FILTER 2 — ENERGY AVERAGING FILTER

Notes:

1. The Prefilter is the same except for the squarer section.
2. $H_1(Z) = H_2(Z) = [2(A1 + A2Z^{-1} + A3Z^{-2})]/(1 - 2B1Z^{-1} - 2B2Z^{-2})$
3. $H_3(Z) = (LPGAIN)/[1 - (LPFBK)(Z^{-1})]$

Figure 4-7. Biquad Filter and Level Detector

Table 4-6. Example Tone Detector Filter Coefficients

Sampling Rate/Filter	Biquad1 Coefficients (Hex)					Biquad2 Coefficients (Hex)				
	A3	A2	A1	B2	B1	A3	A2	A1	B2	B1
7200 Hz (Non-V.FC Modes)										
1100 Hz	01B3	FC9C	01B4	C147	48C6	01B3	0097	01B4	C147	4897
1800 Hz	0184	FCFB	0185	C147	001C	0184	01BD	0185	C147	FFE4
2250 Hz	0205	FBF9	0206	C147	CF9C	0205	0380	0206	C147	CF68
2100 Hz	01E8	FC32	01E9	C147	DF4F	01E8	034E	01E9	C147	DF19
2225 Hz	0205	FBF9	0206	C147	D22D	0205	0380	0206	C147	D1F8
1270 Hz	02B2	FAA1	02B3	C147	38A4	02B2	00F0	02B3	C147	3871
1650 Hz	0306	F9F9	0307	C147	10A6	0306	010D	0307	C147	106E
980 Hz	0205	FBF9	0206	C147	5337	0205	00B4	0206	C147	530D
1300 Hz	0244	FB7B	0245	C147	35A7	0244	00CA	0245	C147	3574
245-650 Hz[1]	08C2	EE7C	08C2	C774	74FE	08C2	1184	08C2	CD4F	6495
360-440 Hz[2]	0000	FD36	02CA	C63E	7243	02CA	0593	02CA	C63E	7243
9600 Hz (V.8, V.34, & V.FC Modes)										
1800 Hz	0372	FEA6	0372	C063	30D6	00C4	FFDA	00C4	C063	30D6
2250 Hz	0119	FE72	0130	C063	0C82	02D9	FEE3	02D9	C063	0C82
2100 Hz	0397	F8D3	0399	C3C9	1905	0397	02C0	0399	C3C9	176D
2225 Hz	0884	EF47	0889	C147	0E90	0884	FE54	0889	C147	0E68
1270 Hz	0123	FDBA	0123	C147	55B6	0123	00DF	0123	C147	5596
1650 Hz	028B	FAEA	028C	C289	3BDA	028B	01F3	028C	C289	3A68
980 Hz	0224	FBB8	0225	C289	64FF	0224	01A4	0225	C289	6403
1300 Hz	0112	FDDB	0113	C147	536D	0112	00D2	0113	C147	533D
245-650 Hz	F8EA	0000	0716	C63E	6FE1	0716	F5FB	0716	C774	7601
360-440 Hz	01AA	FEBC	01AA	C7CD	7438	FF5C	0000	00A4	C148	7A66

Notes:

1. TONEA default.
2. TONEB default.

Function 30:   RLSD Drop Out Timer   **Acc. Method: 1**   **Addr.: 270, 271**

<u>**a. VFC, V.32 bis, V33, V17, V29, V27, V.26 and V.21 channel 2**</u>

RAM address 270, 271 holds the value for a 16-bit counter which decrements at a baud interval when energy is removed from RXA. When the counter reaches 0000, RLSD turns off. The count down may be observed in RAM addresses 389 (value from address 388) and 046 (value from address 270). The value in address 271 (MSB), 270 (LSB) may be changed anytime after RLSD = 1. The default time may be read in address 271, 270 after RLSD = 1. See Table 1-1 to obtain baud rates for individual modes. By prolonging the RLSD on-off time, the modem can be kept in a freeze mode which can be used to bridge long dropouts. Dropouts of several seconds can be bridged by extending this timer. The default RLSD on-off time for V.FC and V.32bis is approximately 500 ms. Note that in VFC and V.32 bis modes, it is possible for the receiver to lock onto the local transmit signal when the received signal is lost. (See the DISDET description in Table 3-1.)

<u>**b. V.22 bis, V.22, Bell 212/1200**</u>

The 8-bit value in RAM address 270 controls the RLSD on-off time. The value counts down to 0 in address 046. Once this value starts to decrement, after the signal has been removed from RXA, the host may continuously write a large value in address 046, not allowing the counter to decrement, in order to prolong the RLSD on-off time if the 8-bit counter is not sufficient. This, however, requires the host to monitor address 046 during the connection until it starts to decrement.

The 8-bit value in RAM address 271 controls the time the modem will wait for energy to return after RLSD has turned off. This value is loaded into address 049 and starts to count up until it reaches a value of 63h. The default value in address 271 is 0 which gives the maximum freeze time of 63h bauds. After RLSD = 0, the host may continuously write 00 in address 049, not allowing the counter to increment, in order to prolong the freeze time. Both addresses 271 and 270 may be written to after RLSD = 1.

Function 31:	**RLSD Turn-On Threshold (RLSD_ON)**	**Acc. Method: 2**	**Addr.: 134, 135**
Function 32:	**RLSD Turn-Off Threshold (RLSD_OFF)**	**Acc. Method: 2**	**Addr.: 136, 137**
	RLSD Threshold Offset	**Acc. Method: 2**	**Addr.: 138, 139**
	RLSD Overwrite Control	**Acc. Method: 1**	**Addr.: 10D (Bit 2)**
	Extended RTH Control	**Acc. Method: 1**	**Addr.: 10D (Bit 6)**
	Receiver Gain	**Acc. Method: 1**	**Addr.: A03**
	Receiver Turn-off Threshold	**Acc. Method: 3**	**Addr.: A04**
	Receiver Turn-on Threshold	**Acc. Method: 3**	**Addr.: A05**

The receive RLSD thresholds may be modified by altering the internal receiver gain (address A03) or threshold values (address A04, A05) to shift the turn-on and or turn-off threshold up or down.

<u>Method 1</u>

A control bit (address 10D, bit 2) enables or disables the over-writing of the RLSD thresholds by the modem's own default threshold table [0 = overwriting enabled (default); 1 = overwriting disabled]. The default state is initialized only by power on or a soft reset.

The RLSD thresholds are loaded into memory locations RLSD_ON and RLSD_OFF. During the Idle mode initialization, the 2-byte value stored in RLSD_ON is used as the RLSD on threshold. When the modem is in Data mode, the 2-byte RLSD_OFF value is used for the RLSD off threshold.

During reset, the respective thresholds for V.32 bis 14400 bps are loaded into RLSD_ON and RLSD_OFF as initial values. After reset, the host may then alter these values using the following procedure:

1.   Set 10D, bit 2 (to prevent custom values from being overwritten by default values).

2.   Load in the custom RLSD values.

3.   Set NEWC.

Note: the thresholds can be over-written at any time, but this method ensures that the first connection after a NEWC uses the correct value of ON threshold.

<u>Extended RLSD Threshold Selection:</u>

The Extended RTH bit (XRTH) (address 10D, bit 6) controls the reduction of RLSD thresholds by approximately 5 dBm [0 = disables reduction (default); 1 = enables reduction]. If XRTH is a 1, RTH must be reset to 0. This extended RLSD threshold method affects all configurations while preserving the hysteresis.

The amount of threshold reduction (offset) can be controlled manually by the host writing a 16-bit offset value into address 138, 139. For example, this offset is useful for compensating for any loss or gain that may be introduced by the DAA/hybrid used. Note that if a negative offset is wanted, then the twos complement number should be entered. The maximum amount of offset that can safely be subtracted is 900h (F700h, 2s complement).

RC288DPi Modem Designer's Guide

Method 2

The RTH bit field selects a default threshold setting for the modem's receiver (see RTH description in Table 3-1). The receiver gain is adjusted automatically for each of the four RTH values and switches between a turn-on and a turn-off value depending if the modem is in an idle mode (RLSD off) or connect mode (RLSD on). A threshold offset is associated with each RTH setting (see Function 32) which in turn offsets the receiver gain by a given amount. The higher the gain value, the higher the threshold. The following are the RTH offset RAM addresses and the corresponding default offset.

RTH Code	Parameter	Method	Address (Hex)	Default (Hex)
0	RTH0 Offset	2	2D0, 2D1	0000
1	RTH1 Offset	2	2D2, 2D3	1AC0
2	RTH2 Offset	2	2D4, 2D5	2CC0
3	RTH3 Offset	2	2D6, 2D7	4640

Note: A power-on-reset will return the offset values to their default states.

The following are the default idle receiver gain values (turn-on values) for the corresponding modes. The gain values are increased by the modem when in data mode. In V.34, V.FC, and V.32 bis configurations, this value may change several times during the handshake.

Mode	Gain Value (Hex) in Address A03h *	
	Answer	Originate
V.34	0AAF	0AAF
V.FC	1070	1A08
V.32bis, V.32	186E	1533
V.22 bis	13F9	16B2
V.22	16C7	1719
Bell 212A	1689	1822
Bell 103	2200	2200
V.33, V.17	1A90	N/A
V.29	1D4C	N/A
V.27	1B10	N/A
V.21	2300	2300
V.23 1200	1500	1500
V.23/75	2400	2400
V.21 Channel 2	2000	N/A
V.26	1E00	N/A

* Note:
The gain value includes the RTH offset default (shown for RTH offset = 0). Add the appropriate RTH offset value, e.g., for RTH default offset values, add 0 (RTH = 0), 1AC0h (RTH = 1), 2CC0h (RTH = 2), or 4640h (RTH = 3) to obtain the gain value to write to address A03.

Example: To increase both the turn-on and turn-off thresholds by a few tenths of a dB using RTH = 0, write a value of approximately 0100h in RAM address 2D0, 2D1 while in idle mode and set NEWC. By setting NEWC, the offset is added to the receiver gain value. If setting NEWC is not desired, the offset loaded in RAM may be manually added to the receiver gain value at address A03.

Example: To decrease both the turn-on and turn-off thresholds by a few tenths of a dB using RTH = 0, write a value of FF00h to address 2D0, 2D1 while in idle mode and set NEWC. This will subtract 0100h from the gain value.

In both examples, note that if RTH is set to a 1, the corresponding offset is 1AC0 and a value of 1BC0h should be written to address 2D2, 2D3 to increase the threshold or 19C0h to decrease the threshold. The offset is always relative to the RTH value used.

4-20

1026

■ 7811073 0024620 309 ■

The offset may be changed when connected in data mode (RLSD on) if the default hysteresis is not satisfactory. For example, choose an offset value to obtain the desired turn-on threshold and set NEWC. When RLSD is on in data mode, change the offset value to increase or decrease the turn-off threshold in order to obtain a narrower or wider hysteresis. After writing the desired offset, add or subtract the change in offset to the current receiver gain value at address A03. **Do not set NEWC.** Setting NEWC in data mode will either terminate or disrupt the connection. When RLSD turns off, repeat the process.

Selecting the appropriate offset is accomplished by empirical measurements. Note that the gain value for RTH = 1 is equal to the default offset value plus the gain value for RTH = 0, a total offset of 1AC0h. The difference in thresholds between RTH = 0 and RTH = 1 is 10 dB. From this, the user can extrapolate the approximate offset value needed for the desired threshold.

Although address A03 may be used to alter the RLSD thresholds in all modes, by default, the FSK and V.29 modes use the same value in address A03 for both on and off thresholds. Instead of changing A03, these modes use the threshold addresses A05 (turn on) and A04 (turn off). The user non-volatile RLSD values and the RLSD offset values in RAM affect addresses A05 and A04 when in these modes.

In summary, when a value is written to the RLSD offset addresses (2D0-2D6), that value is summed with the value in A03 or A05 and A04 depending on the mode used, regardless if the default thresholds or the user non-volatile thresholds (addresses 134-137) are used. When address 10D, bit 2 is set, the user non-volatile thresholds are used. When address 10D, bit 2 is reset, the default threshold values in ROM are used and will appear in addresses 134-137. Regardless of the source, the threshold values (plus the offset value if any) will appear in A03 or A05 and A04 depending on the mode used. The XRTH function parallels the operation of the offset address 2D0, 2D1 and may be used to shift both the on and off RLSD thresholds up or down for all modes when RTH = 0.

Function 34:   V.32 PN Length   Acc. Method: 2   Addr.: 288, 289

The V.32 bis/V.32 handshake and retrain sequence may be shortened or lengthened to meet special applications by adjusting the length of the PN (TRN) sequence. The answering modem sends two TRN sequences during the handshake while the originating modem sends only one.

The TRN time T (in ms) is calculated as follows:

Equation: $N = (2.4 \times T) - 256$

Where: N is the decimal equivalent of the hex number written to RAM and T is the time in ms.

Note: Values of N should be kept within 400h to 1F00h. A power-on reset will clear this location.

Changing the TRN lengths should be reserved for special applications only and is not recommended. Short TRN sequences may jeopardize the success of the handshake or retrain. Consult the CCITT V.32/V.32 bis specifications for TRN length limitations. Only the originate TRN and the first answer TRN lengths are affected.

Function 36:   AGC Gain Word   Acc. Method: 4   Addr.: A00

Function 36 is useful for determining the receive level (RL) at the Receive Analog (RXA) input. The number in RAM is related to the receive level as follows:

Configuration	Equation
V.34, V.FC, V.33, V.17, V.29, V.27	RL = N/682.7 - 52 dB
V.32 bis, V.32	RL = N/682.7 - 53 dB
V.22 bis, V.22, Bell 212, V.23/1200	RL = N/682.7 - 48 dB
V.21, V.23/75	RL = N/682.7 - 54 dB
Bell 103	RL = N/682.7 - 51 dB
Where: N is the decimal value of the hex number read from RAM.	

This formula is valid only if the receive level is above the RLSD off-to-on threshold.

Function 37:   Round Trip Far Echo Delay   Acc. Method: 4   Addr.: 239

Function 37 provides the value of the round trip delay measured during the V.32 handshake.

Equation: $RTD = (N/X) - 10$ (for V.34)

$RTD = (N/X) - 3.5$ (for V.FC)

$RTD = (N/2.4) - 29$ (for V.32 bis)

Where: RTD = Round Trip Delay in ms

N = Decimal equivalent of value read from RAM

X = symbol rate/1000, i.e., 2.4, 2.8, 3.0, 3.2, or 3.429 (see Function 60).

Function 45:   Equalizer Frequency Correction   **Acc. Method: 4**   **Addr.: 811**

Function 45 provides the value of the Equalizer Frequency Correction.

Equation: $F = N/27.3$ (for V.32 bis)

Where: F = Carrier frequency offset in Hz

N is the decimal value of the hexadecimal number read from RAM

Function 46:   Eye Quality Monitor   **Acc. Method: 4**   **Addr.: 20C**

In V.32 4800 bps, V.29, V.27, V.22 bis, V.22 and Bell 212A modes, EQM is the filtered squared magnitude of the error vector. However, for all TCM modes (V.34, V.FC, and V.33 modes, and V.32 12000, 9600, and 7200 bps modes), EQM is the filtered minimum trellis path length (or metric). This gives a better indication of signal quality for trellis modes.

The error vector formed by the decision logic can be used to indicate relative signal quality. As signal quality deteriorates, the average error vector increases in magnitude. By calculating the magnitude of the error vector and filter the results, a number inversely proportional to signal quality is derived. This number is called the eye quality monitor (EQM). Because of the filter time constant, EQM should be allowed to stabilize for approximately 700 baud times following RLSD going active.

The EQM value for the non-trellis configurations is the filtered squared magnitude of the error vector and represents the average signal power contained in the error component. The power is directly proportional to the probability of errors occurring in the received data and can be used to implement a discrete Data Signal Quality Detector circuit (circuit 110 of CCITT Recommendation V.24 or circuit CG of the RS-232-C standard) by comparing the EQM value against experimentally determined criteria (Bit Error Rate curves). Figure 4-6 illustrates the relationship of the EQM number to an eye pattern created by a 4-point signal structure (e.g., V.29/4800 bps) in the presence of high level white noise. The EQM value is proportional to the square of the radius of the disk around any ideal point. The radius increases when signal to noise ratio (SNR) decreases. As the radius approaches the ideal point's boundary values, the bit error rate (BER) increases. Curves of BER as a function of the SNR are used to establish a criteria for determining the acceptability of EQM values. Therefore, from an EQM value, the host processor can determine an approximate BER value. If the BER is found to be unacceptable, the host may cause the modem to fallback to a lower speed to improve BER.

It should be noted that the meaning of EQM varies with the type of line disturbance present on the line and with the various configurations. A given magnitude of EQM in V.29/9600 does not represent the same BER as in V.27/4800. The former configuration has 16 points that are more closely spaced than the four signal points in the latter, resulting in a greater probability of error for a given level of noise or jitter. Also, the type of line disturbance has a significant bearing on the EQM value. For example, white noise produces an evenly distributed smearing of the eye pattern with about equal magnitude and phase error while phase jitter produces phase error with little error in magnitude.

Since EQM is dependent upon the signal structure of the modulation being used and the type of line disturbance, EQM must therefore be determined empirically in each application.

A typical eye pattern generation circuit is shown in Figure 7-7.

Note that the eye pattern is not displayed when 2800 or 3429 baud is selected in V.34 or V.FC modes. The use of precoding and shaping in V.34 and V.FC modes will distort the eye pattern's appearance, even under ideal conditions. The EQM value should be monitored in V.34 and V.FC modes to determine the quality of the connection.
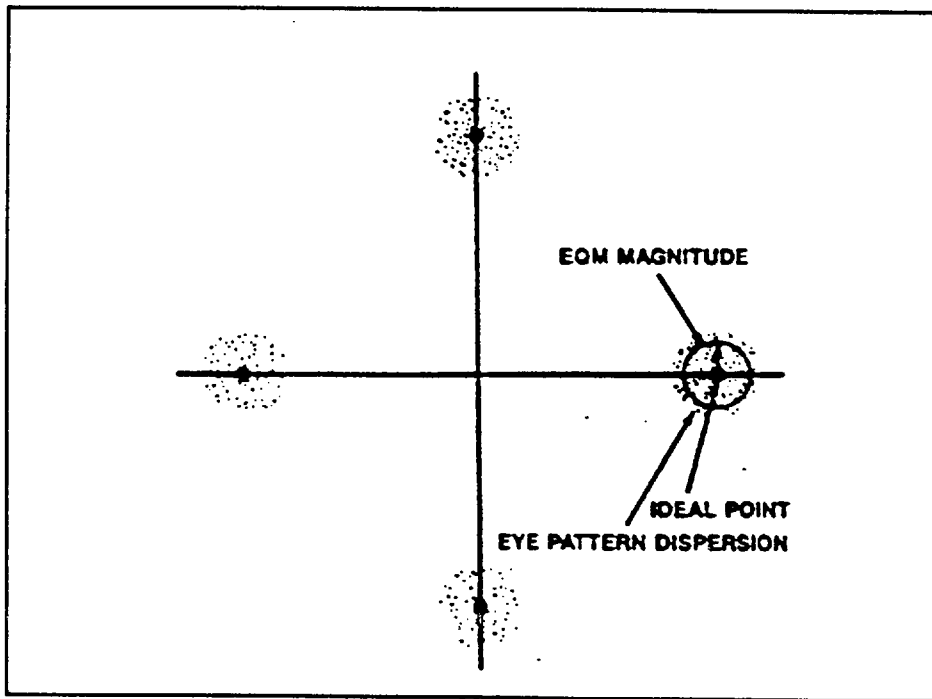
Figure 4-8.   Relationship of EQM to Eye Pattern

Function 47:   Maximum Period of Valid Ring Signal   **Acc. Method: 1**   **Addr.: 21F**

Function 48:   Minimum Period of Valid Ring Signal   **Acc. Method: 1**   **Addr.: 21E**

The ring detector measures the period of pulses on the ring detect input and determines whether the pulses are within the frequency range specified by the Maximum Period of Valid Ring Signal and Minimum Period of Valid Ring Signal functions. Since maximum period corresponds to minimum frequency, the formula for calculating these functions is given in terms of frequency.

Frequency F (in Hz) is calculated as follows:

Equation: $N = 2400/F$

Where: N is the decimal value of the hex number written to RAM (05h-FFh).

Default: The default values are:

Function	Parameter	Method	Address	Default (Hex)	Default (Dec)
47	Maximum Period of Valid Ring Signal	1	21F	A0	15 Hz
48	Minimum Period of Valid Ring Signal	1	21E	23	68 Hz

Note: Writing 00 to Function 48 will cause the RI bit state and ~RI output pin level to follow the RINGD input pin level.

Function 49:   Phase Jitter Frequency   **Acc. Method: 4**   **Addr.: 80E**

The phase jitter frequency estimate is available in V.34/V.FC/V.32 bis/V.32 modes only. The phase jitter amplitude must be greater than approximately 6 degrees with a minimum frequency of 10 Hz in order for the modem to lock on and track the jitter.

Equation: $F = N*\text{Symbol Rate}/2^{16}$ (V.34/V.FC)

$F = N/27.3$ (V.32 bis/V.32)

Where: F is the frequency in Hz.

N is the decimal equivalent of the hex number read from RAM.

Symbol Rate = 2400, 2800, 3000, 3200, or 3429.

Function 50:   Phase Jitter Amplitude   **Acc. Method: 4**   **Addr.: 80D**

The phase jitter amplitude estimate is available in V.34/V.FC/V.32 bis/V.32 modes only. The phase jitter amplitude must be greater than approximately 6 degrees with a minimum frequency of 10 Hz in order for the modem to lock on and track the jitter.

Equation: $AP = N/90$

Where: AP is the amplitude in degrees.

N is the decimal equivalent (absolute value) of the hex number read from RAM

Function 51:   Guard Tone Level   **Acc. Method: 3**   **Addr.: B46**

Guard tone power in dBm (PO) is calculated as follows (based on TLVL bits = 9 and 600 Ω termination):

Configuration	Equation	Default Value (Hex)
1800 Hz guard tone (GTS bit = 0; CEQ bit = 1)	$N = 4926 [10^{Po/20}]$	036C
1800 Hz guard tone (GTS bit = 0; CEQ bit = 0)	$N = 8458 [10^{Po/20}]$	05E0
550 Hz guard tone (GTS bit = 1; CEQ bit = 1)	$N = 5128 [10^{Po/20}]$	0390
550 Hz guard tone (GTS bit = 1; CEQ bit = 0)	$N = 8458 [10^{Po/20}]$	05D8

Notes:

1.   Setting the NEWC bit will reset the power level to its default level.

2.   The power level may be adjusted only after the GTE bit is set.

3.   The transmit level bits (TLVL) affect the guard tone power output level.

4.   Guard tone power is available in V.22 bis/2400 or V.22/1200 answer mode only.

Function 52:   CCITT CRC 32   **Acc. Method: 1**   **Addr.: 0B3**

The type of cyclic redundancy check (CRC) generation and detection can be selected by writing to address 0B3, bit 0 [0 = CCITT CRC 32; 1 = CCITT CRC 16 (default)].

Function 53:   Secondary Channel Transmitter Speed Select (V.32 bis/V.32)
                                                                           Acc. Method: 1   **Addr.: 28E**
            Secondary Channel Receiver Speed Select (V.32 bis/V.32)
                                                                           Acc. Method: 1   **Addr.: 28B**

The default data rate for the secondary channel is 150 bps. The rate can be changed by modifying a divide factor in two addresses: 28E for the transmitter and 28B for the receiver. The following table lists the possible secondary channel speeds for the various main channel speeds and the corresponding RAM value. Reset will clear locations 28E and 28B.

Main Channel Speed (bps)	Secondary Channel Speed (bps)					
	Transmitter and Receiver RAM Divide Constant Values (Hex)					
	75	150	300	600	1200	2400
14400	8	10				
12000	8	10				
9600 TCM	4	8	10			
9600 QAM	2	4	8	10		
7200	2	4 .	8	10		

Functions 54 - 57: Not Applicable.

Functions 58:   V.FC Automatic Carrier Select (ACS) Enable   **Acc. Method: 1**   **Addr.: 13F (Bit 4)**
            V.FC Carrier Deviation Negotiation (CDN) Disable   **Acc. Method: 1**   **Addr.: 100 (Bit 4)**
            V.FC Carrier Deviation Offset   **Acc. Method: 1**   **Addr.: 10A**

Carrier Deviation Negotiation (CDN) can be controlled by writing to address 100, bit 4 [0 = CDN enabled (default); 1 = CDN disabled].

Automatic Carrier Select (ACS) can be controlled by writing to address 13F, bit 4 [0 = ACS disabled (default); 1 = ACS enabled] when the CDN bit is reset.

ACS is enabled when the ACS bit is set and the CDN bit is reset. When ACS is enabled, the center frequency is calculated from the estimates of the bandwidth low band edge and high band edge. The difference between this 'ideal' center frequency and the default carrier frequency (for a given symbol rate) is derived and used to provide carrier deviation information during the handshake negotiation. On receiving this offset, the remote receiver will select a carrier recommended by the local transmitter and both will use this carrier. Note that the carrier selection may be asymmetric.

When the ACS bit is reset and the CDN bit is reset, manual or host control of carrier deviation is possible. This is achieved by writing the required amount of offset (in 5 Hz units) into address 10A.

Note that during the handshake, the CDN bit may be set by the modem. The host must reset the CDN bit for ACS or host control to be enabled.

Functions 59:   V.FC Carrier Bias   **Acc. Method: 1**   **Addr.: 212**

This function provides a bias that can be used when determining the optimal carrier frequency. This may be used to set the carrier to a position which may best suit the frequency response of the DAA.

To use this feature, add the amount of additional bias in units of 5 Hz to the default value (40h) and store the sum in address 212.

Example 1: If a bias of 50 Hz is desired, store 4Ah (40h + 50/5 = 40h +0Ah) into address 212.

Example 2: If a bias of -10 Hz is desired, store 3Eh (40h - 10/5 = 40h -02h) into address 212.

Function 60:   **V.34/V.FC Symbol Rate Value**   **Acc. Method: 1 (RO)**   **Addr.: 2E3**
Function 61:   **V.34/V.FC Baud Rate Mask (BRM)**   **Acc. Method: 1**   **Addr.: 101**

During the start-up handshake, the modem probes the communication channel and determines the available bandwidth. This information helps establish the common symbol rate between the modems. The following data rate ranges are available for a selected symbol rate:

Symbol Rate (baud)	Highest Possible V.34/V.FC Data Rate (bps)
2400	21600
2800	24000
3000	26400
3200	28800
3429	28800

If line conditions cannot support the higher symbol rates, the modem automatically reduces the data rate to match the allowable symbol rate.

The host can control the symbol rate negotiation process via the Baud Mask Register (BMR), located at address 101. By either setting or resetting one or more of five bits in the BMR, the host can specify if a particular symbol rate is to be supported. In Loop 3 (L3ACT = 1), the baud rate may be selected by writing the desired symbol rate value (0, 2, 3, 4, or 5) to address 2E3 anytime prior to establishing the loopback. The default value is 4 for 3200 baud. The symbol rates and the corresponding bit positions are:

Symbol Rate (baud)	Symbol Rate Value (Addr. 2E3)	Baud Mask Register (BRM) Enable Bit Position (Addr. 101)
2400	0	0
Reserved	1	1*
2800	2	2
3000	3	3
3200	4	4
3429	5	5
* Bit 1 must be always be a 0.		

When the modem determines, from the bandwidth, the maximum supportable symbol rate, the modem will enable all symbol rates below that maximum value. For example, if the line probe indicates that the bandwidth is adequate to support 3000 baud, then 2800 and 2400 baud will also be supported. This selection of symbol rates is, however, dependent upon the contents of the BMR. Again, for the same example, if a host does not want to support 2800 baud, the host must reset bit 2 of the BMR. If both modems do not agree during probing, e.g., the originate modem chooses 3000 baud and the answer modem chooses 2800 baud, then the highest common rate will be 2400 baud. In the event there is no common rate, the modems will default to 2400 baud.

Figure 4-9 shows the symbol rate negotiation process. The final symbol rate chosen may be read from address 2E3 after the negotiation is complete. A value of 10h, for example, would indicate a symbol rate of 3200 baud.
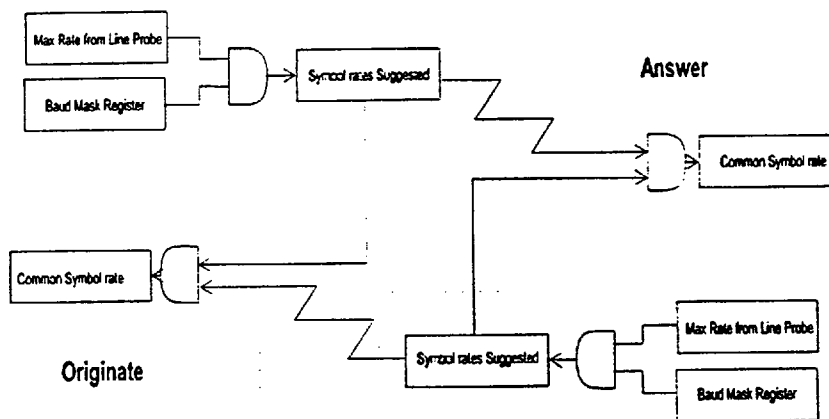

Figure 4-9. V.FC Symbol Rate Negotiation Process

Function 62:   V.34/V.FC Pre-Emphasis Filter Number   Acc. Method: 4   Addr.: B44
Function 63:   V.34/V.FC Pre-Emphasis Filter Override Number   Acc. Method: 1   Addr.: 0E6
                       V.34/V.FC Emphasis Disable   Acc. Method: 1   Addr.: 100 (Bit 1)

For V.FC, a result obtained from measuring the communication channel characteristics, by means of a line probe, is the amount of attenuation measured at the upper band edge of the probe spectrum. A number is derived which maps into a selection of 15 transmit equalizer filters. This number, in most cases, approximates to 50% of this upper band edge attenuation. This number is transmitted to the remote modem during the Frame Negotiation phase of the V.FC start-up handshake. The mapping of this number to the amount of Pre-emphasis in dBs is:

For V.34, there are only 11 pre-emphasis filters defined, each matching the templates defined in ITU-T V.34 (Figure 1 and 2). The locations which indicate which filter is being used is the same as for V.FC and the method to manually load one of the eleven filters (0 to Ah) is also the same.

V.FC		V.34	
Pre-emphasis Filter Suggestion Number	Amount of Upper Band Edge Attenuation Compensated (dB)	Pre-emphasis Filter Suggestion Number	Amount of Upper Band Edge Attenuation Compensated (dB)
0	0	0	See ITU-T V.34 Figures 1 and 2.
1	1	1	
2	2	2	
3	3	3	
4	4	4	
5	5	5	
6	6	6	
7	7	7	
8	8	8	
9	9	9	
A	10	A	
B	12		
C	13		
D	14		
E	15		
F	22		

The Pre-emphasis filter selected can be read from the V.34/V.FC Pre-Emphasis Filter Number (address B44).

The Pre-emphasis negotiation can be ignored by setting address 100, bit 1, Pre-emphasis Disable (PREDIS). This bit does not stop the measurement or the transmission of the suggested pre-emphasis filter, but rather causes the receiver to ignore the suggestion.

Pre-emphasis can also be controlled by using the CEQ bit in the modem interface memory. If this bit is reset, any selected pre-emphasis or transmit compromise filter will be ignored. In this way, the host can control pre-emphasis by setting/resetting CEQ. However, if the host wishes to use a custom compromise filter, then by using the PREDIS bit, the suggested filter will be ignored and the host's custom defined compromise filter will be used.

The procedure to manually select one of the pre-emphasis filters is:

1.   Set PREDIS (address 100, bit 1) to override negotiation.

2.   Load the Pre-Emphasis Filter Over-Ride Number (address 0E6) with the Pre-emphasis Filter Suggestion Number from the table above.

3.   Ensure that CEQ is on.

Function 64: V.34/V.FC Transmit Level Deviation Disable   **Acc. Method: 1**   **Addr.: 100 (Bit 3)**

During line probing, the modem measures the receive level of the line signal. If that receive level is high enough, the modem suggests that the remote modem reduce its own transmit level in order to improve signal-dependent noise performance.

For V.34, The transmit level power drop does not use receive level alone. Decision is also based on improved noise and harmonic distortion criteria.

For V.FC, the suggestion of transmit level deviation is:

V.FC	
Measured Received Level	**Suggested Transmit Level Reduction**
Above -20 dBm	6 dB
-20 dBm to -25 dBm	4 dB
-25 dBm to -30 dBm	2 dB
Below -30 dBm	0 dB

To force the modem to ignore the suggested transmit level reduction, set the Transmit Level Deviation Disable (TLDDIS) (address 100, bit 3) to a 1.

Function 65: V.FC Transmit Level Deviation Bias   **Acc. Method: 1**   **Addr.: 216**

This function provides a bias which is added to the selected transmit level deviation. This bias can be regarded as an offset to the offset. It allows the host to either add or subtract a host-defined bias to the deviation chosen by the modem during the negotiation handshake. The number stored represents the amount of additional offset required in steps of 1dB. The effect of this offset is limited such that the transmit level cannot be lower than -20 dBm or greater than 0 dBm. The default value of 0 selects transmit level deviation steps of 0, 2, 4, or 6 dB (see Function 64).

Example 1: If transmit level deviation steps of 3, 5, 7, or 9 dB is desired, write 03h (0 + 3 = 03h) to address 216.

Example 2: If transmit level deviation steps of 0, 1, 3, or 5 dB, write FFh (0 - 1 = FFh) to address 216.

Function 66-67: Reserved

Function 68: EQM Above Threshold   **Acc. Method: 1**   **Addr.: 133**

When the high byte of the EQM reading (address 20D) goes above the EQM Above Threshold, the modem will assert the EQMAT bit (register 0B, bit 1). The host can set up a NEWS interrupt to monitor changes to this bit (see EQMAT in Function 17). The default value of EQM Above Threshold is 30h and is written at POR and is unaffected by NEWC. The modem does NOT reset the EQMAT bit; the host must reset the EQMAT bit.

Function 69: EQM Scale Factor (Gain)   **Acc. Method: 3**   **Addr.: A29**
                    EQM ARA Bias (Offset)   **Acc. Method: 2**   **Addr.: 2A4, 2A5**

The automatic rate adaptation (ARA) algorithm adjusts the data rate based on the level of EQM. The algorithm is twofold, one being used for initial train and retrain, the other for rate-renegotiation. In both cases, ARA is enabled by setting the EARC bit (15:0), which defaults off.

Upon initial train and retrain, the EQM is checked towards the end of the training, just before the rate negotiation. The 4-point EQM is compared against a table of values representing the necessary levels to achieve the corresponding data rates with an EQM of around 2000h. Once the maximum achievable rate is determined, the CONF register is changed to reflect the estimate, and is then used to suggest a data rate in the following negotiations.

In rate-renegotiation, only the instigating modem implements the algorithm. The responding modem, as usual, indicates availability of all rates. The instigating modem will attempt to go to a rate which will result in an EQM of 1800h-3000h. To do that, it will check the current EQM (at the start of rate-renegotiation), and change CONF according to the following table:

EQM Before Rate Change	Rate Change
Above 3000h	Down 1
1800h-3000h	No change
C00h-1800h	Up 1
600h-C00h	Up 2
300h-600h	Up 3
Below 300h	Up 4

The rates suggested in the rate-renegotiation will then be reflected the CONF.

There are two methods to modify the ARA scaling.

Method 1 - Modifying the EQM Value

The first method consists of modifying the EQM value read by the ARA algorithm through the EQM offset value at address 2A5 (MSB) and 2A4 (LSB). The EQM offset value is added to the EQM value. If a more reliable connection is desired, write a positive EQM offset value to increase the EQM value. If a less reliable connection is desired, write a negative EQM offset value to decrease the EQM value. This method does not affect the EQM reading at address 20C.

Example 1: For example, if the actual EQM value is 2E00h and the EQM offset value 0500h, the EQM seen by the ARA algorithm will be 3300h, thus giving the impression that the connection quality is worse than it actually is, thereby causing the modem to connect or rate change to a more conservative rate.

Example 2: If a less reliable connection is desired, write a negative number (2s complement) to the EQM offset location. An EQM offset value of FE00h would subtract 200h from the actual EQM value.

Method 2 - Modifying the EQM Gain

The second method to affect these rate adjustments is to increase the EQM gain at address A29 for a more reliable connection or to lower the EQM gain for a less reliable connection. The default value is 1000h. This method affects the EQM reading at address 20C.

In V.34, the EQM gain may be changed after the SDET bit is set.

In V.FC modes, the EQM gain may be written only after the MODEOK bit has been set by the modem.

In V.32 bis, the EQM gain may be changed after the DTR bit is set.

Example 1: If a more reliable (lower speed) connection is desired, increase the EQM gain from the normal value of 1000h to 2000h. The rate selected would then be one lower, e.g., 21600 will be selected whereas 24000 would have been selected without the change.

Example 2: If a less reliable (higher speed) connection is desired, decrease the EQM gain from 1000h to 0800h.

Function 70: V.21/V.23 CTS Mark Qualify	Acc Method: 1	Address: 10D (Bit 3)

In V.21/V.23 configurations, CTS turn-on qualifying time can be controlled by writing to address 10D, bit 3 [0 = no qualifying time after Mark (default); 1 = qualifying time of 45 ±5 ms after Mark]. This bit is unaffected by the action of NEWC.

Function 71:	V.FC Symbol Rate Bandwidth Offset (BWOFFS)	Acc Method: 1	Address: 13B
	V.FC Symbol Rate Edge Offset (BEOFFS)	Acc Method: 1	Address: 13C

The host can control the thresholds used by the probing for the determination of symbol rate using two variables: BWOFFS (address 13B) and BEOFFS (address 13C). BWOFFS is an offset added to the channel bandwidth estimate generated by the handshake probing. This allows a more optimistic bandwidth to be suggested. BEOFFS then adds a further offset to the high band edge and low band edge estimates, such that the position of the available bandwidth can be shifted.

For BWOFFS, the larger the value, the wider the bandwidth estimate. The suggested range is from 0 to 40h. The default value is 0.

For BEOFFS, the larger the value, the greater the shift of the bandwidth up in frequency. The suggested range is from 0 to 10h. The default value is 0.

Example: Two V.FC modems were configured for operation at a data rate of 19.2 kbps over a TAS100 set to line C4. With both BEOFFS and BWOFFS set to zero, the modems selected a 2400 baud symbol rate. Subsequent setting of BWOFFS to 20h was enough to force the modems to select 3429 baud. With BWOFFS set to 20h, the selected baud rate could be reduced gradually from 3429 to 2400 by varying BEOFFS from 0 to 8h.

Function 72:   V.FC Data Rate Sequence Mask   Acc Method: 2   Address: 116, 117
                V.FC Received Rate Sequence   Acc Method: 2   Address: 208, 209

Bits in the V.FC rate sequence can be masked out. The V.FC rate sequence mask is divided into two bytes located at addresses 116 (LSB) and 117 (MSB). The use of separate memory locations for the V.FC rate sequence mask prevents any conflict between V.FC and V.32 bis modes during fallback. The mask is set to FFFFh at reset. It is not affected by NEWC.

To enable a particular rate, the bit corresponding to that rate indicated in Table 4-7 must be set to a 1; to disable a particular rate, the corresponding bit must be cleared to a 0. The frame bits must not be altered.

The received rate sequence can be read at addresses 208 (LSB) and 209 (MSB). This received rate sequence indicates the remote modem's speed by both the remote rate sequence mask register and the remote ARA function (EARC = 1). It does not necessarily indicate the highest speed available by the remote modem. (See Function 87 for a comparison with V.34.)

Table 4-7.   V.FC Rate Sequence Mask Bit Assignments

Bit	Rate Sequence Mask-MSB (address 117) Received Rate Sequence-MSB (Address 209)								Rate Sequence Mask-LSB (address 116) Received Rate Sequence-LSB (Address 208)							
	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Frame Bits	1	X	X	X	1	X	X	X	1	X	X	X	0	1	0	1
14400										1						
16800								1								
19200							1									
21600						1										
24000				1												
26400			1													
28800		1														

Function 73:   No Automode to FSK   Acc Method: 1   Address: 13F (Bit 0)

Automode to FSK modes can be controlled by writing to address 13F, bit 0 [0 = automode to FSK enabled (default); 1 = automode to FSK disabled]. This bit remains unaffected by NEWC.

If enabled (0), the automode selection will allow FSK connections. If disabled (1), automode selection will not configure to any FSK mode.

Function 74:   Receive FIFO Trigger Level   **Acc Method: 1**   **Address: 32C**

Transmitter FIFO (TX FIFO)

Use of the 16-byte TX FIFO is controlled by writing to the FIFOEN bit (register 04, bit 4) [0 = TX FIFO disabled; 1 = TX FIFO enabled].

When the TX FIFO is enabled (FIFOEN = 1), the host can continuously write to TBUFFER as long as (register 0D, bit 1) is set. The TDBE bit (register 1E, bit 3) will be set whenever the TX FIFO is empty. Two control bits, TEOF (register 11, bit 1) and TXP (register 11, bit 0) are buffered along with the TX FIFO data. The TEOF bit is used in HDLC mode to indicate that the next byte written into TBUFFER is the last byte of the frame. TXP is used in 8-bit, stuff parity asynchronous mode to indicate the parity bit. Also, the TXFHF status bit (register 01, bit 2) indicates when the TX FIFO is half full.

When the TX FIFO is ·isabled (FIFOEN = 0), the TX FIFO is one byte in length.

Receiver FIFO (RX FIFO)

The 16-byte RX FIFO is always enabled. Use of the RX FIFO can be controlled by writing to address 032. The default value is CBh which gives a trigger level of 14 bytes and a time-out of 17 clock cycles.

Bits 6-7: Trigger Level. Selects the trigger level in the 16-byte RX FIFO. For example, setting bits 7 and 6 to 11 selects a trigger level of 14 bytes. That is, RDBF will not become asserted until the receive FIFO is 14 bytes full and the time-out delay has not elapsed (see below).

B7	B6	Trigger Level (No. of Bytes)
0	0	Trigger level = 1
0	1	Trigger level = 4
1	0	Trigger level = 8
1	1	Trigger level = 14

Bit 5:   Must be 0.

Bits 2-4: Time-out Delay. Selects the length of idle time that will cause RDBF to be asserted when the RX FIFO is not empty. Idle time is the length of time that elapses without the modem data pump writing into the RX FIFO or the host reading data from the RX FIFO. This feature prevents data from being "held up" in the RX FIFO.

B4	B3	B2	Idle Time (In Bit Times)
0	0	0	9 bit times
0	0	1	13 bit times
0	1	0	17 bit times
0	1	1	21 bit times
1	0	0	25 bit times
1	0	1	29 bit times
1	1	0	33 bit times
1	1	1	37 bit times

Bit 1: Idle Time Time-out Enable. 1 = the time-out enabled; 0 = time out disabled. When Time out is disabled (0), RDBF will be asserted only when the RX FIFO threshold is reached.

Bit 0: Not Used.

RX FIFO Error Status Bits

The RX FIFO includes five error status bits: BRKD (register 0E, bit 6), SYNCD (register 0A, bit 1), RXP (register 01, bit 0), FE (register 0A, bit 4), and PE (register 0A, bit 5). SYNCD is used for 7E flag detection in HDLC mode only and BRKD indicates that an asynchronous break has been received. FE indicates a framing error in asynchronous mode or an abort condition in HDLC mode. PE indicates an asynchronous parity error or a CRC error in HDLC mode. RXP indicates the received parity bit in 8-bit asynchronous stuff parity mode.

IMPORTANT: The host must read the status bits prior to reading the byte from RBUFFER. Note that this is the opposite of how it should be done using the RC96DPL/RC144DPL or RC96DPi/RC144DPi.)

Also, there are two status bits (RXHF and RXFNE) that the host can use to monitor the RX FIFO operation. RXHF (register 01, bit 1) indicates when the receive FIFO is half full and RXFNE (register 0C, bit 1) is set whenever the RX FIFO has data in it.

Function 75: V.34/V.FC GSTN Cleardown Option   **Acc Method: 1**   **Address: 10D (Bit 4)**

Two methods can be used to communicate the GSTN Cleardown request. The first is through a retrain request and the second is via a rate re-negotiation. Regardless which of the two methods the host decides to use, the Cleardown procedure is the same for both.

V.34

Sourcing a V.34 Cleardown Request

The Cleardown procedure provided in the V.34 modes is strictly defined, and as such there is now only one method to initiate the Cleardown. The retrain method that has been provided in V.32bis and V.FC is not supported in V.34. The method used is:

1. The host loads CONF with C0h.

2. The host sets RREN to 1

3. The data pump transmits Cleardown request as per §11.7 of ITU-TSS Recommendation V.34.

Receiving a V.34 Cleardown Request

1. On receiving a Cleardown request, the remote modem responds by writing 96h into the ABCODE register and also writing C0h into the CONF register.

Alternatively, the host can select an option which will allow the modems to exit to their idle states after transmitting or receiving a Cleardown request. In doing so, the modem's RLSD will drop and thus allow the host a simpler check for disconnecting. This option is selected by setting address 10D, bit 4.

V.FC

Sourcing a V.FC GSTN Cleardown Request

1. The host loads CONF with 40h.

2. The host sets either RTRN or RREN to a 1.

3. Upon completion of transmitting the request, the modem writes a Cleardown Abort Code into ABCODE. This allows a host to either terminate the connection immediately upon receiving this ABCODE, or (as implemented in the RC96DPL) allows a timer to expire after setting CONF to 40h and then terminates the connection.

Receiving a V.FC Cleardown Request

A Cleardown request is acted upon when the modem receives either a retrain with the Cleardown request in the Negotiation Packet or a rate re-negotiation with no speed indicated. On receiving this request, the modem will write 40h into CONF and will also write the Cleardown Abort Code into ABCODE. The host can, therefore, check either location for Cleardown request occurrence.

Alternatively, the host can select an option which will allow the modems to exit to their idle states after transmitting or receiving a Cleardown request. In doing so, the modem's RLSD will drop and thus allow the host a simpler check for disconnecting. This option is selected by setting address 10D, bit 4.

V.32 bis

Sourcing a V.32 bis GSTN Cleardown Request

1. The host loads CONF with 70h.

2. The host sets either RTRN or RREN to a 1.

3. RLSD drops automatically.

Receiving a V.32 bis Cleardown Request

1. The host loads CONF with 70h.

2. RLSD drops automatically.

Function 81:   V.34 Spectral Parameters Control   **Acc Method: 1**   **Address: 105**

The host can control some of the spectral parameters that the transmitter uses for cases where the local PTT has regulations governing transmission. These control bits can usually be used in their default state and the host need only alter them if required to meet PTT approval.

Bit 7: Transmitter Enable for the Low Carrier Frequency for 3200 Baud. When set, the transmitter is allowed to use the low carrier frequency for 3200 baud.

Bit 6: Transmitter Enable for the High Carrier Frequency for 3200 Baud. When set, the transmitter is allowed to use the high carrier frequency for 3200 baud.

Bit 5: Transmitter Enable for the Low Carrier Frequency for 3000 Baud. When set, the transmitter is allowed to use the low carrier frequency for 3000 baud.

Bit 4: Transmitter Enable for the High Carrier Frequency for 3000 Baud. When set, the transmitter is allowed to use the high carrier frequency for 3000 baud.

Bit 0-3: Reserved. Do not alter the contents.

Function 82:   V.34 Phase 2 Power Reduction   **Acc Method: 1 (RO)**   **Address: 0E2**

In V.34 mode, the modem supports the reduction in transmit power if instructed by the remote modem during the start-up sequence. The amount of power drop from the nominal is 0 to 14 dB. The TLDDIS bit (at location 100 bit 3, see Function 64)) enables the local modem to implement the amount of power drop being suggested by the remote modem or to ignore it and not drop the level at all. The Transmit level Deviation Bias (Function 65) also applies to V.34. Function 82 specifies the amount of power drop in dB after Phase 2.

Function 83:   V.34 Low Band Symbol Rate Edge Estimate Offset   Acc Method: 1   Address: 13B
            V.34 High Band Symbol Rate Edge Estimate Offset   Acc Method: 1   Address: 13C

The probing band edge results can be fine tuned by writing to a Low Band Edge Estimate Offset (address 13B) and a High Band Edge Estimate Offset (address 13C). These parameters store the number of steps (in units of 37.5 Hz) to add to the band edge estimates. If a negative offset is required then the twos complement number is stored. Note that these offsets overwrite any offset or bias used in bandwidth estimation for the V.FC. (see Function 71).

Function 84:   V.34 Receiver Speed Indication   **Acc Method: 1**   **Address: 384**

In V.34 mode, Function 84 bits indicate the receiver's data rate and the SPEED status bits (see Section 3) indicate the transmitter's data rate at the completion of a handshake. The encoding is:

Speed (Hex)	Data Rate (bps)
0	0–300
1	600
2	1200
3	2400
4	4800
5	7200
6	9600
7	12000
8	14400
9	16800
A	19200
B	21600
C	24000
D	26400
E	28800

Function 85:   V.34 Data Rate Mask   **Acc Method: 2**   **Address: 382, 383**

The V.34 data rate masks occupy two bytes in RAM. Locations 382 and 383 represent the lower byte and the upper byte of the mask, respectively (Table 4-8). The bits in the mask represent the enabling of a particular data rate if set or disabled if reset. The definition of the bits are data rate 2400 is at bit 0 (i.e. the LSB of address 382), 4800 is at bit 1, 7200 at bit 2 and so on up to 28800 bps (in 2400 bps increments) which is bit 11 of the mask (or bit 3 of address 383). The remaining 4 bits, bits 12 through 15 must always remain at a logic 1. Bits 12-15 are reserved for future use.

Table 4-8.   V.34 Rate Sequence Mask Bit Assignments

Data Rate (bps)	V.34 Data Rate Mask-MSB (address 383)								V.34 Data Rate Mask-LSB (address 382)							
	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
2400	-	-	-	-	X	X	X	X	X	X	X	X	X	X	X	1
4800	-	-	-	-	X	X	X	X	X	X	X	X	X	X	1	X
7200	-	-	-	-	X	X	X	X	X	X	X	X	X	1	X	X
9600	-	-	-	-	X	X	X	X	X	X	X	X	1	X	X	X
12000	-	-	-	-	X	X	X	X	X	X	X	1	X	X	X	X
14400	-	-	-	-	X	X	X	X	X	X	1	X	X	X	X	X
16800	-	-	-	-	X	X	X	X	X	1	X	X	X	X	X	X
19200	-	-	-	-	X	X	X	X	1	X	X	X	X	X	X	X
21600	-	-	-	-	X	X	X	1	X	X	X	X	X	X	X	X
24000	-	-	-	-	X	X	1	X	X	X	X	X	X	X	X	X
26400	-	-	-	-	X	1	X	X	X	X	X	X	X	X	X	X
28800	-	-	-	-	1	X	X	X	X	X	X	X	X	X	X	X

V.34 has a different requirement on how rates and configurations are interpreted. Previous CCITT specifications were in the most part symmetric but V.34 allows for data rates to be asymmetric. This implies that the procedures for rate setting are now different from other configurations, and some control words and bits (e.g., CONF and SPEED) lose their meaning.

V.34 does have a bit to force symmetric rates. If that bit is set, the behavior is same as in V.FC. Then CONF decides the rate if initiating, and the highest enabled rate in the rate ask if responding. This is of course modified if ARA is enabled.

With asymmetric rates, the following preliminary procedure is used.

1.   First of all, CONF will reflect the RECEIVE rate, since that is what is controlled locally.

2.   The transmit rate suggested to the remote modem is always the highest rate enabled in the rate mask. This makes sense since if data rates are to be limited then it will happen via the rate masks.

3.   The receive rate suggested is taken from CONF code, both if responding and initiating.

If the modem is responding the data rates will remain unchanged unless either a rate-renegotiation is requested or ARA is enabled.

If the modem is initiating, the host will first set CONF and then set RREN, and the rate will be that given by CONF. Of course, if ARA is enabled, then CONF is irrelevant.

Receive or Transmit	Modem Initiating or Responding	Determining Factor of Data Rates Selected			
		Without ARA		With ARA	
		Symmetric Rates	Asymmetric Rates	Symmetric Rates	Asymmetric Rates
Receive	Initiating	CONF	CONF	ARA algorithm	ARA algorithm
	Responding	Rate Mask	CONF	ARA algorithm	ARA algorithm
Transmit	Initiating	CONF	Rate Mask	ARA algorithm	Rate Mask
	Responding	Rate Mask	Rate Mask	ARA algorithm	Rate Mask

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Function 86:   **V.34 Asymmetric Data Rates Enable**   **Acc Method: 1**   **Address: 13F Bit 6**

V.34 modes normally operate with asymmetric data rates for the transmitter and receiver. Resetting (default state) address 13F bit 6 (Function 85) forces the transmitter and receiver data rates to be the same. Setting address 13F bit 6 allows the transmitter data rate to be different than the receiver data rate. Bits 12-15 are reserved for future use.

Function 87:   **V.34 Remote Modem Data Rate Capability**   **Acc Method: 2**   **Address: 208, 209**
                V.34 Remote Modem Asymmetric Data Rate   **Acc Method: 1**   **Address: 209, bit 7**

The data rate capability of the remote modem is reflected in a binary sequence transmitted by the remote modem during Phase 4 of the handshake. This 12-bit received sequence is stored in locations 208h and 209h (Table 4-9). The definition of this field is the same as that described for the V.34 Data Rate Mask (Function 84). Also stored in bit 7 of the 209h is the capability of the remote modem to support asymmetric data rates (if set, then capability is enabled). This information is valid after RLSD is ON. Note that unlike V.FC, the received V.34 rate sequence indicates the remote modem's true speed capabilities as it is masked only by the remote mask sequence register and not by the remote ARA function (EARC bit = 1). For example, the modem may connect at 24000 bps by request of the remote modem's ARA, yet the received rate sequence may indicate that the remote modem can support 28800 bps. This information may be used for fall forward decisions.

Table 4-9.   V.34 Remote Mode Data Rate Capability Bit Assignments

Data Rate (bps)	V.34 Remote Mode Data Rate Capability -MSB (Address 209)								V.34 Remote Mode Data Rate Capability-LSB (Address 208)							
	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
2400	-	-	-	-	X	X	X	X	X	X	X	X	X	X	X	1
4800	-	-	-	-	X	X	X	X	X	X	X	X	X	X	1	X
7200	-	-	-	-	X	X	X	X	X	X	X	X	X	1	X	X
9600	-	-	-	-	X	X	X	X	X	X	X	X	1	X	X	X
12000	-	-	-	-	X	X	X	X	X	X	X	1	X	X	X	X
14400	-	-	-	-	X	X	X	X	X	X	1	X	X	X	X	X
16800	-	-	-	-	X	X	X	X	X	1	X	X	X	X	X	X
19200	-	-	-	-	X	X	X	X	1	X	X	X	X	X	X	X
21600	-	-	-	-	X	X	X	1	X	X	X	X	X	X	X	X
24000	-	-	-	-	X	X	1	X	X	X	X	X	X	X	X	X
26400	-	-	-	-	X	1	X	X	X	X	X	X	X	X	X	X
28800	-	-	-	-	1	X	X	X	X	X	X	X	X	X	X	X

Function 88:   V.8 Status Registers - See Section 9.

Function 89:   V.8 Control Registers - See Section 9.

Function 90:   Modulation Modes- See Section 9.

Function 91:   V.8 MaxFrameByteCount- See Section 9.

Function 92:   V.8 Call Functions- See Section 9.

Function 93:   CM Frame - - See Section 9.

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Function 100:   Minimum On Time (DTMF)   Acc Method: 3   Address: A78

The on-time is defined as the minimum period of time of the DTMF signal beginning when the signal is detected and ending when the energy is below the turn-off threshold. The on-time parameter cannot be set below 20 ms (0000h). The default on-time parameter is set for 40.0 ±1 ms. The on-time will vary with signal level. To increase or decrease the on-time parameter value, convert the increase/decrease into hexadecimal and add/subtract to/from the current value.

    Format: 16 bits, twos complement, positive value

    Range: 0000h to 7FFFh

    Equation: Minimum On Time ± [(Increase/Decrease)Sample Rate]h

Function 101   Minimum Off Time (DTMF)   Acc Method: 3   Address: 878

The minimum off time is defined as the minimum period of time of the DTMF signal beginning when the energy falls below the turn-off threshold and ending when a gain hit is detected. The off-time parameter is equal to the desired minimum off-time minus the drop out time. The default off time is set for 40.0 ± 1 ms with a default dropout time parameter of 5.0 ms. To increase or decrease the off-time parameter value, convert the increase/decrease into hex and add/subtract to/from the current value.

    Format: 16 bits, twos complement, positive value

    Range: 0000h to 7FFFh

    Equation: Minimum Off Time ± [(Increase/Decrease)Sample Rate]h (dropout time equal to 5.0 ms).

Function 102:   Minimum Cycle Time (DTMF)   Acc Method: 3   Address: 978

The minimum cycle time is defined as the minimum period of the DTMF signal beginning when the signal is detected and ending when the next signal begins. The cycle time parameter is equal to the desired minimum cycle-time minus the dropout time. The default cycle time parameter is set for 93.0 ±1 ms with a default drop out time parameter of 5.0 ms. To increase or decrease the cycle time parameter value, convert the increase/decrease into hex and add/subtract to/from the current value.

    Format: 16 bits, twos complement, positive value

    Range: 0000h to 7FFFh

    Equation: Minimum Cycle Time ± [(Increase/Decrease)Sample Rate]h (dropout time equal to 5.0 ms).

Function 103:   Minimum Dropout Time (DTMF)   Acc Method: 3   Address: B78

The minimum dropout time is defined as the maximum period of the DTMF signal beginning when the signal energy drops below the turn-off threshold and ending when the signal energy returns that is considered to be part of the on time. The default dropout time parameter is set to 5.0 ms.

    Format: 16 bits, twos complement, positive value

    Range: 0000h to 7FFFh

    Equation: [(Desired time)Sample Rate]h

Function 104:   Maximum Speech Energy (DTMF)   Acc Method: 3   Address: A77

This parameter specifies the maximum relative speech energy that may be detected and still receive DTMF signals. The speech energy is measured in the frequency region of second or third harmonics of the DTMF tones. To disable the speech energy detector, set this parameter to its full scale positive value (7FFFh). Decreasing the value of this parameter may degrade signal-to-noise ratio (SNR) performance, but may reduce false settings of status bit EDET due to speech signals. To increase or decrease the maximum speech energy parameter value, convert the increase/decrease into hex and add/subtract to/from the current value.

    Format: 16 bits, twos complement, positive value

    Range: 0000h to 7FFFh

    Equation: Maximum Speech Energy ± (Increase/Decrease)h

Function 105: Frequency Deviation, Low Group (DTMF) **Acc Method: 3** **Address: 876**

This parameter controls the acceptable frequency range for the low group DTMF tones (697, 770, 852, and 941 Hz). Increasing the value of this parameter increases the frequency range. The frequency range will vary from one DTMF symbol to another. To increase or decrease the parameter value, convert the increase/decrease into hex and add/subtract to/from the current value.

    Format: 16 bits, twos complement, positive value

    Range: 0000h to 7FFFh

    Equation: Frequency Deviation ±(Increase/Decrease)h

Function 106: Frequency Deviation, High Group (DTMF) **Acc Method: 3** **Address: A76**

This parameter controls the acceptable frequency range for the high group DTMF tones (1209, 1336, 1477, and 1633 Hz). Increasing the value of this parameter increases the frequency range. The frequency range will vary from one DTMF symbol to another. To increase or decrease the parameter value, convert the increase/decrease into hex and add/subtract to/from the current value.

    Format: 16 bits, twos complement, positive value

    Range: 0000h to 7FFFh

    Equation: Frequency Deviation ±(Increase/Decrease)h

Function 107: Negative Twist Control, TWIST4 (DTMF) **Acc Method: 3** **Address: 977**

This parameter controls the acceptable negative twist for the DTMF signals. Decreasing this parameter increases the acceptable negative twist level. The twist will vary from one DTMF symbol to another. To increase or decrease the parameter value, convert the increase/decrease into hex and add/subtract to/from the default value.

    Format: 16 bits, twos complement, positive value

    Range: 0000h to 7FFFh

    Equation: Negative Twist ±(Increase/Decrease)h

    Default: 1420h

Function 108: Positive Twist Control, TWIST8 (DTMF) **Acc Method: 3** **Address: 877**

This parameter controls the acceptable positive twist for the DTMF signals. Decreasing this parameter increases the acceptable positive twist level. The twist will vary from one DTMF symbol to another. To increase or decrease the parameter value, convert the increase/decrease into hex and add/subtract to/from the default value.

    Format: 16 bits, twos complement, positive value

    Range: 0000h to 7FFFh

    Equation: Positive Twist ±(Increase/Decrease)h

    Default: 2800h

Function 109: Maximum Energy Hit Time (DTMF) **Acc Method: 3** **Address: A67**

This parameter represents the duration of an allowed energy impulse during the off time measurement. The default value of 0000h means no gain hits will be tolerated during the off time.

    Format: 16 bits, twos complement, positive value

    Range: 0000h to 7FFFh

    Equation: [(Desired Time)(Sample Rate)]h

Function 110: ADC Speech Sample Scaling Parameter, ADCS (ADPCM Rx-coding)
                                            Acc Method: 3 **Address: BD1**

The received signal sample is scaled by parameter ADCS prior to ADPCM compression by the Rx-coder. Decreasing the value of this parameter attenuates the received speech samples.

    Format: 16 bits, twos complement, positive value

    Range: 0000h to 7FFFh

    Default: 7FF0h

■ 7811073 0024637 602 ■

Function 111:   White Noise Output Scaling Parameter, RANOISE (ADPCM Tx-decoding and Silence Interpolation)
                                                            Acc Method: 3   Address: A35

This parameter controls the output level of the white noise inserted during silence intervals when the decoder is enabled.

    Format: 16 bit, twos complement, positive value

    Range: 0000h to 7FFFh

    Default: 0080h

Function 112:   Minimum Silence Magnitude Threshold, MTHRESH (ADPCM Rx-coding and Silence Deletion)
                                                            Acc Method: 3   Address: A36

If the background noise level is high, MTHRESH may be increased to allow more silence to be detected and deleted. Any signal with energy less than MTHRESH is detected as silence. However, a signal with energy greater than MTHRESH may or may not be detected as silence depending upon ADPCM algorithm processing.

    Format: 16 bits, twos complement, positive value

    Range: 0000h to 7FFFh

    Default: 0100h

Function 113:   Detecting Silence in Speech Parameter, SILSPE (ADPCM Rx-coding and Silence Deletion)
                                                            Acc Method: 3   Address: B37

SILSPE is used in determining when silence is detected during speech. To delay detection of speech-to-silence transition, increase SILSPE. A late transition will prevent the ends of spoken words from being deleted.

    Format: 16 bits, twos complement, positive value

    Range: 0000h to 7FFFh

    Default: 5555h

Function 114:   Detecting Speech in Silence Parameter, SPESIL (ADPCM Rx-coding and Silence Deletion)
                                                            Acc Method: 3   Address: B38

SPESIL is used in determining when speech is detected during silence. To advance detection of silence-to-speech transition, increase SPESIL. An early transition will prevent the beginning of spoken words from being deleted.

    Format: 16 bits, twos complement, positive value

    Range: 0000h to 7FFFh

    Default: 5000h

Function 115:   Minimum Silence Magnitude Adaptation Parameter, MADAPT (ADPCM Rx-coding and Silence Deletion)
                                                            Acc Method: 3   Address: B39

MADAPT controls the rate at which the silence-to-speech energy threshold adapts to the changing received signal energy. If MADAPT is too small, segments of a speech signal will be deleted resulting in unintelligible, choppy, speech.

    Format: 16 bits, twos complement, positive value

    Range: 0000h to 7FFFh

    Default: 5555h