TOSHIBA

INTEGRATED CIRCUIT

TECHNICAL DATA

TOSHIBA MOS TYPE DIGITAL INTEGRATED CIRCUIT

T6497

SILICON MONOLITHIC CMOS SILICON GATE

CMOS CLOCK GENERATOR/CONTROLLER FOR CMOS Z80®

GENERAL DESCRIPTION

The T6497 is a clock generator/controller for Toshiba CMOS Z80 microprocessor (TMPZ84C00P) and peripheral devices. The T6497 has two inputs for choosing one of three modes. When CPU executes HALT instruction, T6497 enters to one of three states described below

(1) RUN MODE

The T6497 is always providing the clock (CLK) to Z80 CPU and peripheral devices. (CPU is actually in HALT state and executes NOP instruction until an interrupt signal or a reset signal is recognized).

(2) IDLE MODE

The T6497 stops providing the clock. However only the internal oscillator continues its operation.

(3) STOP MODE

The T6497 stops its operation.

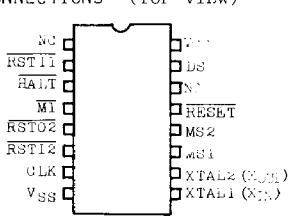
In STOP MODE, CMOS Z80 microcomputer system may stop its operation, so that power consumption to maintain microcomputer system will be extremely reduced.

An interrupt signal ($\overline{NMI}$ or $\overline{INT}$) or a reset signal ($\overline{RESET}$) makes CPU terminate HALT states. The T6497 is fabricated with Toshiba C^2MOS Silicon Gate Technology and molded in 16-pin standard dual-in-line plastic package.

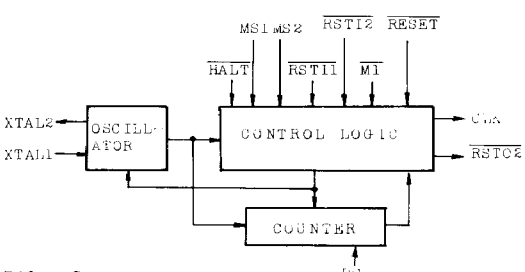
FEATURES

- Toshiba CMOS Z80 Compatible
- 5 Volt Single Power Supply
  5V±10%
- Selectable Three Modes
  RUN MODE
  IDLE MODE
  STOP MODE
- Low Power Consumption
  2mA Typ. @5V @4MHz
  500μA Typ. @5V @4MHz(IDLE MODE)
  10μA Max. @5V(STOP MODE)
- Extended Operating Temperature Range
  -40°C to 85°C

PIN CONNECTIONS (TOP VIEW)



BLOCK DIAGRAM



® Z80 is a trademark of Zilog Inc..

PIN NAMES AND PIN DESCRIPTION

Pin Name	No. of Pins	I/O, 3-state	Description
MS1, MS2	2	Input	Input for Mode select.
XTAL1, XTAL2	2	Input	Terminals for a crystal.
$\overline{\text{RSTI1}}$	1	Input	Input to resume the CLK. (Level trigger) Usually input for $\overline{\text{INT}}$ request.
$\overline{\text{RSTI2}}$	1	Input	Input with a latch to resume the CLK. (Edge trigger) Usually input for $\overline{\text{NMI}}$ request.
$\overline{\text{RSTO2}}$	1	Output	Output corresponding to RSTI2. Usually output for NMI terminal of CPU.
$\overline{\text{MI}}$	1	Input	Input for $\overline{\text{MI}}$ signal from CPU.
$\overline{\text{HALT}}$	1	Input	Input for $\overline{\text{HALT}}$ signal from CPU.
RESET	1	Input	Input signal to resume the CLK. Usually input for RESET signal.
CLK	1	Output	Clock output. When HALT instruction is executed by Z80 CPU in either IDLE MODE or STOP MODE, CLK is kept a low level.
DS	1	Input	Input for selecting the number of counter stage. It is used to determine warming-up time when T6497 restarts from STOP MODE.
NC	2	-	No connection
V_{CC}	1	Power	Single 5V power supply.
V_{SS}	1	Power	Ground reference.

FUNCTIONAL DESCRIPTION

Table 1 illustrates mode select and those functions.
There are two modes (IDLE and STOP) effective when HALT instruction is executed by Z80 CPU. The T6497 continuously provides the system clock (CLK) to Z80 CPU and peripherals unless HALT instruction is executed. In Idle Mode or Stop mode, $\overline{RSTI1}$, $\overline{RSTI2}$ or $\overline{RESET}$ makes the T6497 resume the CLK.

MS1	MS2	MODE	FUNCTIONS
1	1	RUN	Always provides the system clock (CLK).
0	(Note) X	IDLE	Stops the system clock (CLK), but keeps the oscillator operation. The CLK is kept low in this mode.
1	0	STOP	Stops all the internal operation and the CLK is kept low.

Note) X= Don't care

TABLE 1. OPERATION MODES

1. HALT OPERATION IN EACH MODE

(1) RUN MODE (MS1=1, MS2=1)

Figure 1 shows a basic timing when HALT instruction is executed. When Z80 CPU fetches the OPcode of HALT instruction (76H) from program memory, $\overline{HALT}$ signal goes active ("0" level) at the timing synchronized with the falling edge of T4 clock cycle and it shows that Z80 CPU is in the HALT state. In this mode, T6497 always provides the CLK.

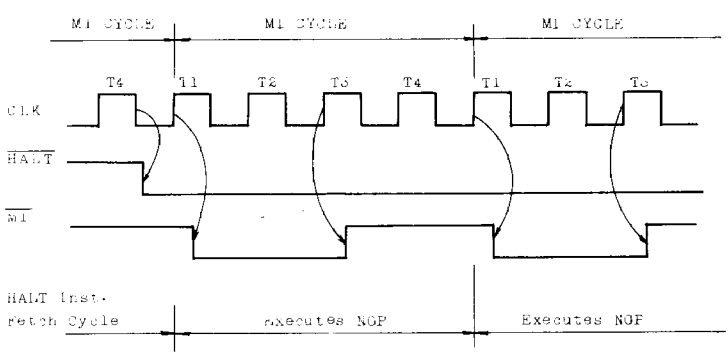


FIGURE 1. RUN MODE

(2) IDLE MODE (MS1=0, MS2= don't care)

Figure 2 shows a basic timing when HALT instruction is executed in Idle Mode. When Z80 CPU fetches the OPcode of HALT instruction (76H) from program memory, $\overline{HALT}$ signal goes active at the timing synchronized with the falling edge of T4 clock cycle and it shows that Z80 CPU is in the HALT state.

T6497 stops providing the CLK at low level state during the T4 clock cycle of the following machine cycle next to OPcode fetch cycle of HALT instruction.

A rising edge of $\overline{M1}$ signal during active $\overline{HALT}$ signal makes the T6497 stop the CLK.

However the internal oscillator continuously works.

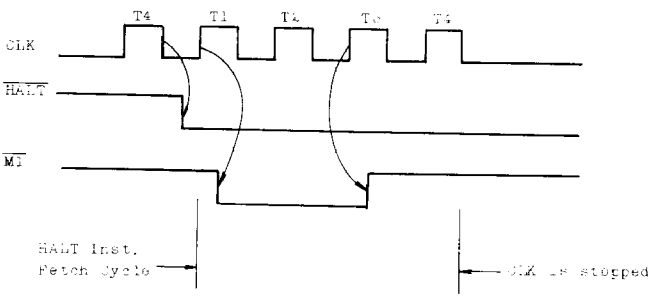


FIGURE 2. CLK STOP SEQUENCE IN IDLE/STOP MODE

(3) STOP MODE (MS1=1, MS2=0)

The same function as IDLE MODE is implemented when $\overline{HALT}$ instruction is executed. (See figure 2.)
Only difference from IDEL MODE is that the T6497 completely stops its operation.

2. CLK RESTART SEQUENCE

There are three inputs to resume the CLK. $\overline{\text{RSTI1}}$ (level trigger), $\overline{\text{RSTI2}}$ (edge trigger) or $\overline{\text{RESET}}$ (level trigger) can be used.

(1) IDLE MODE

Figure 3 shows the sequence to resume the CLK in IDLE MODE. IN IDLE MODE, the CLK will resume in small delay when a signal to terminate is generated as the internal oscillator is working.

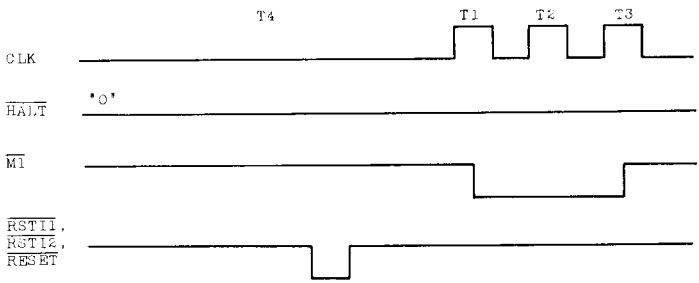


FIGURE 3. CLK RESTART SEQUENCE IN IDLE MODE.

(2) STOP MODE

Figure 4 shows the sequence to resume the CLK in STOP MODE. As the T6497 needs warming-up time to stabilize the frequency it uses the counter when a restart signal is generated.

DS (Divider Select) input must be used to determine warming-up time. External crystal frequency is devided by either 2^{17} or 2^{14}.

Figure 5 shows the block diagram regarding counter and Table 2 illustrates the warming-up time.

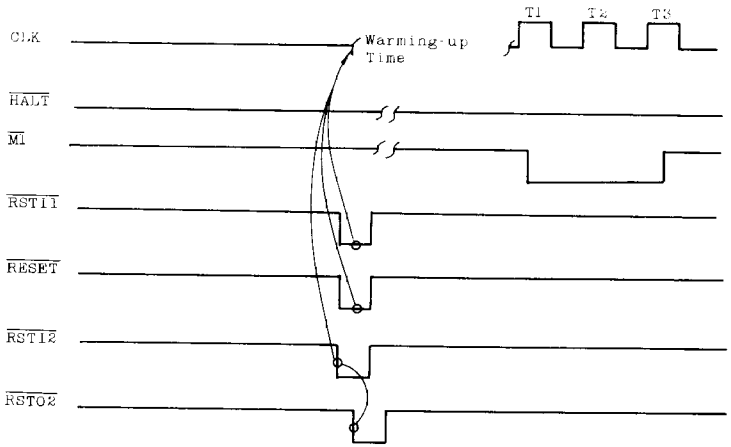


FIGURE 4. CLK RESTART SEQUENCE IN STOP MODE.

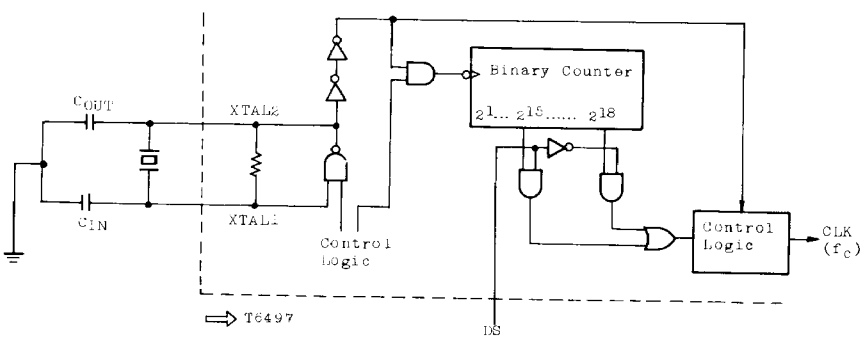


FIGURE 5. BLOCK DIAGRAM of COUNTER and CONTROL LOGIC.

DS	Counter Output	Warming-up Time		
		fXTAL=4MHz	fXTAL=2.5MHz	fXTAL=400kHz
0	2^{18}	≒ 32.8ms	≒ 52.4ms	≒ 328ms
1	2^{15}	≒ 4 ms	≒ 6.6ms	≒ 40ms

TABLE 2. WARMING-UP TIME IN STOP MODE.

Note 1)

Note that either interrupt input or $\overline{\text{RESET}}$ input must be generated to terminate the HALT state of Z80 CPU, where CLK is stopped at a low level during T4 state, in either IDLE MODE or STOP MODE.

(1) In case of $\overline{\text{RESET}}$ input signal is connected with both Z80 CPU $\overline{\text{RESET}}$ terminal and T6497 $\overline{\text{RESET}}$ terminal

$\overline{\text{RESET}}$ input signal to Z80 CPU must be kept active (Low) during at least three clock cycles. When $\overline{\text{RESET}}$ input signal goes inactive, CPU fetches the first OPcode from address 0000H after at least two dummy clock cycles. Thus CPU will terminate HALT state

Note that if $\overline{\text{RESET}}$ input is connected with both Z80 CPU $\overline{\text{RESET}}$ terminal and T6479 $\overline{\text{RESET}}$ terminal, the $\overline{\text{RESET}}$ signal should be active for enough period to reset the Z80 CPU surely at power on reset. (See Figure 6.)

(2) In case of using an interrupt signal

Figure 7 shows the timing to resume the CLK and to terminate HALT state by an interrupt signal.
$\overline{\text{RSTI1}}$ or $\overline{\text{RSTI2}}$ input makes T6497 resume the CLK. And then an interrupt signal ($\overline{\text{INT}}$ or $\overline{\text{NMI}}$) must be generated to terminate HALT state.
Note that Z80 CPU in HALT state executes NOP instruction unless an interrupt is recognized.

a) In case of using $\overline{\text{NMI}}$

$\overline{\text{NMI}}$ of Z80 CPU is an input (edge trigger) with a latch. If active (low) $\overline{\text{NMI}}$ signal is accepted prior to sampling timing for an interrupt request signal, Z80 CPU recognizes $\overline{\text{NMI}}$. $\overline{\text{RSTI2}}$ of T6497 may be used as $\overline{\text{NMI}}$ input, since $\overline{\text{RSTI2}}$ has a latch and $\overline{\text{RSTO2}}$ may be connected with $\overline{\text{NMI}}$ input of Z80 CPU.

b) In case of using $\overline{\text{INT}}$

In maskable interrupt ($\overline{\text{INT}}$), interrupt enable flip flop (IFF) must be set by software before receiving an interrupt signal.

Figure 7 shows the timing when an interrupt signal is connected with both $\overline{\text{RSTI1}}$ terminal of T6497 and $\overline{\text{INT}}$ terminal of Z80 CPU.

Note 2)

The internal counter of T6497 to determine warming-up time is not used in stop mode when $\overline{\text{RESET}}$ input is activated to resume the clock, so Z80 CPU may not restart properly due to unstable clock when the oscillator restarts. Therefore connect $\overline{\text{RESET}}$ input of T6497 with that of Z80 CPU when $\overline{\text{RESET}}$ input of T6497 is used to restart the clock in stop mode. Also it is suggested that $\overline{\text{RESET}}$ input be kept low for enough period to initialize Z80 CPU.

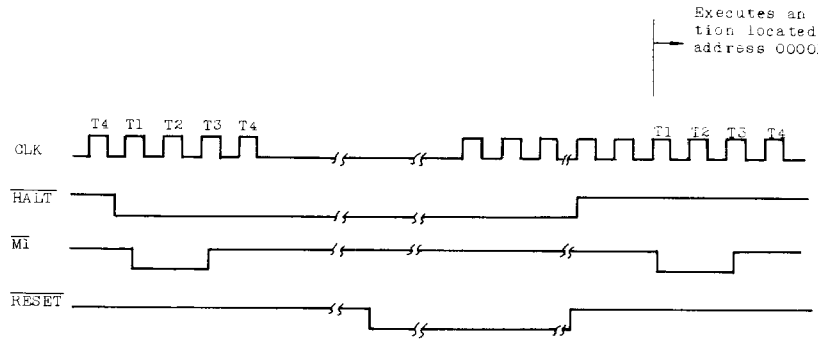


FIGURE 6. EXAMPLE of RESUMING CLK by $\overline{\text{RESET}}$

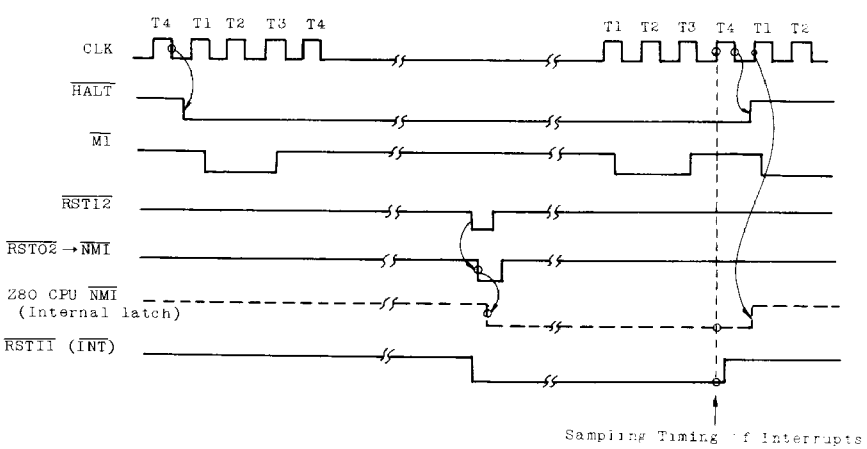


FIGURE 7. EXAMPLE of RESUMING CLK by $\overline{\text{RSTII}}$ or $\overline{\text{RSTI2}}$