SIEMENS

ICs for Communications

ISDN Subscriber Access Controller
for U_{PN}-Interface Terminals
ISAC®-P TE
PSB 2196

User's Manual 10.94

PSB 2196 Revision History:	Original Version 10.94
Previous Releases:	
Page	Subjects (changes since last revision)

Data Classification

Maximum Ratings

Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

Operating Range

In the operating range the functions given in the circuit description are fulfilled.

For detailed technical information about **"Processing Guidelines"** and **"Quality Assurance"** for ICs, see our **"Product Overview"**.

Edition 10.94

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1 Introduction

The PSB 2196, ISDN Subscriber Access Controller for U_{PN}-interface ISAC-P TE, implements the subscriber access functions for a digital terminal to be connected to a two-wire U_{PN}-interface.

The PSB 2196 ISAC-P TE is an optimized device for TE-applications, covering the layer-1 and -2 functions.

The PSB 2196 ISAC-P TE combines the functions of the U_{PN}-transceiver with reduced loop length (one channel of the OCTAT-P PEB 2096) and the ISDN Communications Controller (ICC, PEB 2070) onto one chip.

The microcontroller interface of the ISAC-P TE is compatible to standard multiplexed microcontrollers. In addition it provides the microcontroller clock signal as well as a supply voltage control and reset generation.

The terminal repeater function of the ISAC-P TE allows to cascade two telephones which are controlled by one U_{PN}-interface from the line card.

The PSB 2196 ISAC-P TE interfaces to voice/data devices via the IOM®-2 interface.

The PSB 2196 ISAC-P TE is a 1 micron CMOS device offered in a P-LCC-44 and P-MQFP-44 pin package. It operates from a single 5 V supply.

Note: U_{PN} in the document refers to a version of the U_{P0}-standard with a reduced loop length.

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ISDN Subscriber Access Controller for U_{PN}-Interface Terminals (ISAC®-P TE)

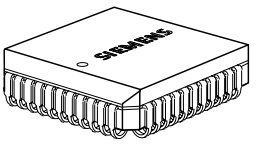
PSB 2196

Preliminary Data

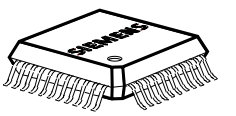
CMOS IC

1.1 Features

- Cost/performance-optimized U_{PN}-interface transceiver, compatible to PEB 2096 OCTAT-P
- HDLC-controller with 2 × 32 byte FIFO per direction
- HDLC-address recognition and control field handling compatible to PEB 2070
- IOM-2 interface for terminal application compatible to PEB 2070 ICC
- 8-bit multiplexed microprocessor interface
- 4-wire serial programming interface
- CPU-clock and reset outputs
- Test loops
- Advanced CMOS-technology
- Low power consumption: 100 mW



P-LCC-44-1

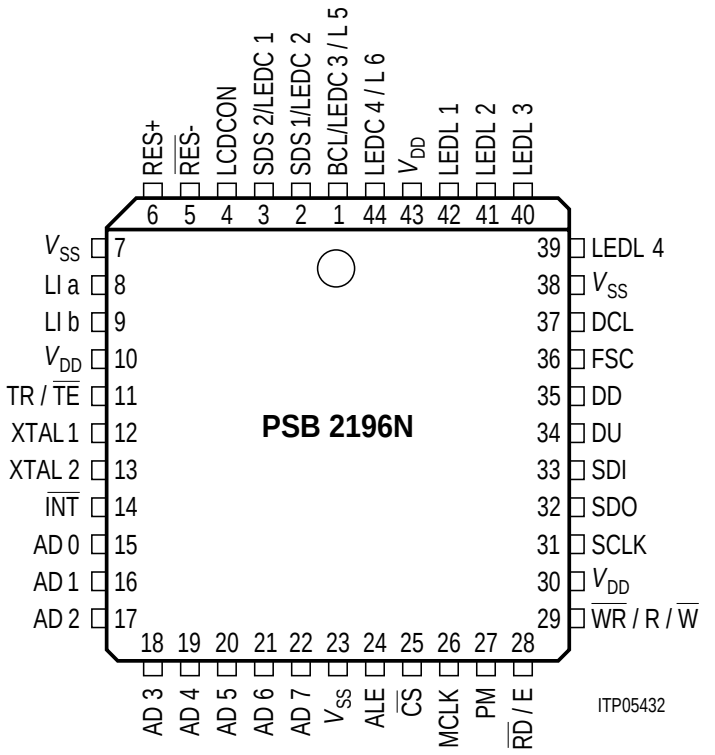


P-MQFP-44-2

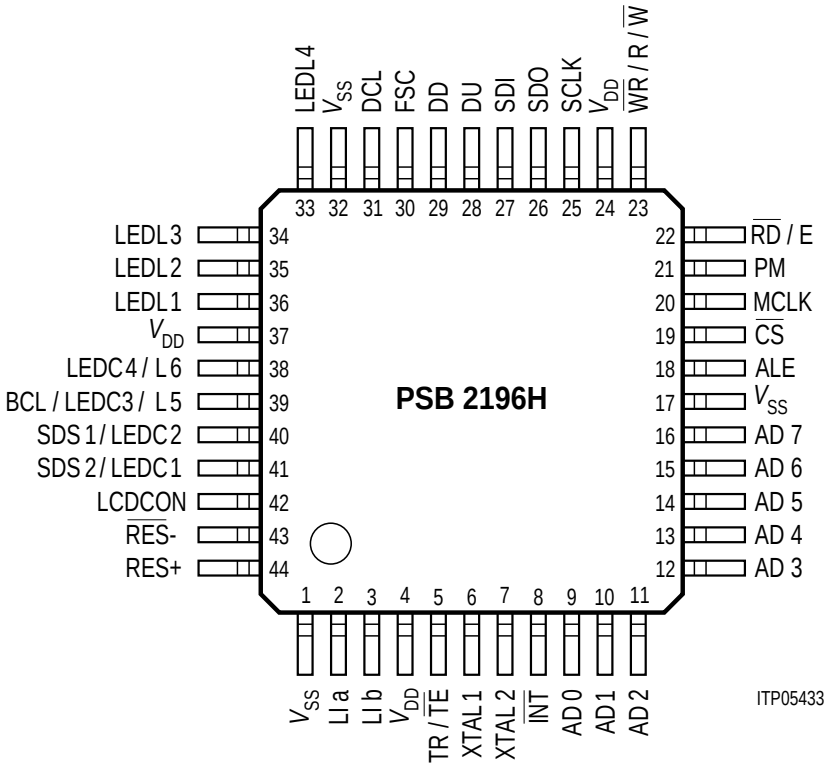
Type	Ordering Code	Package
PSB 2196 N	Q67100-H6392	P-LCC-44-1 (SMD)
PSB 2196 H	Q67100-H6391	P-MQFP-44-2 (SMD)

1.2 Pin Configurations

(top view)



P-MQFP-44-2


LEDL4
V_{SS}
DCL
FSC
DD
DU
SDI
SDO
SCLK
V_{DD}
WR / R / W
33 32 31 30 29 28 27 26 25 24 23
LEDL3 34
LEDL2 35
LEDL1 36
V_{DD} 37
LEDC4 / L6 38
BCL / LEDC3 / L5 39
SDS1 / LEDC2 40
SDS2 / LEDC1 41
LCDCON 42
RES- 43
RES+ 44
22 RD / E
21 PM
20 MCLK
19 CS
18 ALE
17 V_{SS}
16 AD 7
15 AD 6
14 AD 5
13 AD 4
12 AD 3
PSB 2196H
1 2 3 4 5 6 7 8 9 10 11
V_{SS}
LIa
LIb
V_{DD}
TR / TE
XTAL1
XTAL2
INT
AD0
AD1
AD2
ITP05433

1.3 Pin Definitions and Functions

Pin No.		TE-Mode		TR-Mode		
Pin No. P-LCC	**Pin No. P-MQFP**	**Symbol**	**Input (I) Output (O) Open Drain (OD)**	**Symbol**	**Input (I) Output (O) Open Drain (OD)**	**Function**
15 16 17 18 19 20 21 22	9 10 11 12 13 14 15 16	AD 0 AD 1 AD 2 AD 3 AD 4 AD 5 AD 6 AD 7	I/O I/O I/O I/O I/O I/O I/O I/O	V_{SS} V_{SS} V_{SS} V_{SS} V_{SS} V_{SS} V_{SS} V_{SS}	I I I I I I I I	**TE-Mode: Multiplexed Bus Mode: Address/Data Bus.** Transfers addresses from the microprocessor to the ISAC-P TE and data between the microprocessor and the ISAC-P TE. AD0–7 have programmable pull-up resistors which are active after reset. **TR-Mode:** Have to be connected to V_{SS}.
25	19	$\overline{CS}$	I	V_{DD}	I	**Chip Select:** A low level indicates a microprocessor access to the ISAC-P TE.
29	23	R/$\overline{W}$	I	V_{DD}	I	**Motorola Bus Mode: Read/Write.** A high level indicates a read access to the ISAC-P TE, a low level indicates a write access to the ISAC-P TE. The state of R/$\overline{W}$ is evaluated while E is high.
29	23	$\overline{WR}$	I			**Intel Bus Mode: Write.** A low level indicates a write access to the ISAC-P TE.
28	22	E	I	V_{DD}	I	**Motorola Bus Mode: Enable.** The low period is used to setup the address and control lines. The high period indicates the register access. The falling edge marks the end of a valid read or write access.
28	22	$\overline{RD}$	I			**Intel Bus Mode: Read.** A low level indicates a read access to the ISAC-P TE.
14	8	$\overline{INT}$	OD			**Interrupt Request.** INT becomes active if the ISAC-P TE requests an interrupt.

Pin Definitions and Functions (cont'd)

Pin No.		TE-Mode		TR-Mode		
Pin No. P-LCC	**Pin No. P-MQFP**	**Symbol**	**Input (I) Output (O) Open Drain (OD)**	**Symbol**	**Input (I) Output (O) Open Drain (OD)**	**Function**
24	18	ALE	I	TCM	I	**Address Latch Enable/T-Channel Mapping.** Selects between parallel and serial microprocessor interface. The falling edge latches the contents of the AD0–AD5 lines as register address and selects parallel microprocessor interface. **TR-Mode:** Selects whether the downstream T-bit is controlled by the S/G-bit or set to "0".
26	20	MCLK	O			**Microprocessor Clock.** Clock output for the microcontroller.
6	44	RES+	O	RES	I	**Reset +.** High active reset output (TE), high active reset input (TR).
5	43	$\overline{\text{RES}}$c–	O (OD)			**Reset –.** Low active reset output (TE, open drain), not used in TR-mode.
27	21	PM	I	V_{DD} or V_{SS}	I	**Processor Mode.** PM = 0 selects Intel control lines. PM = 1 selects Motorola control lines.
11	5	TR/$\overline{\text{TE}}$ (V_{SS})	I	TR/$\overline{\text{TE}}$ (V_{DD})	I	**Terminal Repeater/TE-Mode Selection.** Selects terminal repeater mode (V_{DD}) or TE-mode (V_{SS}).
33	27	SDI	I	V_{SS}	I	**Serial Data.** In Receive data line of the serial control interface. Peripheral input if the parallel microprocessor interface is selected.
32	26	SDO	O (OD)	V_{SS}	I	**Serial Data Out.** Transmit data line of the serial control interface. Peripheral output if the parallel microprocessor interface is selected.
31	25	SCLK	I	V_{SS}	I	**Serial Clock.** Clock signal of the serial control interface. Peripheral input if the parallel microprocessor interface is selected.

Pin Definitions and Functions (cont'd)

Pin No.		TE-Mode		TR-Mode		
Pin No. P-LCC	**Pin No. P-MQFP**	**Symbol**	**Input (I) Output (O) Open Drain (OD)**	**Symbol**	**Input (I) Output (O) Open Drain (OD)**	**Function**
35 34	29 28	DD DU	I/O (OD) I/O (OD)	DD DU	I/O (OD) I/O (OD)	**Data Downstream.** **Data Upstream.** Transfer the data of the IOM-2 interface.
12 13	6 7	XTAL 1 XTAL 2	I O	XTAL 1 XTAL 2	I O	**Crystal 1.** Connection for a crystal or used as external clock input. **Crystal 2.** Connection for a crystal. Not connected if an external clock is supplied on XTAL1. (TE- & TR-mode)
37	31	DCL	O	DCL	I	**Data Clock.** IOM-interface clock signal. Clock frequency is twice the IOM-data rate. TE: clock output IOM-2: 1536 kHz TR: clock input IOM-2: 1536 kHz
36	30	FSC	O	FSC	I	**Frame Sync.** **TE:** Frame synchronization output. **TR:** Input synchronization signal IOM-2 mode.
8 9	2 3	LIa LIb	I/O I/O	LIa LIb	I/O I/O	**Line interface a.** **Line interface b.** U_{PN}-transceiver signals.
1	39	BCL	O			**Bit Clock.** IOM-bit clock signal (768 MHz). Multiplexed on LEDC3/L5. Selection is done by GCR:LLC bit.
2 3	40 41	SDS1 SDS2	O O			**Serial Data Strobe 1, 2.** Strobe signal to indicate 64 or 128 kbit/s time-slot. Multiplexed on LEDC1, 2. Selection is done by GCR:LLC bit.

Pin Definitions and Functions (cont'd)

Pin No.		TE-Mode		TR-Mode		
Pin No. P-LCC	**Pin No. P-MQFP**	**Symbol**	**Input (I) Output (O) Open Drain (OD)**	**Symbol**	**Input (I) Output (O) Open Drain (OD)**	**Function**
42 41 40 39	36 35 34 33	LEDL 1 LEDL 2 LEDL 3 LEDL 4	O O O O			**LED-Line 1.** **LED-Line 2.** **LED-Line 3.** **LED-Line 4.** Driver for each line of the LED matrix.
3 2 1 44	41 40 39 38	LEDC 1 LEDC 2 LEDC 3/ L5 LEDC 4/ L6	O O O O			**LED-Column 1.** **LED-Column 2.** **LED-Column 3 / LED Line 5.** **LED-Column 4 / LED Line 6.** Driver for each column of the LED matrix (4 × 4) or line driver 5 and 6 two multiplexed column drivers (6 × 4) if selected by GCR:LLC.
4	42	LCDCON	O			**LCD-Contrast Control.** Output of a pulse width modulator if selected by GCR:LLC.
10, 30 43	4, 24, 37	V_{DD}		V_{DD}		**Power Supply** + 5 V ± 5 % (U_{PN}-specification)
7, 23, 38	1, 17, 32	V_{SS}		V_{SS}		**Ground.**

Note: Pin 7 and 10 (MQFP: 1 and 4) are supply pins to the U_{PN} transceiver.

1.4 Logic Symbol

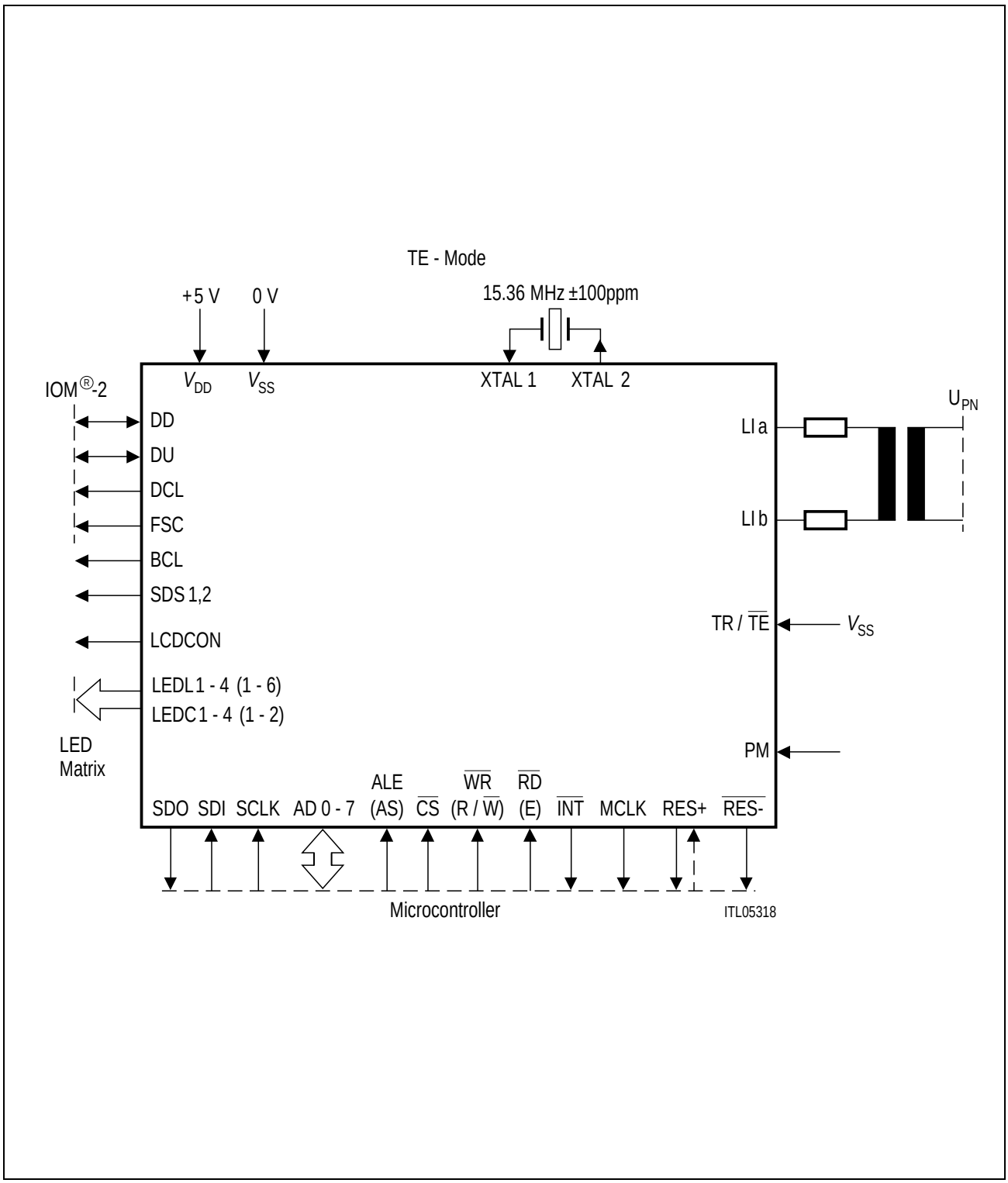


Figure 1
Logic Symbol of the ISAC®-P TE
TE-Mode

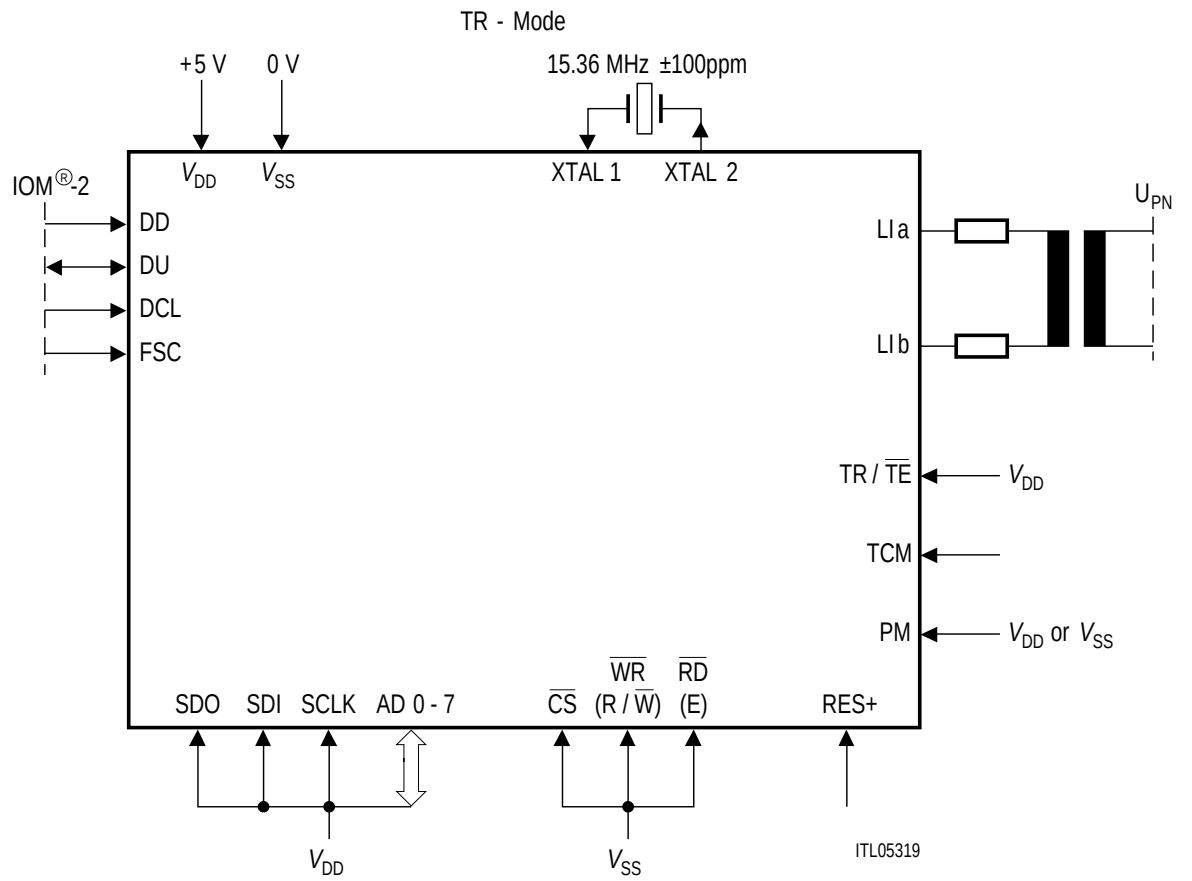


Figure 2
Logic Symbol of the ISAC®-P TE
TR-Mode

1.5 Functional Block Diagram

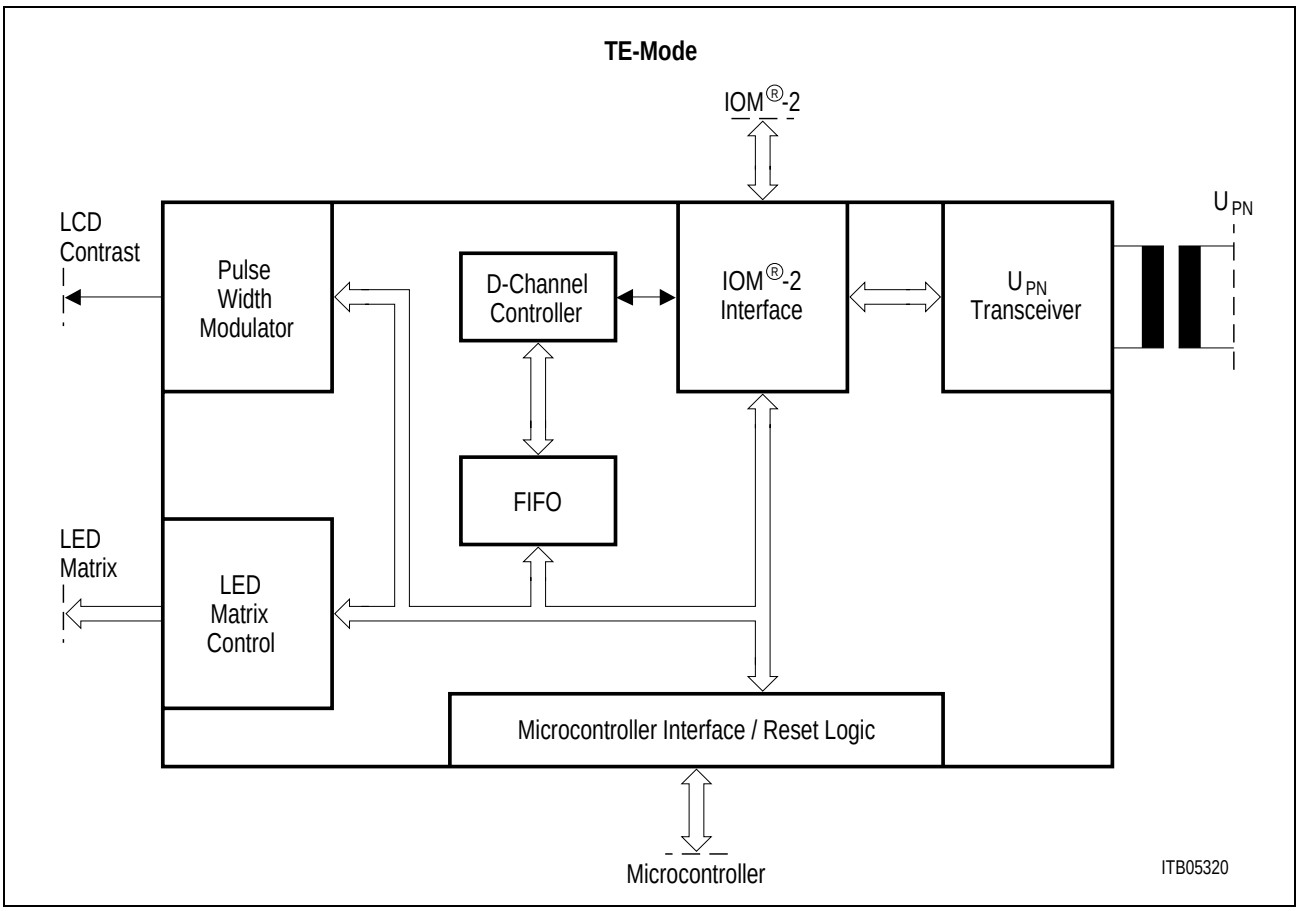


Figure 3
Block Diagram of the ISAC®-P TE
TE-Mode

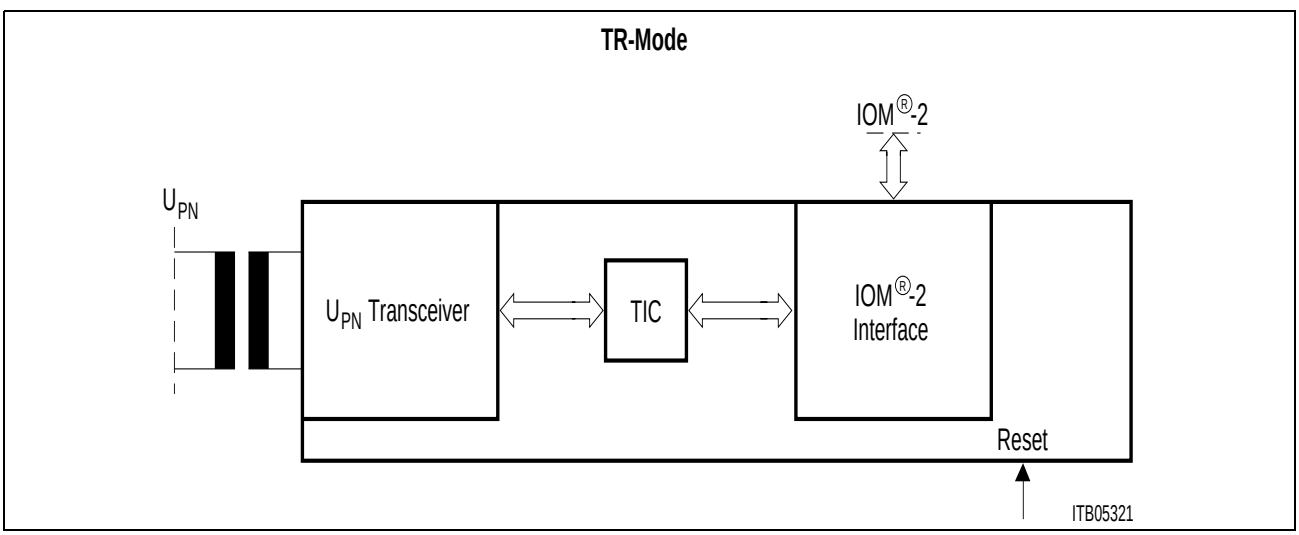


Figure 4
Block Diagram of the ISAC®-P TE
TR-Mode

1.6 System Integration

1.6.1 Low Cost Digital Telephone Using the ISAC®-P TE

A low cost digital telephone behind a PBX consists of the ISAC-P TE, a standard codec and a microcontroller with on-chip ROM. This architecture is shown in **figure 5**. The ISAC-P TE performs the conversion between the U_{PN}-interface and the IOM-2 interface of the B-channel and D-channel information. The D-channel signaling information is processed by an HDLC-controller inside the ISAC-P TE which provides 2×32 byte FIFOs in each direction. The serial strobe signal controls the time-slot which is used by the codec.

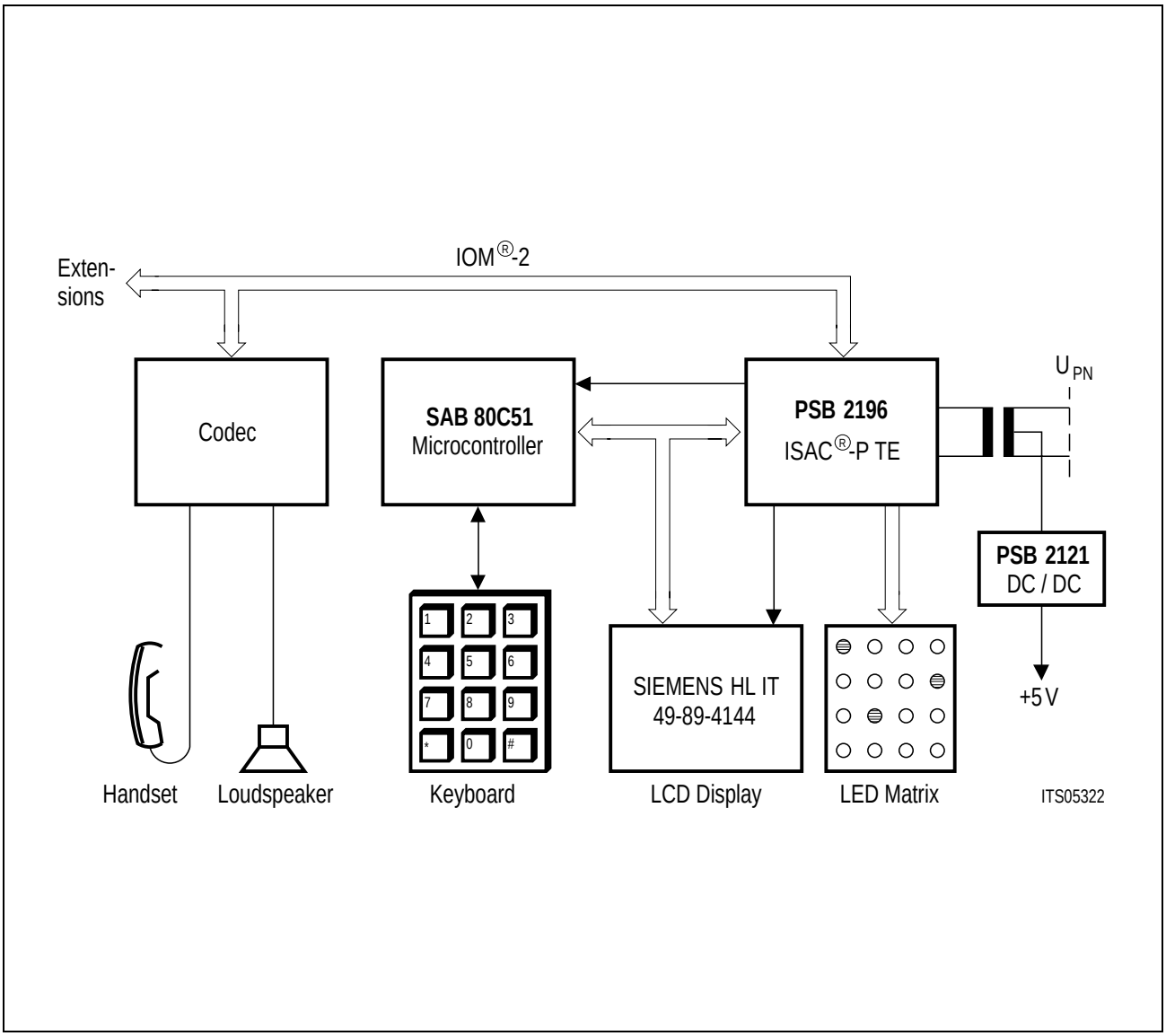


Figure 5
Low Cost Digital Telephone Using the ISAC®-P TE

1.6.2 Low Cost Digital Feature Phone Using the ISAC®-P TE

A low cost digital feature phone behind a PBX consists of the ISAC-P TE, a feature codec like the ARCOFI®-SP PSB 2165/63 and a microcontroller with on-chip ROM. This architecture is shown in **figure 6**. The ISAC-P TE performs the conversion between the U_{PN}-interface and the IOM-2 interface of the B-channel and D-channel information. The D-channel signaling information is processed by an HDLC controller inside the ISAC-P TE which provides 2×32 byte FIFOs in each direction. A pulse width modulated signal can be used to control the contrast of an LCD-display. The LED-matrix is controlled by the ISAC-P TE.

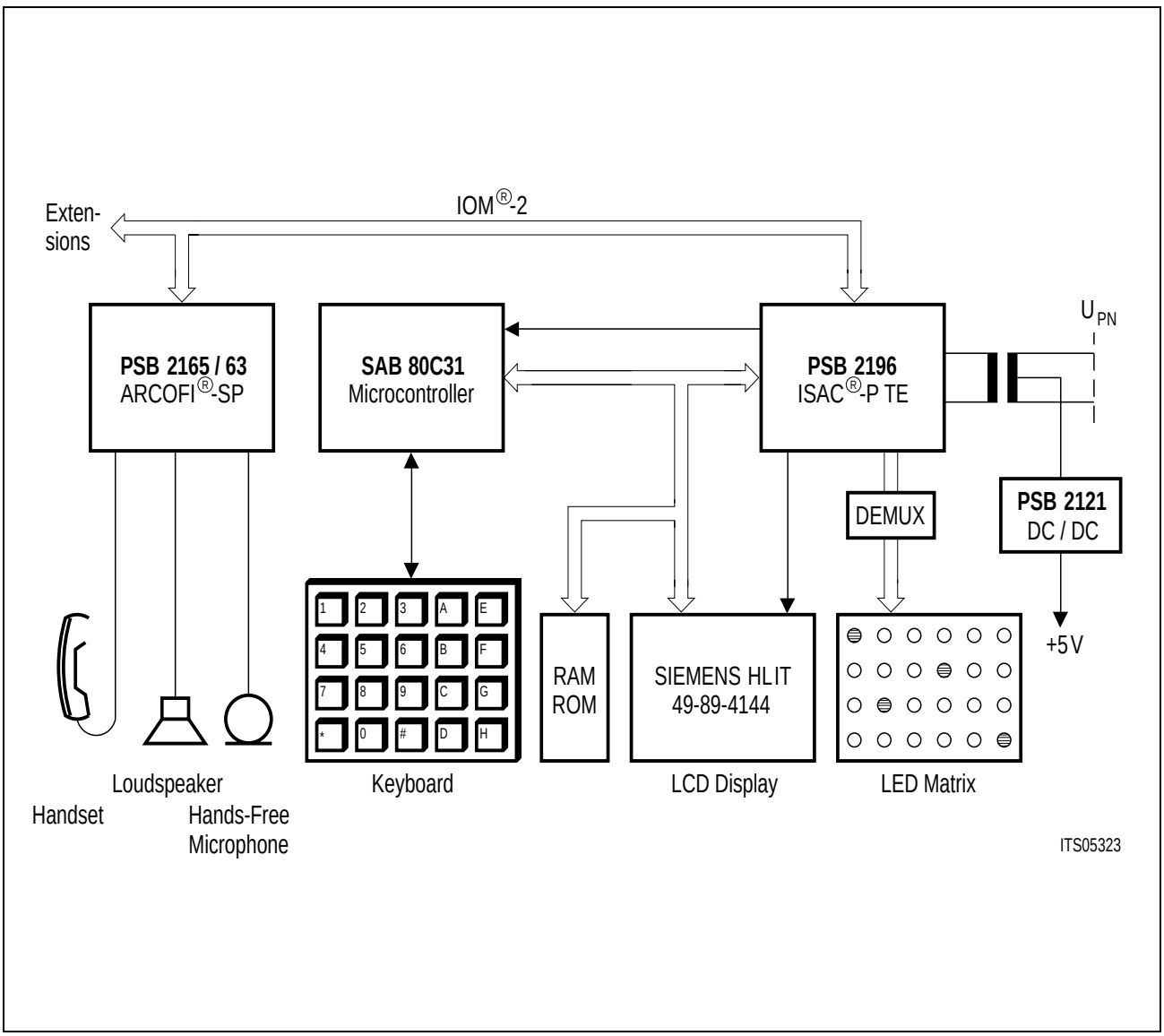


Figure 6
Low Cost Digital Feature Phone Using ISAC®-P TE

1.6.3 U_{PN}-Terminal Repeater

The ISAC-P TE is designed to operate as a U_{PN}-terminal repeater (**figure 7**). It provides a mechanism to control further U_{PN}-terminals by using the T-channel of the U_{PN}-interface and the TIC-bus on the IOM-2 interface.

The terminal repeater function allows to cascade two U_{PN}-telephones up to a loop length of 100 m.

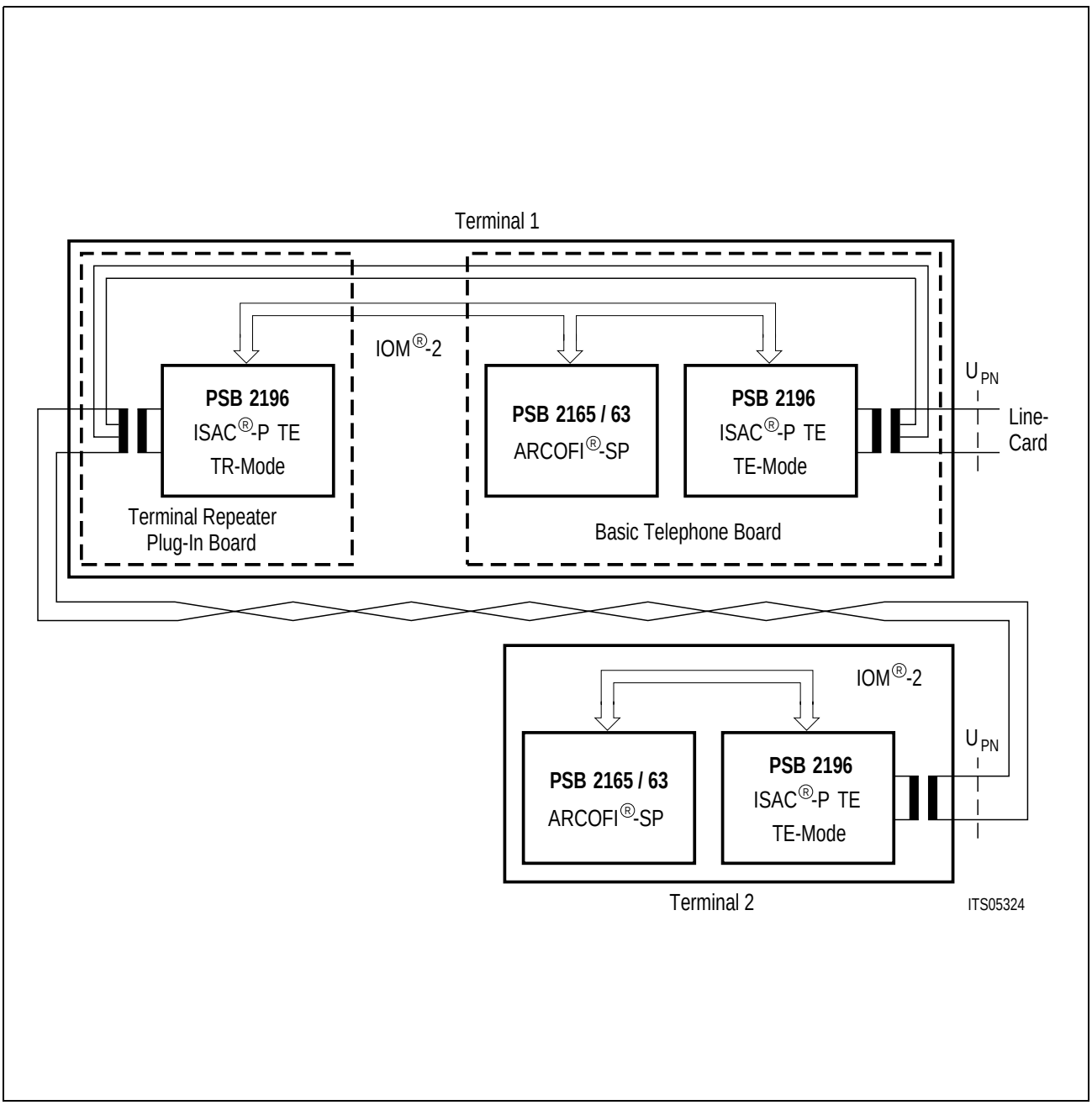


Figure 7
U_{PN}-Terminal Repeater

1.6.4 Network Termination Module

The combination of the PEB 2091 (IEC-Q) and PSB 2196 (ISAC-P TE) allows the extention of the loop length up to 8 km. The ISAC-P TE provides the regular U_{PN}-interface to connect standard U_{PN}-terminals to it.

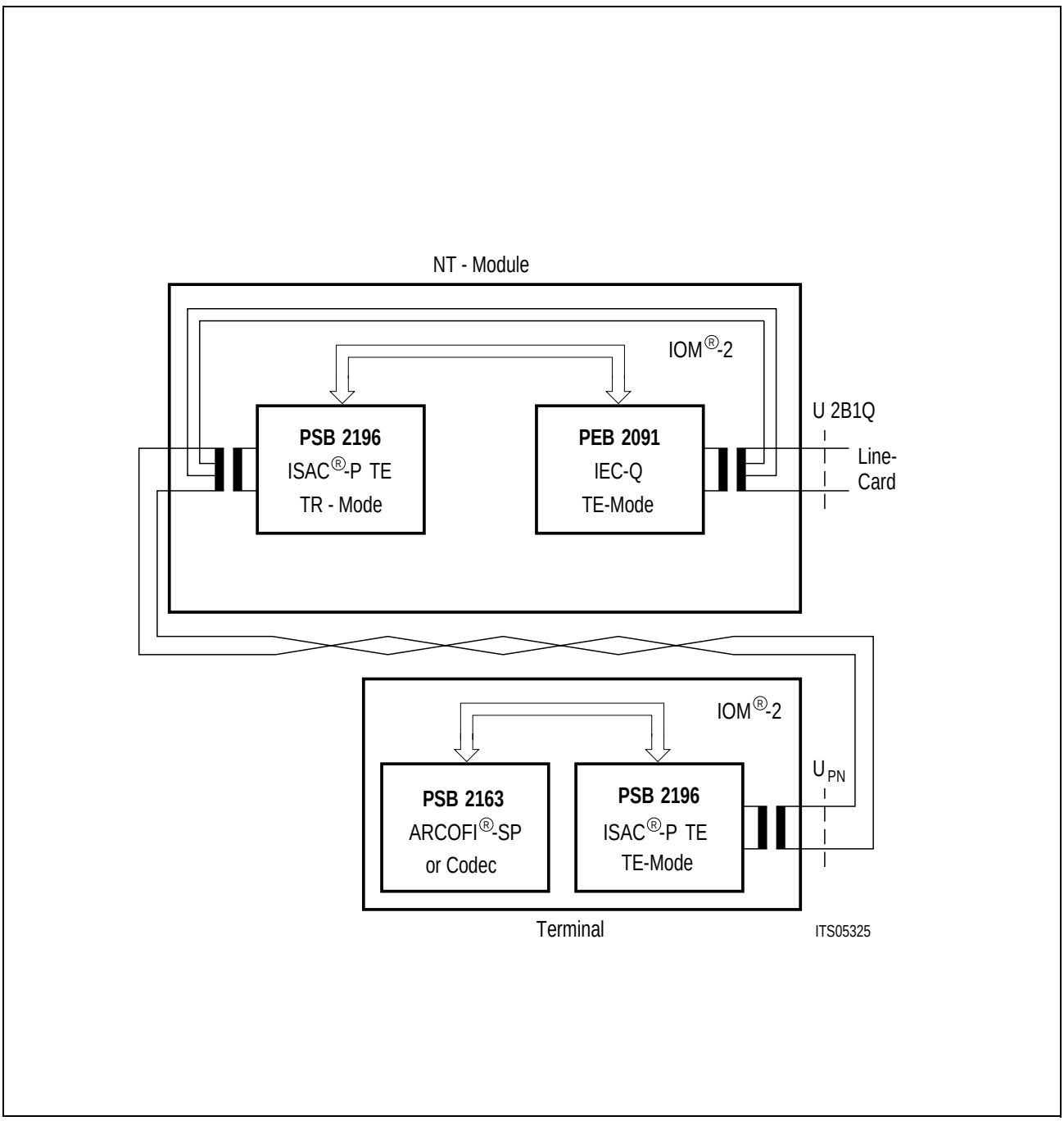


Figure 8
Network Termination Using the ISAC®-P TE

1.6.5 S/T-Interface Option

A telephone based on the ISAC-P TE may be extended by an S/T-interface option to connect standard S/T-interface terminals like ISDN PC-cards or videophones to it (**figure 9**). This option uses the PEB 2081 S-interface transceiver device for the S/T-interface. The D-channel arbitration between the D-channel controller of the ISAC-P TE and the upstream D-channel data of the S/T-interface is done by the TIC-bus of the IOM-2 interface.

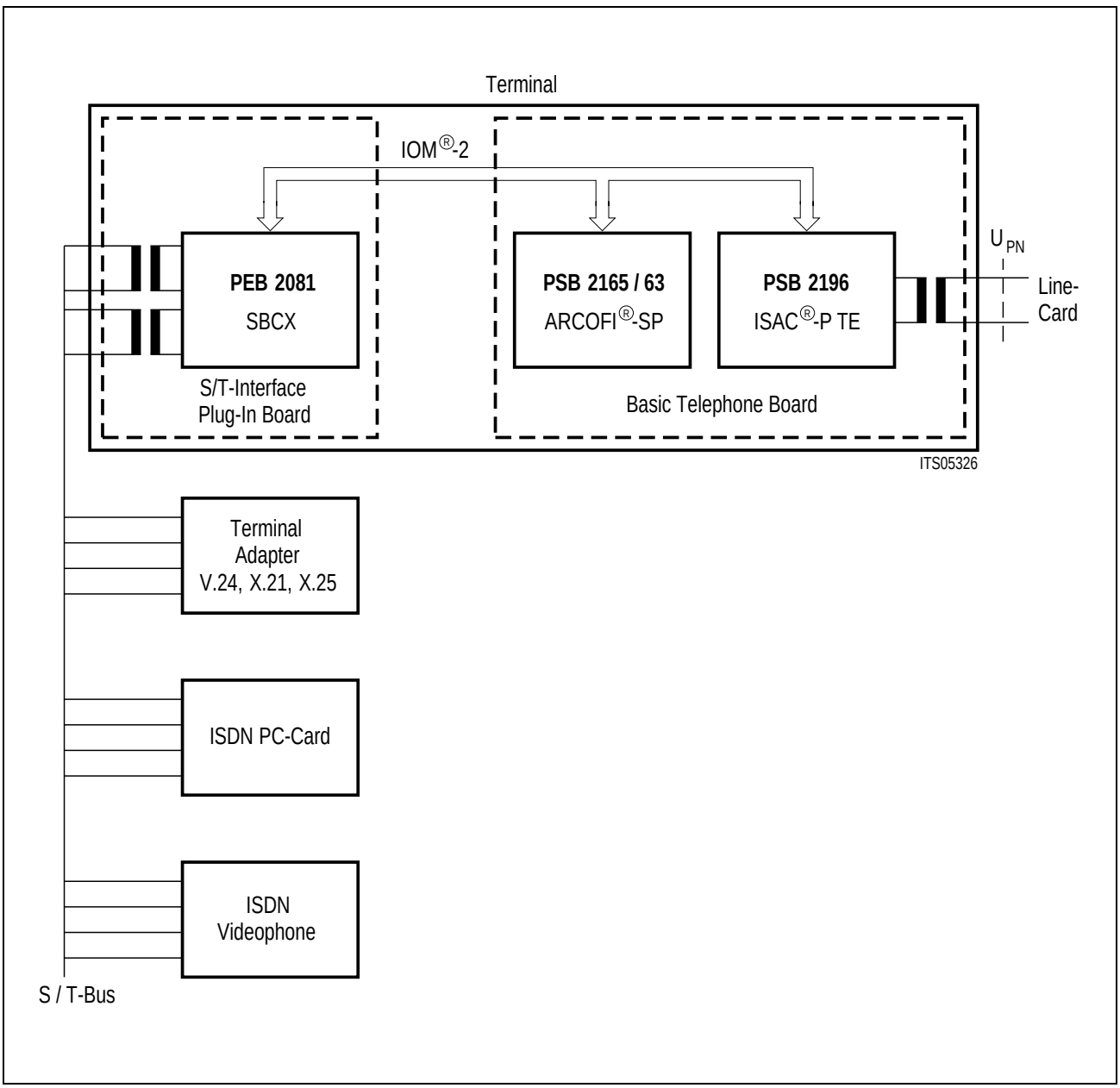


Figure 9
U_{PN}-Telephone with S/T-Interface Option

2 Functional Description

Selection between TE- and TR-Mode

The selection between TE- and TR-mode is done via the TR/$\overline{\text{TE}}$-mode input. If it is connected to V_{SS} (GND), the terminal equipment mode is selected.

The TR-mode remains as a stand-alone function with the requirement that AD0-7, SDI, SDO and SCLK must be connected to V_{SS} and TR/$\overline{\text{TE}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{CS}}$ must be connected to V_{DD}.

2.1 Terminal Equipment (TE) Mode

2.1.1 General Functions and Device Architecture (TE-mode)

Figure 10 depicts the detailed architecture of the PSB 2196 ISAC-P TE in TE-mode:

- U_{PN}-interface transceiver, functionally fully compatible to both PEB 2095 IBC and PEB 2096 OCTAT-P
- Multiplexed microprocessor interface (Intel/Motorola control lines) or serial control interface including reset and clock generation
- HDLC-controller with 2×32 byte FIFO per direction
- HDLC-address recognition and control field processing compatible to PEB 2070
- IOM-2 interface for terminal application compatible to PEB 2070 ICC
- Pulse width modulator for LCD-contrast control
- LED-matrix control (4×4, 6×4 LEDs)
- Watchdog timer

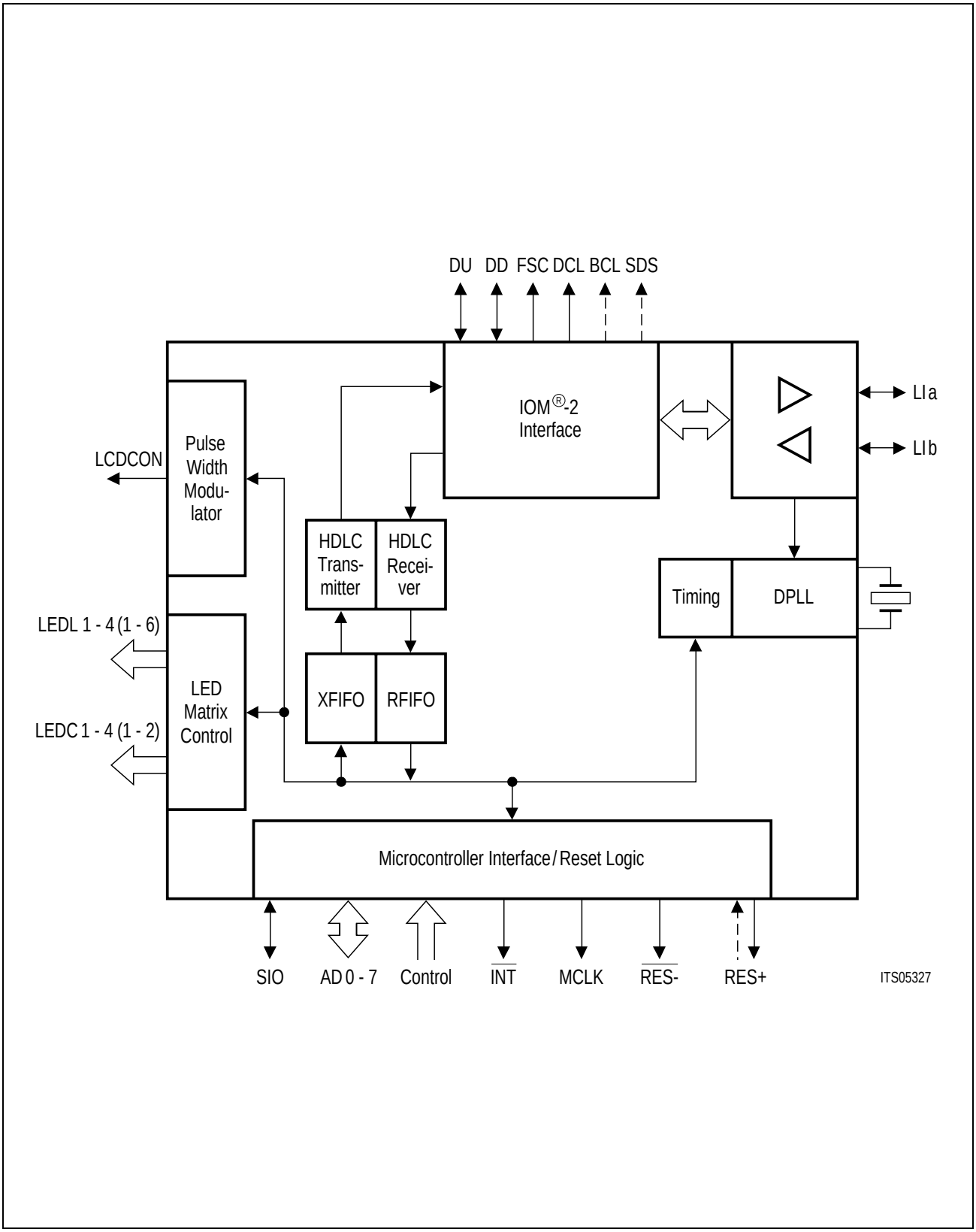


Figure 10
Device Architecture of the ISAC®-P TE in TE-Mode

2.1.2 Clock Generation (TE-mode)

In TE-mode, the oscillator is used to generate a 15.36-MHz clock signal. This signal is used by the DPLL to synchronize the IOM-2 clocks to the received U_{PN}-frames. The oscillator clock is divided by 2 to generate a 7.68-MHz clock which drives the remaining functions. The prescaler for the microcontroller clock divides the 7.68-MHz clock by 1, 2, 8 or 16. Note that only the IOM-2 clock signals (FSC, DCL, BCL) are stopped during the power-down state. The oscillator and the other modules remain active all the time.

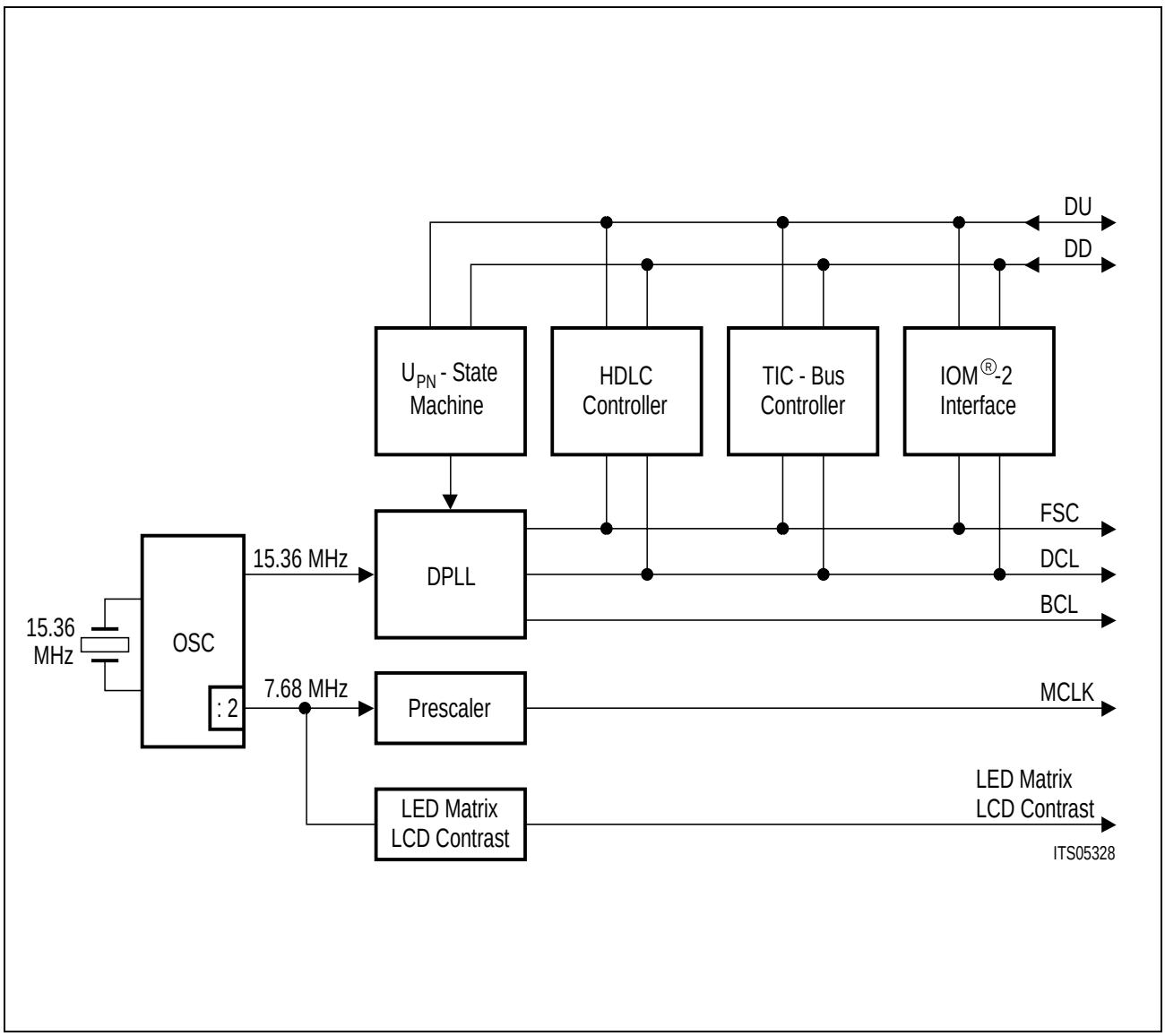


Figure 11
Clock Generation in TE-Mode

2.1.3 Interfaces (TE-mode)

The PSB 2196 ISAC-P TE serves four interfaces in TE-mode:

- Parallel/Serial microcontroller interface for higher layer functions incl. reset and microcontroller clock generation
- IOM-2 interface: between layer-1 and layer-2 and as a universal backplane for terminals
- U_{PN}-interface towards the two-wire subscriber line
- Pulse width modulator for LCD-contrast control
- LED-matrix control

2.1.3.1 Microprocessor Interface

The ISAC-P TE is programmable via an 8-bit parallel microprocessor interface or a serial control interface. Easy and fast microprocessor access is provided by 6-bit address decoding on the chip.

Microprocessor Interface Modes

Selection between three interface modes is done by the ALE-input together with the PM-input. A falling edge on the ALE-input selects the parallel microprocessor interface. The control line configuration is selected by the PM-input between Intel/Siemens and Motorola mode. The state of the SDI, SCLK input and SDO-output is represented/ controlled by the GCR-register.

If the ALE-input is connected to V_{SS} (GND) the serial control interface is selected. The state of the !CS, !RD, !WR, PM inputs is ignored. It is recommended to connect them to V_{DD}.

Table 1
Microprocessor Interface Signals

Input: ALE	Input: PM	Bus Mode	Address Lines	Data Lines	Control Lines
ALE	V_{SS} (GND)	Intel Multiplexed	AD 0 – AD 5	AD 0 – AD 7	$\overline{RD}$, $\overline{WR}$
AS	V_{DD} (+ 5 V)	Motorola Multiplexed	AD 0 – AD 5	AD 0 – AD 7	E, R/$\overline{W}$
V_{SS}	x	Serial Control Interface	internal	internal	internal

Serial Control Interface

The serial control interface provides control of the internal register via indirect address mechanism. It consists of 5 lines: SCLK, SDI, SDO, $\overline{CS}$, $\overline{INT}$.

$\overline{CS}$ is used to start a serial access to the ISAC-P TE registers: Following a falling edge on $\overline{CS}$, the first eight bits transmitted on SDI specify the address of the register and the access mode (read/write). The subsequent eight bits read or write the contents of the selected register once the $\overline{CS}$-line becomes inactive.

The data transfer is synchronized by the SCLK-input. SDO changes with the falling edge of SCLK while the contents of SDI is latched on the rising edge of SCLK.

Figure 12 shows the timing of a serial control interface transfer.

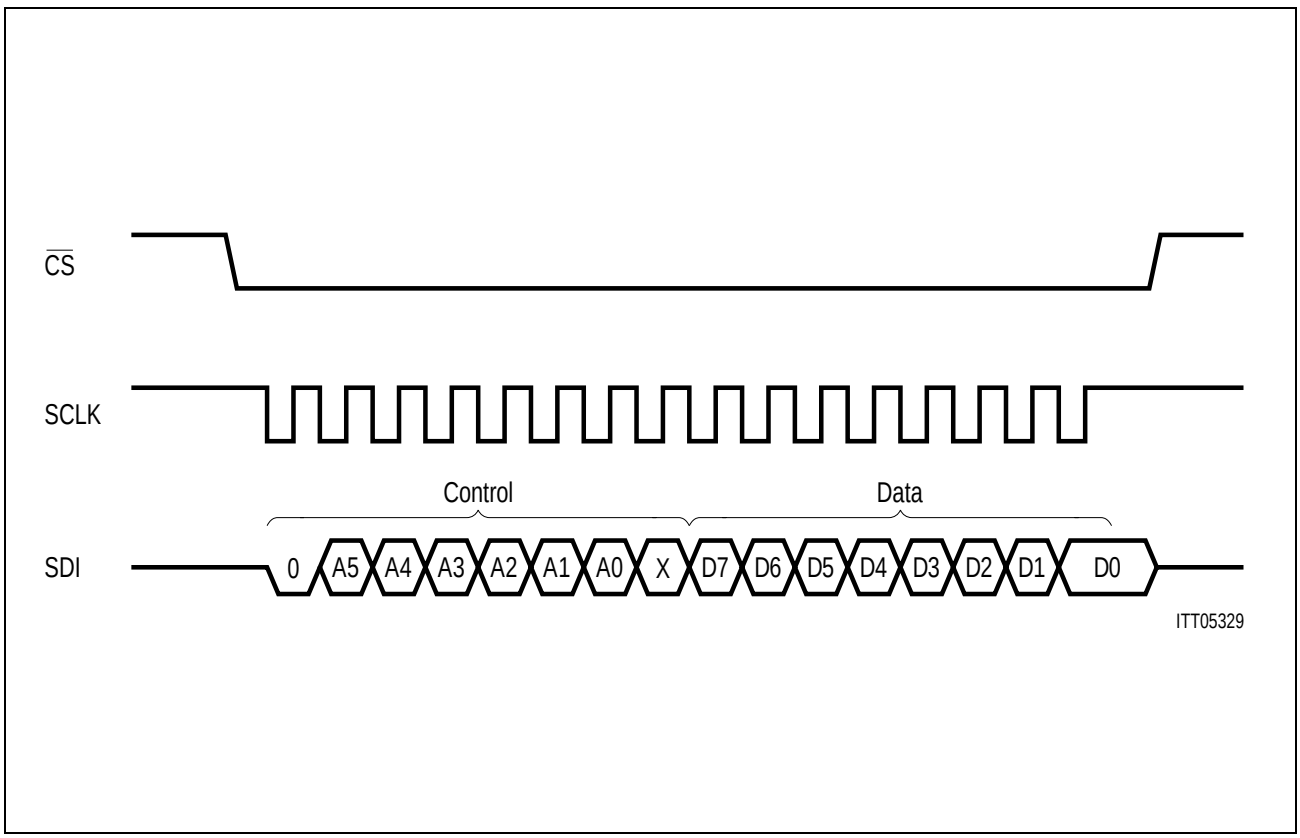


Figure 12a
Serial Control Interface Timing
Write Access

Up to 32 bytes of data may be received in one access. Following the control byte the data is transferred every eight clocks.

During a read access, only one byte can be read. Following that byte, “FF” is transmitted.

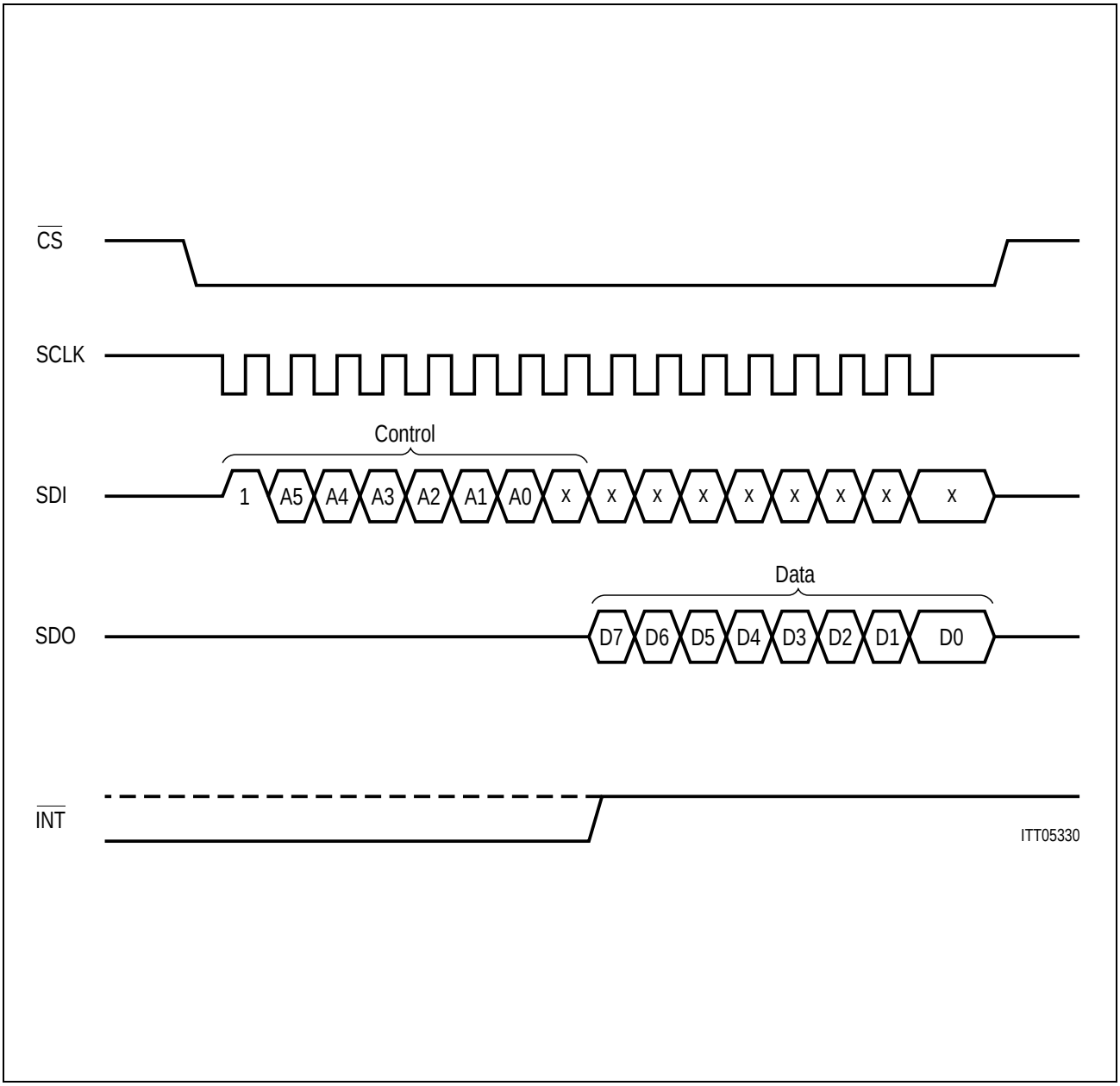


Figure 12b
Serial Control Interface Timing
Read Access

Microprocessor Clock Output

The microprocessor clock is provided by the MCLK-output. Four clock rates are provided by a programmable prescaler. These are 7.68 MHz, 3.84 MHz, 0.96 MHz, 0.48 MHz. Switching between the clock rates is based on the lowest frequency and realized without spikes.

The value after reset is 3.84 MHz.

Interrupt Output

The interrupt output is an open drain output.

Reset Logic

The ISAC-P TE provides two reset outputs which are controlled by the undervoltage detector. A second reset source is the watchdog timer and the third is a C/I-code change. The later two have to be enabled by setting the STCR:TSF to “1”. The CIX0:RSS bit selects between watchdog and C/I-code change source.

An alternative mode setting is possible to disable the undervoltage detector and to provide an external reset signal to RES +. This mode is used for the device test and is entered by setting TR/$\overline{\text{TE}}$- to TR-mode and to connect SDI, SLCK to V_{DD} and SDO to V_{SS}.

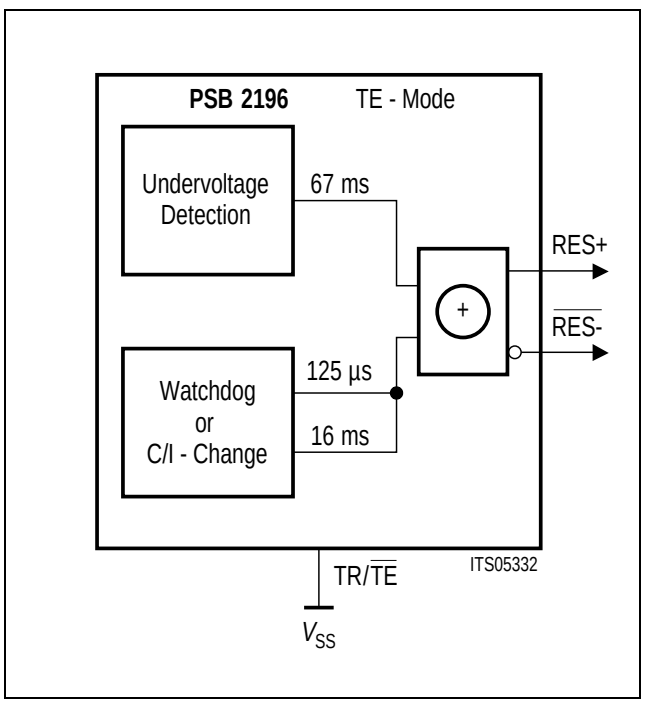


Figure 13a
Reset Source (Undervoltage detection used, no external reset source possible)

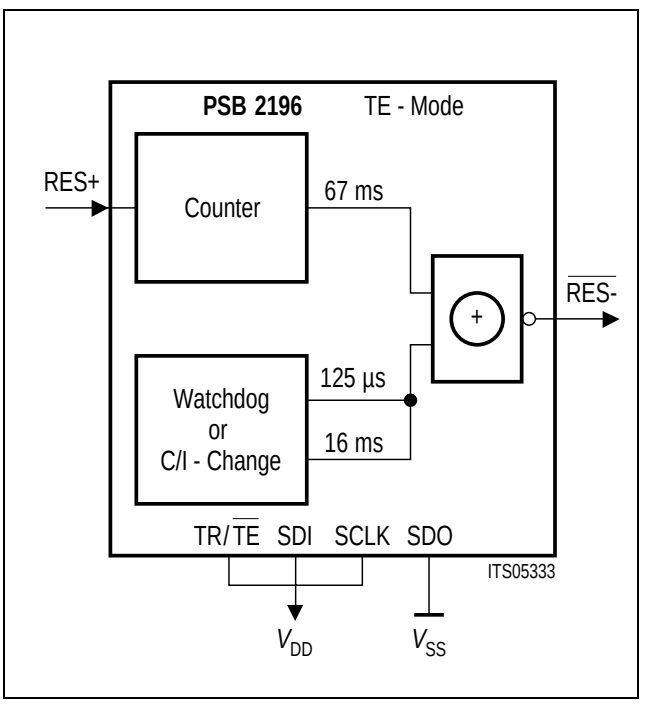


Figure 13b
Reset Source (External reset source only)

Undervoltage Detection

The undervoltage detector activates the reset signal if the supply voltage drops below the threshold level V_{TH1} and generates a reset pulse of t_r ms after the supply voltage rises above the threshold level V_{TH2}.

During power-up, the reset output is active until the threshold V_{TH2} has been reached. After that, a period of t_r is counted until the reset output becomes inactive. It stays inactive until the supply voltage drops below threshold level V_{TH1}.

While the supply voltage is below the threshold V_{TH1}, the microcontroller clock MCLK is stopped and the MCLK output remains low. If the supply voltage falls below threshold V_{TH1}, the clock is stopped immediately which may result in a shorter high period of the clock signal.

V_{TH1} has a value of 4.3 V ± 0.1 V. The threshold between V_{TH1} and V_{TH2} is in the range of 70 … 230 mV. t_r has a value of 67 ms. The minimum period (t_{min}) for the undervoltage detection is 10 µs ± 10 %. The delay (t_d) after threshold voltages have been passed is maximum 1 µs.

During power-up, the reset pulse may be extended due to the oscillator start until a stable 15.36-MHz clock is achieved.

Figure 14 shows the undervoltage control timing.

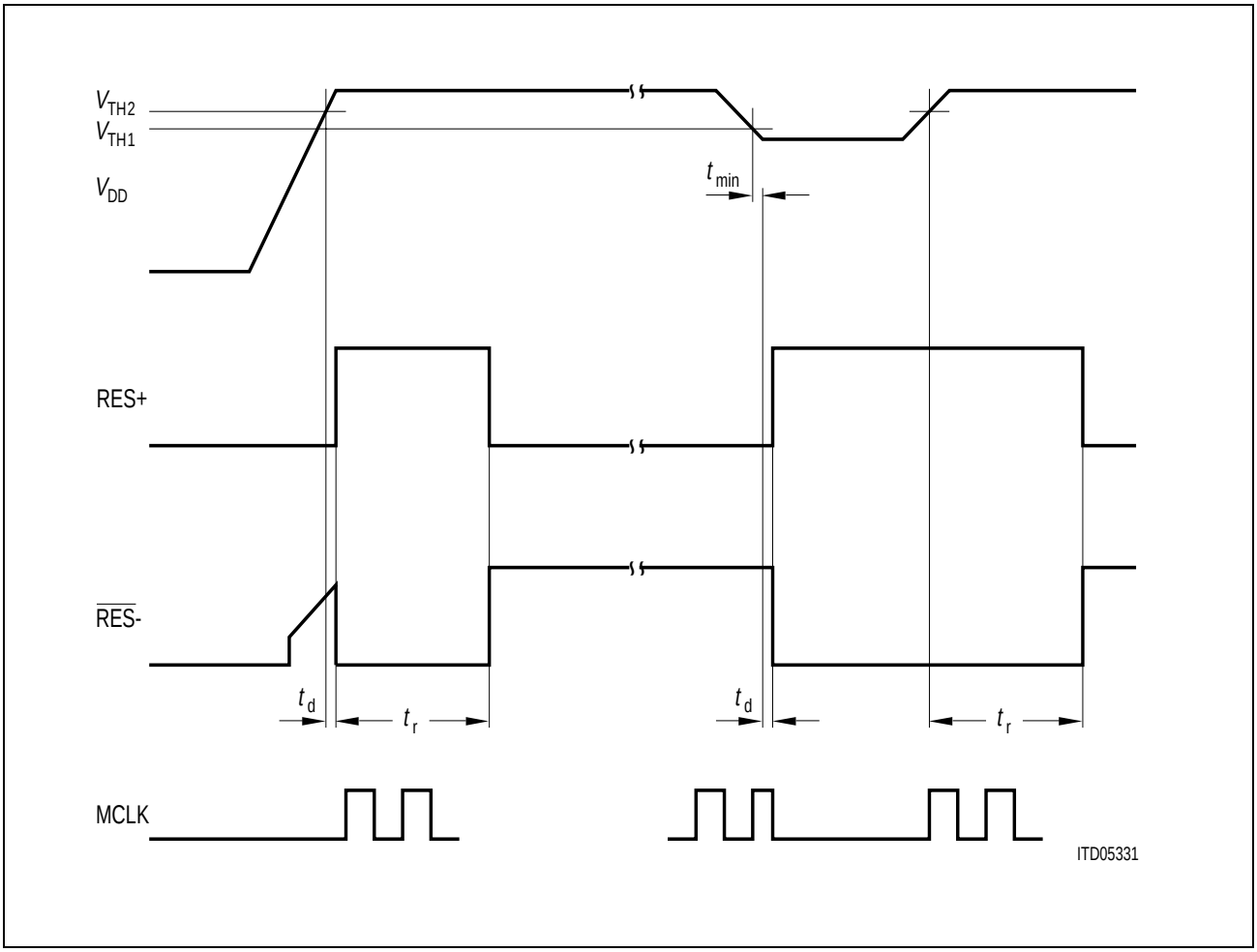


Figure 14
Undervoltage Control Timing

Watchdog Operation

The watchdog is enabled by setting the STCR:TSF to “1” and the CIX0:RSS bit to “1”. Switching RSS from “0” to “1” or “1” to “0” resets the watchdog timer.

After the microcontroller has enabled the watchdog timer it has to write the bit patterns “10” and “01” in the WTC1- and WTC2-bits (ADF1-register) within a period of 128 ms. If it fails to do so, a reset signal of 125 µs is generated.

C/I-Code Change

If the RSS-bit is set to “0”, a change in the downstream command/indicate channel (C/I0) generates a reset signal of 16 ms. This feature can be used to set the ISAC-P TE in power-down mode (layer-1 idle, IOM clocks off) and to allow a peripheral IOM-2 device to activate the ISAC-P TE. Activation is done by pulling the DU-line to V_{SS}.

Figure 15 shows as an example how the ISAC-P TE is interfaced to a Siemens/Intel 80C52 or Motorola MC68HC11 microcontroller.

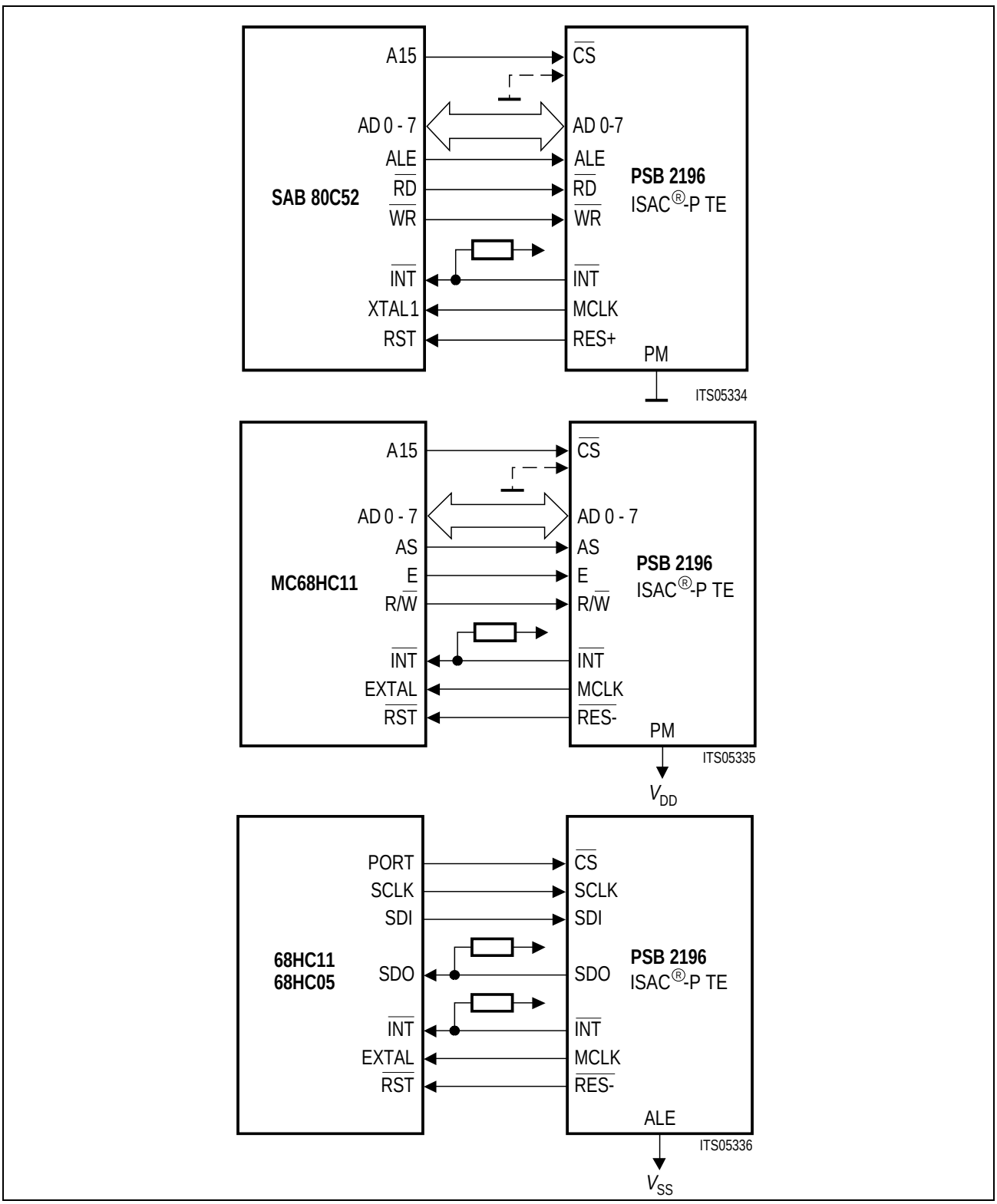


Figure 15
Interfacing the ISAC®-P TE to Siemens/Intel or Motorola Microcontroller

2.1.3.2 IOM®-2 Interface in TE-Mode

The ISAC-P TE supports the IOM-2 terminal mode. The interface consists of four lines: FSC, DCL, DD and DU. FSC transfers a frame start signal of which the rising edge indicates the start of an IOM-2 frame (8 kHz). The FSC-signal is generated by the receive DPLL which synchronizes it to the received U_{PN}-frame. The DCL-signal is the clock signal to synchronize the data transfer on both data lines (768 kbit/s). Its frequency is twice the transmission rate (1.536 MHz). The first rising edge indicates the start of a bit while the second falling edge is used to latch the contents of the data lines. Additionally the BCL and SDS1,2 signals are provided to connect standard codec's to the ISAC-P TE. The BCL (bit clock) provides a clock signal synchronous to the IOM-data at the same data rate. SDS1,2 provide strobe signals which are active high during the B1, B2, B1 + B2 or IC1, IC2, IC1 + IC2 channels.

The length of the FSC-signal on the IOM-2 interface is reduced to one DCL-period every eighth IOM-2 frame. A reduced FSC-signal is generated after a code violation has been received from the U_{PN}-interface.

If a peripheral IC connected to IOM-2 is not able to handle the short FSC pulse correctly, SDS1 or SDS2 may be used instead of FSC. They must be programmed to select B1 or B1+B2 time-slot.

IOM®-2 Driver Selection

The output driver of the IDP0/DD and IDP1/DU pins can be set to open drain (default for IOM-2) or to a push-pull output. The output drivers are active for the selected time-slot bits and remain tri-state during the rest of the frame.

IOM®-2 Frame Structure

The principle frame structure of the IOM-2 terminal mode is shown in **figure 16**. The frame is composed of three channels.

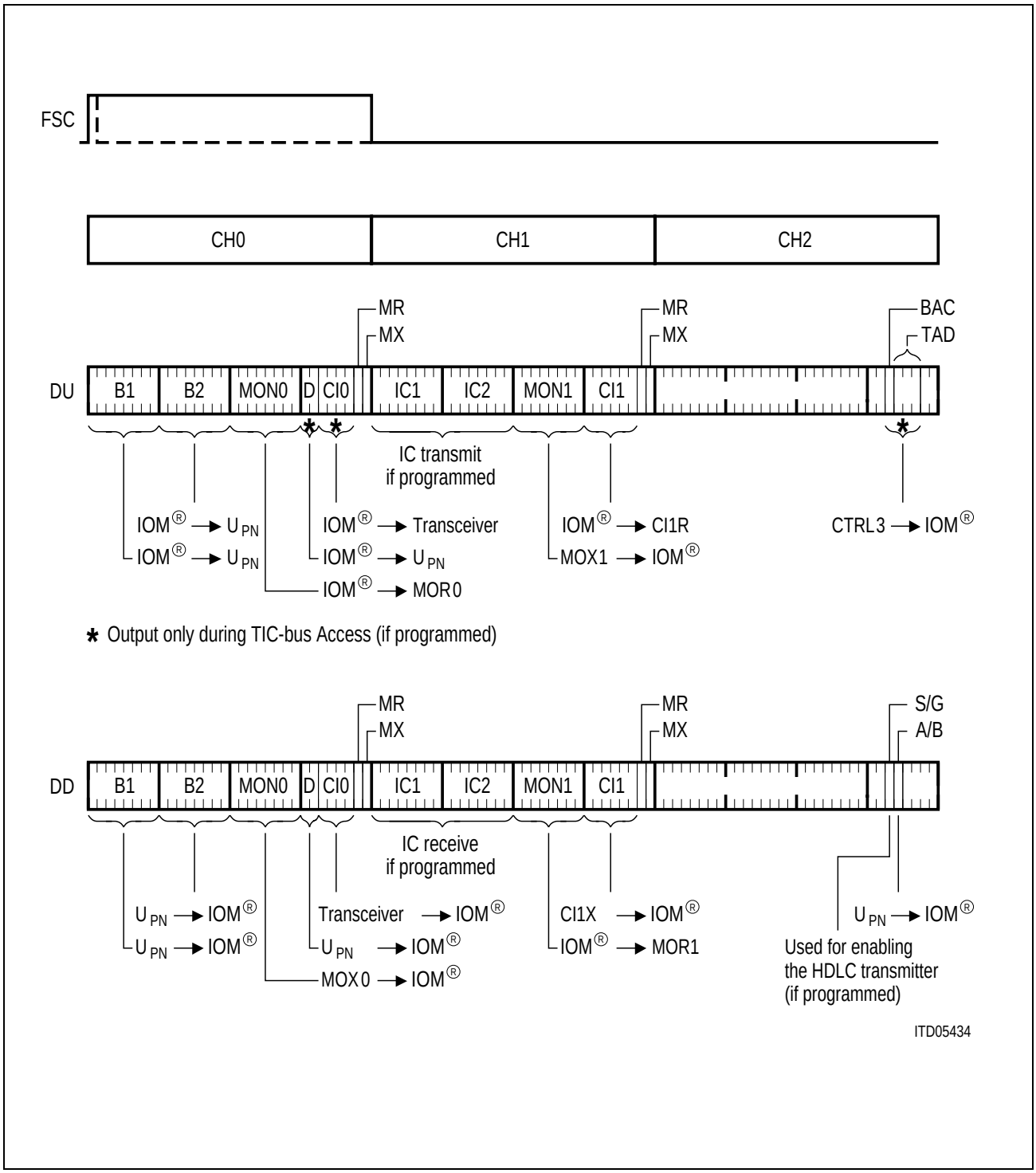


Figure 16
IOM®-Terminal Mode

- Channel 0 contains 144 kbit/s of user and signaling data (2B + D) plus a MONITOR and command/indicate channel for control and programming of the layer-1 transceiver.
- Channel 1 contains two 64-kbit/s intercommunication channels plus a MONITOR and command/indicate channel to program or transfer data to other IOM-2 devices.
- Channel 2 is used for the TIC-bus access. Only the command/indicate bits are specified in this channel.

IOM®-2 Time-Slots used by the ISAC®-P TE

The ISAC-P TE accesses a subset of all IOM-2 channels. It provides access to the D-channel, the C/I-channel 0 and to the TIC-bus. The information of the B1-, B2- and D-channel time-slots is forwarded transparently between the IOM-2 interface and the transceiver.

The ISAC-P TE provides also access to the MON0, MON1 monitor channels and handshake bits as well as to the C/I1-channel. The IC1-, IC2-channels may also be accessed.

Other time-slots are not influenced by the ISAC-P TE. They can be controlled by other devices connected to the IOM-2 interface.

The state of the BAC-bit is transmitted on the upstream T-channel to indicate a D-channel request to a TR-module which uses the ISAC-P TE.

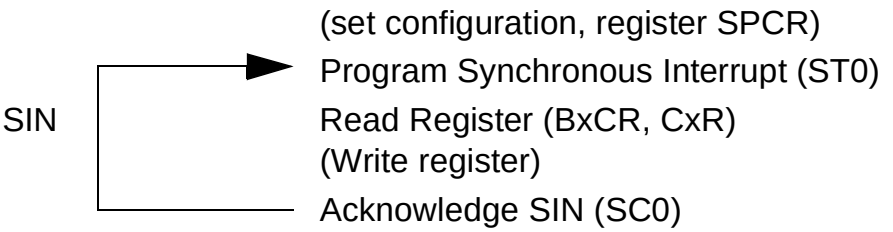
B/IC-Channel Access

The B1-, B2- and/or IC1-, IC2-channels are accessed by reading the B1CR/B2CR or by reading and writing the C1R/C2R-registers. The µP-access can be synchronized to the IOM-interface by means of a Synchronous Transfer programmed in the STCR-register.

The read/write access possibilities are shown in the table below.

CxC1	CxC0	CxR Read	CxR Write	BxCR Read	Output to IOM-2	Application(s)
0	0	ICx	–	Bx	–	Bx monitoring, ICx monitoring
0	1	ICx	ICx	Bx	ICx	Bx monitoring, ICx looping from/to IOM
1	0	–	Bx	Bx	Bx	Bx access from/to IOM; transmission of a constant value in Bx channel to IOM.
1	1	Bx	Bx	–	Bx	Bx looping from IOM; transmission of a variable pattern in Bx channel to IOM.

The general sequence of operations to access the B/IC-channels is:



Note: The data transfer itself works independent of the Synchronous Transfer Interrupt. In case of a SOV e.g. transfer is still possible.

IOM®-Channel 1 Access

The access to IOM-channel 1 may be reversed.

If IDC is set to “0” (Master Mode):

– DD carries the MONITOR 1 and C/I 1 channels as output to peripheral (voice/data) devices;

– DD carries the IC channels as output to other devices, if programmed (CxC1-0 = 01 in register SPCR).

If IDC is set to “1” (Slave mode):

– DU carries the MONITOR 1 and C/I 1 channels as output to a master device;

– DU carries the IC channels as output to other devices, if programmed (CxC1-0 = 01 in register SPCR).

C/I-Channel Handling

The Command/Indication channel carries real-time status information between the ICC and the U_{PN}-transceiver.

1) C/I0-channel conveys the commands and indications between a layer-1 device and a layer-2 device. It can be accessed from the microcontroller to control the layer-1 activation/deactivation procedures. Access is arbitrated via the TIC-bus access protocol (if programmed):

   This C/I-channel is access via register CIR0 (in receive direction layer 1-to-layer 2) and register CIX0 (in transmit direction, layer 2-to-layer 1). The code is four bits long.

   In the receive direction, the code from layer 1 is continuously monitored, with an interrupt being generated anytime a valid change occurs. A new code must be found in two consecutive IOM-frames to be considered valid and to trigger a C/I-code change interrupt status (double last look criterion).

   In the transmit direction, the code written in CIX0 is continuously transmitted in the channel.

2) A second C/I-channel (called C/I1) can be used to convey real time status information between the ISAC-P TE and various non-layer 1 peripheral devices. The channel consists of six bits in each direction.

The C/I1-channel is accessed via registers CIR1 and CIX1. A change in the received C/I1-code is indicated by an interrupt status without double last look criterion.

MONITOR Channel Access

In this case, the MONITOR channel protocol is a handshake protocol used for high speed information exchange between the ISAC-P TE and other devices, in MONITOR channel 0 or 1.

The MONITOR channel protocol is necessary (**see figure 17**):

- For programming and controlling devices attached to the IOM. Examples of such devices are: layer-1 transceivers (using MONITOR channel 0), and peripheral V/D-modules that do not have a parallel microcontroller interface (MONITOR channel 1), such as the Audio Ringing Codec Filter featuring speakerphone PSB 2165.
- For data exchange between two microcontroller systems attached to two different devices on one IOM-2 backplane. Use of the MONITOR channel avoids the necessity of a dedicated serial communication path between the two systems. This greatly simplifies the system design of terminal equipment (**figure 17**).

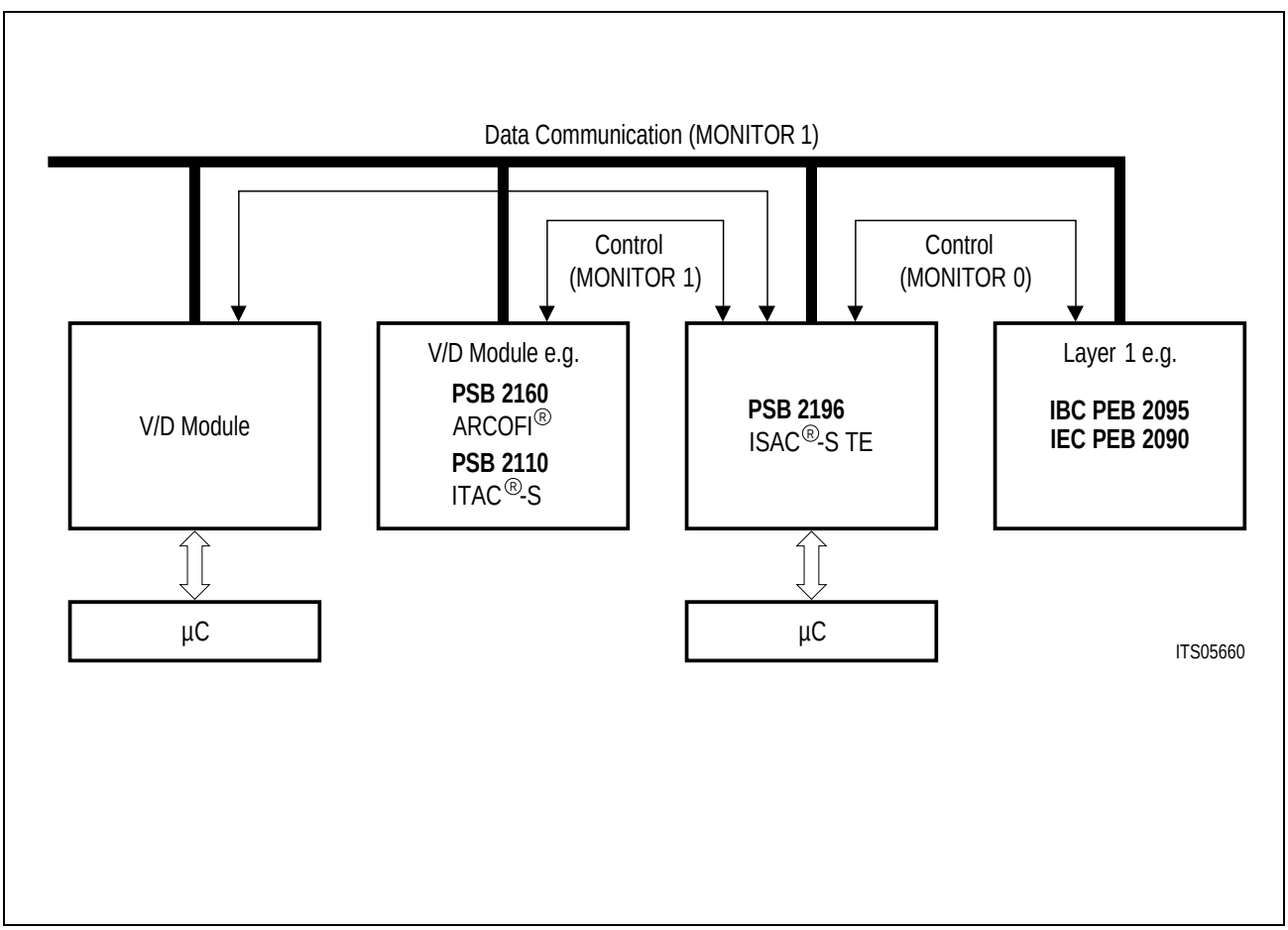


Figure 17
Examples of MONITOR Channel Applications

The MONITOR channel operates on an asynchronous basis. While data transfers on the bus take place synchronized to frame sync, the flow of data is controlled by a handshake procedure using the MONITOR Channel Receive (MR0 or 1) and MONITOR Channel Transmit (MX0 or 1) bits. For example: data is placed onto the MONITOR channel and the MX bit is activated. This data will be transmitted repeatedly once per 8-kHz frame until the transfer is acknowledged via the MR-bit.

The microprocessor may either enforce a “1” (idle) in MR, MX by setting the control bit MRC1,0 or MXC1,0 to “0” (MONITOR Control Register MOCR), or enable the control of these bits internally by the ICC according to the MONITOR channel protocol. Thus, before a data exchange can begin, the control bit MRC (1,0), or MXC (1,0) should be set to “1” by the microprocessor.

The MONITOR channel protocol is illustrated in **figure 18**. Since the protocol is identical in MONITOR channel 0 and MONITOR channel 1, the index 0 or 1 has been left out in the illustration.

The relevant status bits are:

- MONITOR Channel Data Received MDR (MDR0, MDR1)
- MONITOR Channel End of Reception MER (MER0, MER1)

for the **reception** of MONITOR data, and

- MONITOR Channel Data Acknowledged MDA (MDA0, MDA1)
- MONITOR Channel Data Abort MAB (MAB0, MAB1)

for the **transmission** of MONITOR data (Register: MOSR).

In addition, the status bit:

MONITOR Channel Active MAC (MAC0, MAC1)

indicates whether a transmission is in progress (Register: STAR).

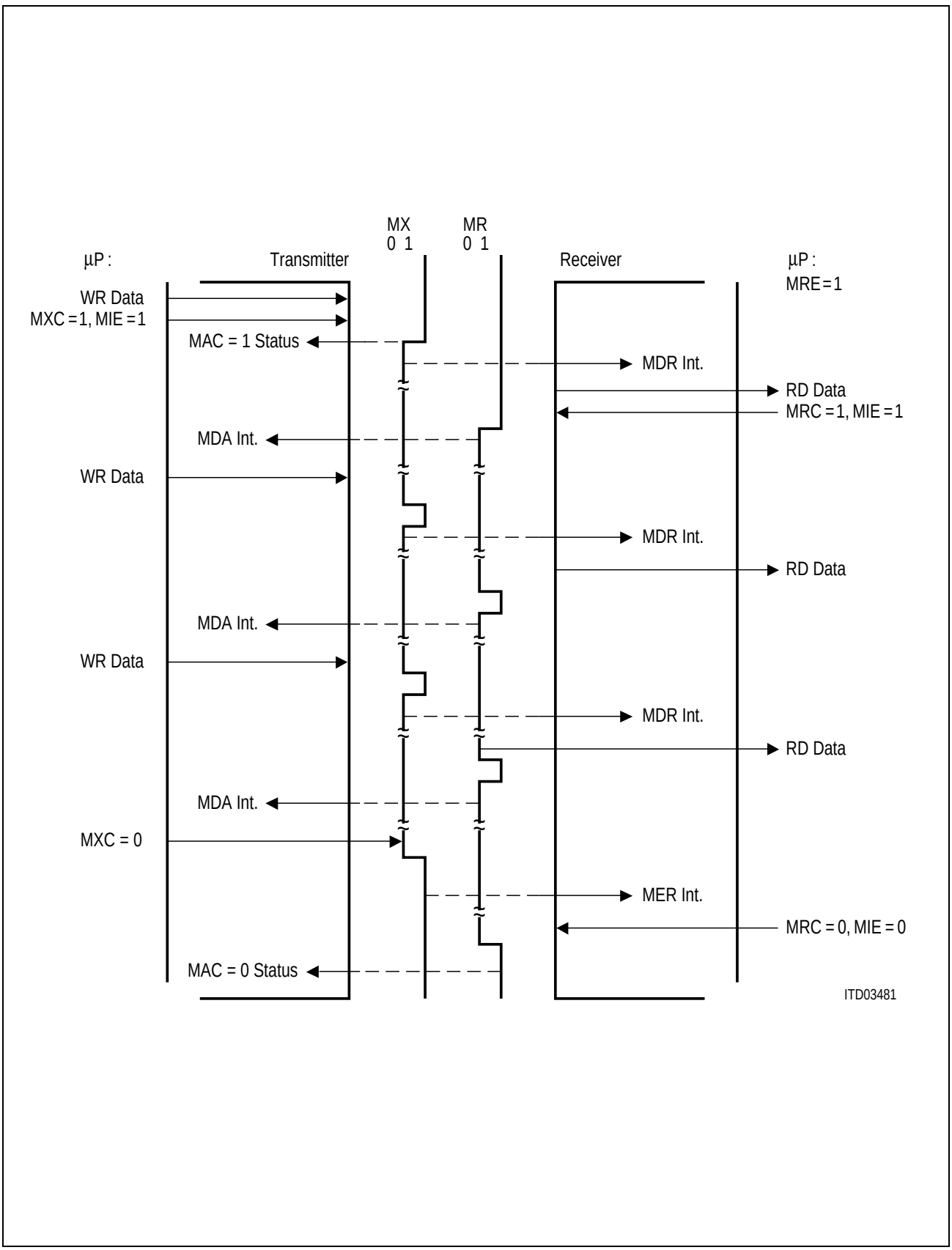

µP :
Transmitter
MX
0 1
MR
0 1
Receiver
µP :
MRE = 1
WR Data
MXC = 1, MIE = 1
MAC = 1 Status
MDR Int.
RD Data
MRC = 1, MIE = 1
MDA Int.
WR Data
MDR Int.
RD Data
MDA Int.
WR Data
MDR Int.
RD Data
MDA Int.
MXC = 0
MER Int.
MRC = 0, MIE = 0
MAC = 0 Status
ITD03481

Figure 18

Before starting a transmission, the microprocessor should verify that the transmitter is inactive, i.e. that a possible previous transmission has been terminated. This is indicated by an “0” in the MONITOR Channel Active MAC-status bit.

After having written the MONITOR Data Transmit (MOX) register, the microprocessor sets the MONITOR Transmit Control bit MXC to 1. This enables the MX-bit to go active (0), indicating the presence of valid MONITOR data (contents of MOX) in the corresponding frame.

As a result, the receiving device stores the MONITOR byte in its MONITOR Receive MOR register and generates a MDR-interrupt status.

Alerted by the MDR-interrupt, the microprocessor reads the MONITOR Receive (MOR) register. When it is ready to accept data (e.g. based on the value in MOR, which in a point-to-multipoint application might be the address of the destination device), it sets the MR-control bit MRC to “1” to enable the receiver to store succeeding MONITOR channel bytes and acknowledge them according to the MONITOR channel protocol. In addition, it enables other MONITOR channel interrupts by setting MONITOR Interrupt Enable to “1”.

As a result, the first MONITOR byte is acknowledged by the receiving device setting the MR bit to “0”. This causes a MONITOR Data Acknowledge MDA-interrupt status at the transmitter.

A new MONITOR data byte can now be written by the microprocessor in MOX. The MX-bit is still in the active (0) state. The transmitter indicates a new byte in the MONITOR channel by returning the MX-bit active after sending it once in the inactive state. As a result, the receiver stores the MONITOR byte in MOR and generates anew a MDR-interrupt status. When the microprocessor has read the MOR-register, the receiver acknowledges the data by returning the MR-bit active after sending it once in the inactive state. This in turn causes the transmitter to generate a MDA-interrupt status.

This “MDA-interrupt — write data — MDR-interrupt — read data — MDA-interrupt” handshake is repeated as long as the transmitter has data to send. Note that the MONITOR channel protocol imposes no maximum reaction times to the microprocessor.

When the last byte has been acknowledged by the receiver (MDA-interrupt status), the microprocessor sets the MONITOR Transmit Control bit MXC to 0. This enforces an inactive (“1”) state in the MX-bit. Two frames of MX inactive signifies the end of a message. Thus, a MONITOR Channel End of Reception MER-interrupt status is generated by the receiver when the MX is received in the inactive state in two consecutive frames. As a result, the microprocessor sets the MR control bit MRC to 0, which in turn enforces an inactive state in the MR-bit. This marks the end of the transmission, making the MONITOR Channel Active MAC-bit return to “0”.

During a transmission process, it is possible for the receiver to ask a transmission to be aborted by sending an inactive MR-bit value in two consecutive frames. This is effected by the microprocessor writing the MR-control bit MRC to 0. An aborted transmission is indicated by a MONITOR Channel Data Abort MAB-interrupt status at the transmitter.

Available / Busy Bit

The A/B-bit is a new bit on the TIC-bus. It is used to transfer the state of the line-card HDLC-controller indicated by the U_{PN} T-channel to the PEB 2081 SBCX used on a S/T-interface option.

If the A/B-bit is “1”, it indicates that the line-card HDLC-controller is available and D-channel messages may be transmitted. If it changes to “0”, the HDLC-controller has to abort the transmission and has to restart the transmission after the A/B-bit becomes “1” again.

The A/B-bit is used by the SBCX (PSB 20810) on a S/T-interface option to control the ECHO channel of the S/T-interface and the Stop/Go bit on the IOM-2 interface.

The selection between mapping the U_{PN} T-channel onto the S/G- or A/B-bit is performed by the GCR:TCM bit.

2.1.3.3 U_{PN}-Interface

Figure 19 demonstrates the general principles of the U_{PN}-interface communication scheme. A frame transmitted by the exchange (LC) is received by the terminal equipment (TE) after a line propagation delay. The terminal equipment waits the minimum guard time (5.2 µs) while the line clears. It then transmits a frame to the exchange. The exchange will begin a transmission every 250 µs (known as the burst repetition period). However, the time between the reception of a frame from the TE and the beginning of transmission of the next frame by the LC must be greater than the minimum guard time.

Within a burst, the data rate is 384 kbit/s and the 38-bit frame structure is as shown in **figure 19**.The framing bit (LF) is always logical “1”. The frame also contains the user channels (2B + D). Note that the B-channels are scrambled. It can readily be seen that in the 250 µs burst repetition period, 4 D-bits, 16 B1-bits and 16 B2-bits are transferred in each direction. This gives an effective full duplex data rate of 16 kbit/s for the D-channel and 64 kbit/s for each B-channel.

The final bit of the frame is called the M-bit.

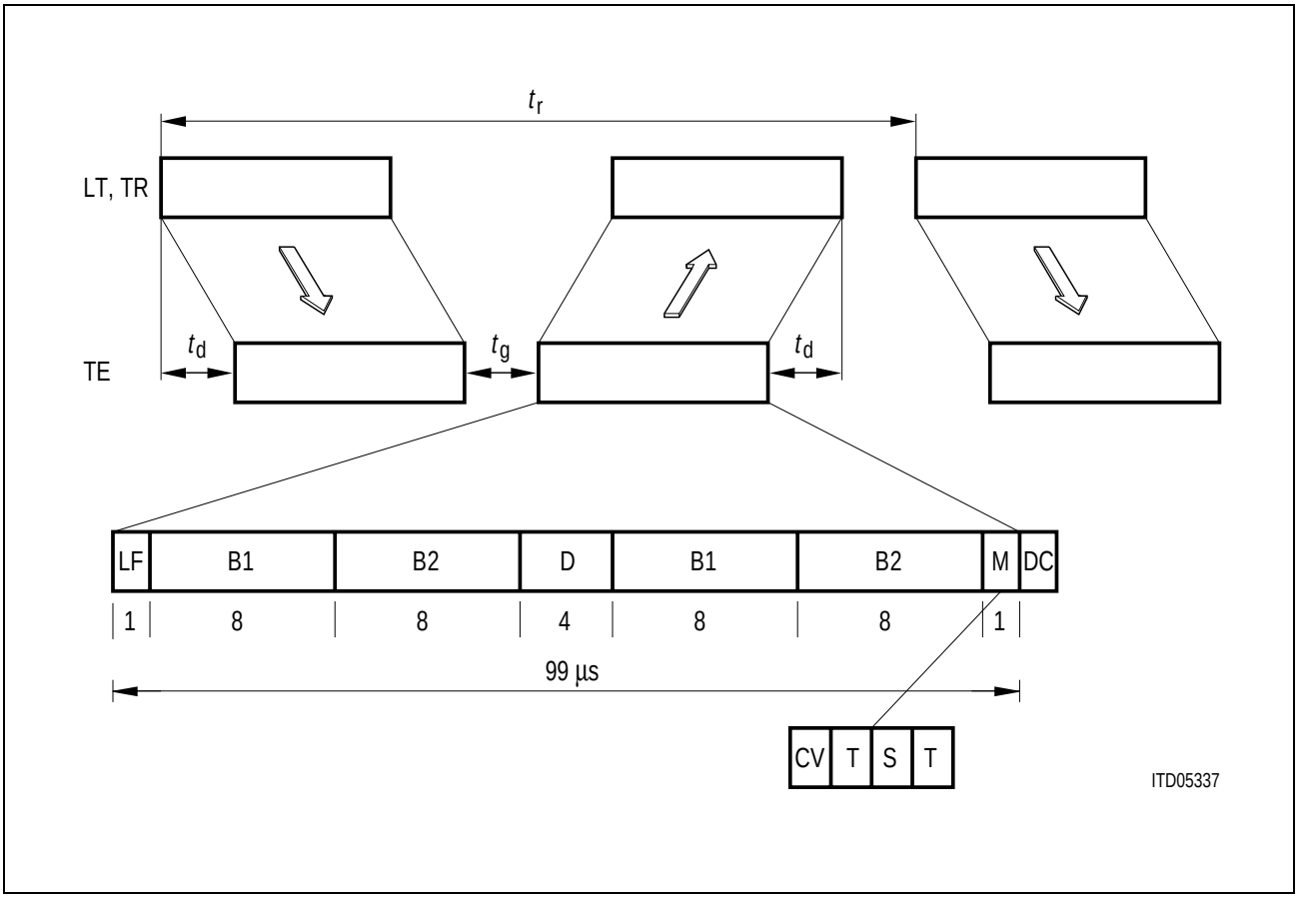
Four successive M-bits, from four successive U_{PN}-frames, constitute a superframe (**figure 19**). Three signals are carried in this superframe. The superframe is started by a code violation (CV). From this reference, bit 3 of the superframe is the service channel bit (S). The S-channel bit is transmitted once in each direction in every fourth burst repetition period. Hence the duplex S-channel has a data rate of 1 kbit/s. It conveys test loop control information from the LC to the TE and reports of transmission errors from the TE to the LC. Bit 2 and bit 4 of the superframe are the T-bits. Not allocated to a specific function until now (cf PEB 2095 IBC and PEB 20950 ISAC-P) they can be used for D-channel control in conjunction with PEB 20550 ELIC and PEB 2096 Octat-P.

In order to decrease DC-offset voltage on the line after transmission of a CV in the M-bit position, it is allowed to add a DC-balancing bit to the burst. The LC-side transmits this DC-balancing bit, when transmitting INFO 4 and when line characteristics indicate potential decrease in performance.

Note that the guard time in TE is always defined with respect to the M-bit, whereas AMI coding includes always all bits going in the same direction.

The coding technique used on the U-interface is half-bauded AMI-code (i.e. with a 50% pulse width). A logical “0” corresponds to a neutral level, a logical “1” is coded as alternate positive and negative pulses.

In the terminal repeater mode no DC-balancing bit will be generated. The loop length of the TR-mode is limited to 100 m.



t_r = burst repetition period = 250 µs
t_d = line delay = 20.8 µs max.
t_g = guard time = 5.2 µs max.

DC balancing bit, only sent after a code violation in the M-bit position and in special configurations.

M Channel Superframe

CV = Code Violation: for superframe synchronization
T = Transparent Channel (2 kbit/s)
S = Service Channel (1 kbit/s)

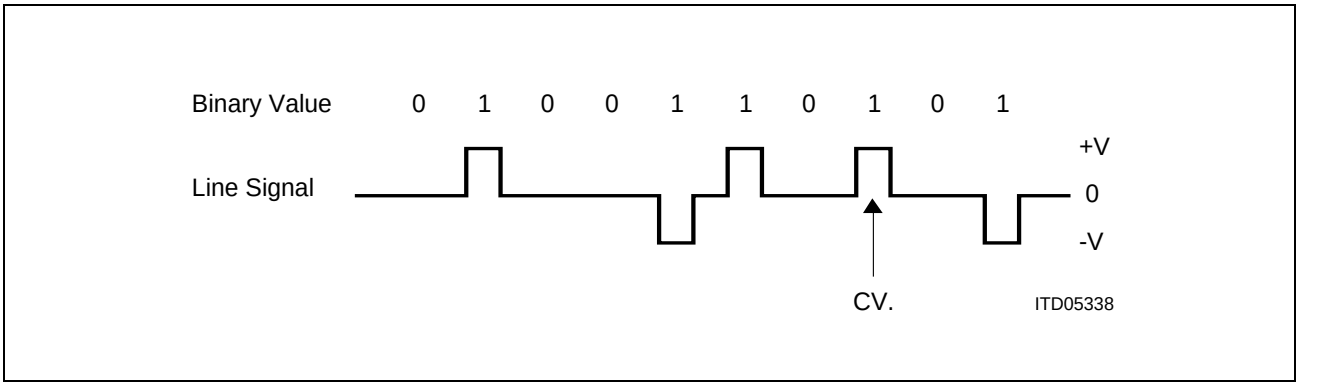


Figure 19
U_{PN}-Interface Structure

Scrambler/Descrambler

B-channel data on the U_{PN}-interface is scrambled to give a flat continuous power density spectrum and to ensure enough pulses are present on the line for a reliable clock extraction to be performed at the downstream end.

The ISAC-P TE therefore contains a scrambler and descrambler, in the transmit and receive directions respectively. The basic form of these are illustrated in **figure 20**. The form is in accordance with the CCITT V.27 scrambler/descrambler and contains supervisory circuitry which ensures no periodic patterns appear on the line.

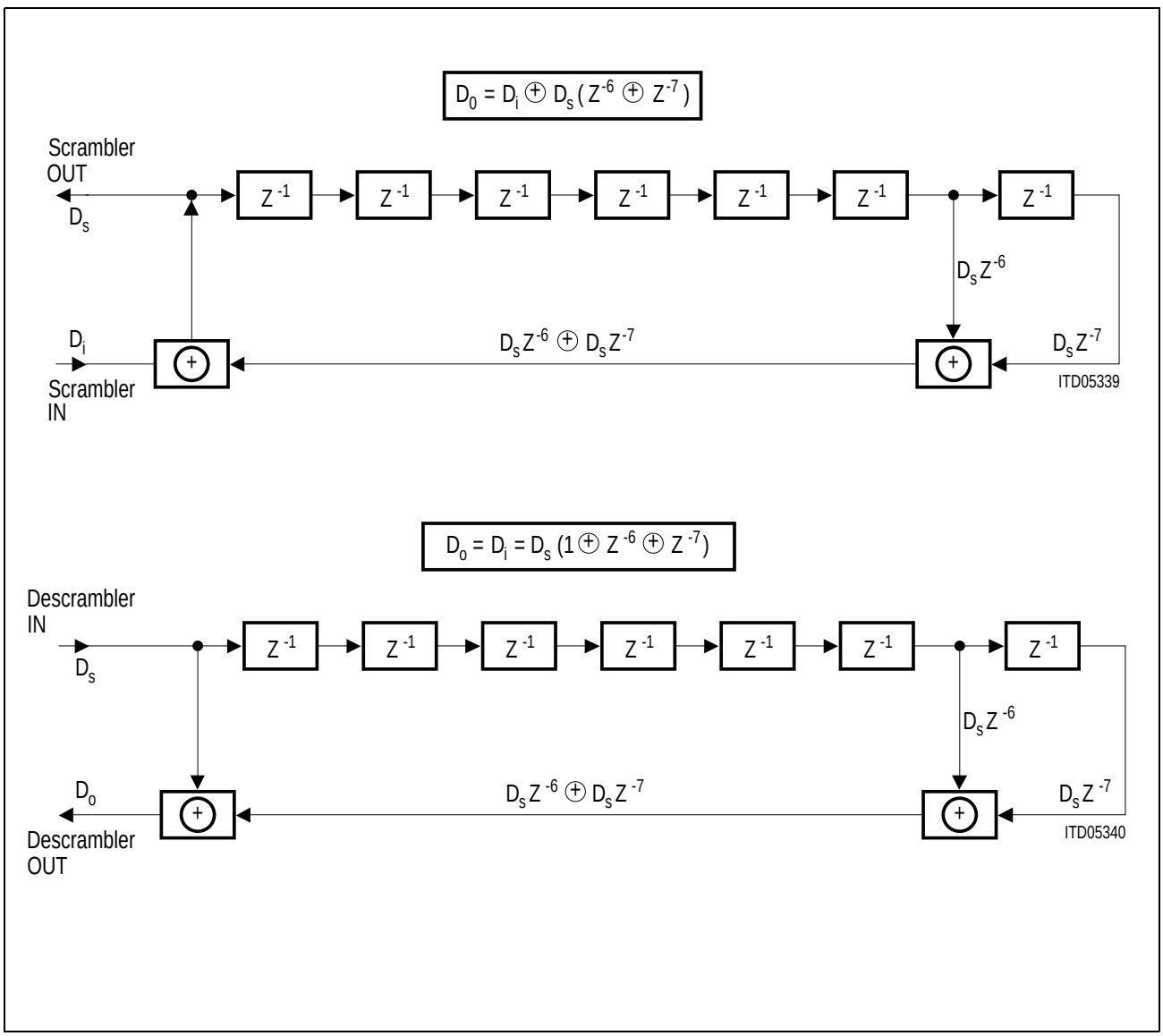


Figure 20
Scrambler/Descrambler

Info Structure on the U_{PN}-Interface

The signals controlling the internal state machine on the U_{PN}-interface are called infos. In effect these pass information regarding the status of the sending U_{PN}-transceiver to the other end of the line. They are based upon the same format as the U_{PN}-interface frames and their precise form is shown in **table 2**.

When the line is deactivated info 0 is exchanged by the U_{PN}-transceivers at either end of the line. Info 0 effectively means there is no signal sent on the line in either direction.

When the line is activated info 3 upstream and info 4 downstream are continually exchanged. Both info 3 and info 4 are effectively normal U_{PN}-Interface data frames containing user data and exchanged in normal burst mode.

Note that the structure of info 1 and info 2 are the same, they only differ in the direction of transmission. Similarly info 3 / info 4 and info 1w / info 2w also constitute info pairs. This will be important when considering looped states.

As we will see, the other infos are exchanged during various states which occur between activation and deactivation of the line.

Table 2
U_{PN}-Interface Info Signals

Name	Direction	Description
Info 0	Upstream Downstream	No signal on the line
Info 1w	Upstream	Asynchronous wake signal 2-kHz burst rate F000100010001000100010101010001011111 1 Code violation in the framing bit
Info 1	Upstream	4-kHz burst signal F000100010001000100010101010001011111M[1)]DC[2)] Code violation in the framing bit
Info 2	Downstream	4-kHz burst signal F000100010001000100010101010001011111M[1)]DC[2)] Code violation in the framing bit
Info 3	Upstream	4-kHz burst signal No code violation in the framing bit User data in B-, D- and M-channels B-channels scrambled, DC-bit [2)] optional
Info 4	Downstream	4-kHz burst signal No code violation in the framing bit User data in B-, D- and M-channels B-channels scrambled, DC-bit [2)] optional

Notes:

1) The M-channel superframe is transparent:
   S-bits transparent (1-kbit/s channel)
   T-bits transparent (2-kbit/s channel)

2) DC-balancing bit

U_{PN}-Transceiver

Figure 21 depicts the transceiver architecture and the analog connections of the ISAC-P TE. External to the line interface pins Lla and Llb a transformer and external resistors are connected as shown. Note that the internal resistors of the transformer are calculated as zero. The actual values of the external resistors must take into account the real resistor of the chosen transformer.

The receiver section consists of an amplifier followed by a peak detector controlling the thresholds of the comparators. In conjunction with a digital oversampling technique the PSB 2196 ISAC-P TE covers the electrical requirements of the U_{PN}-interface for loop lengths of at least 4.5 kft on AWG 22 (to be verified) cable and 1.0 km on J-Y(ST) Y $2 \times 2 \times 0.6$ cable.

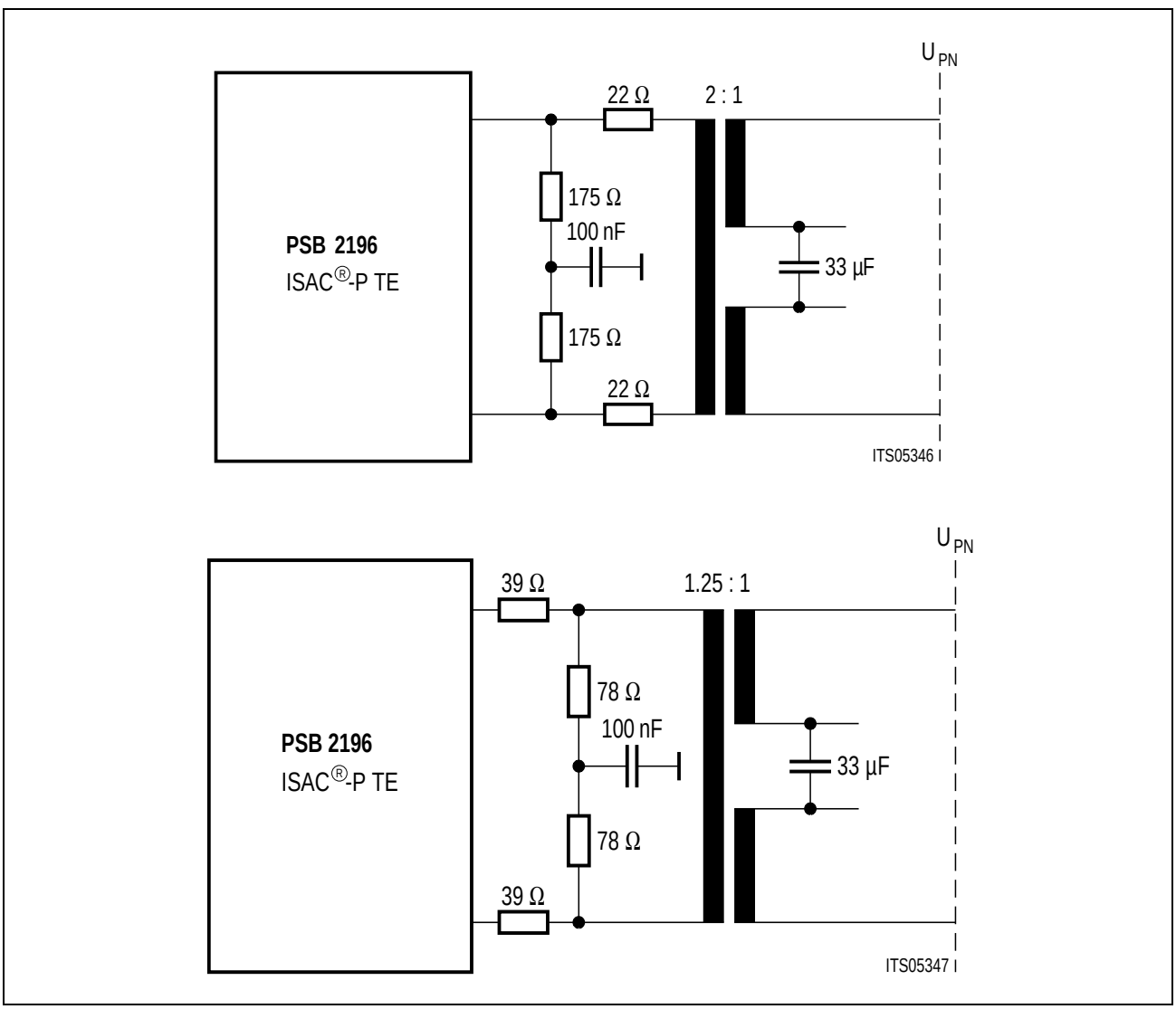


Figure 21
U_{PN}-Transceiver of the ISAC®-P TE

U_{PN}-Transceiver Timing

The receive PLL uses the 15.36-MHz clock to generate an internal 384-kHz signal which is used to synchronize the PLL to the received U_{PN}-frame. The PLL-outputs the FSC-signal as well as the 1.536-MHz double bit clock signal and the 768-kHz bit clock.

The length of the FSC-signal is reduced in the next IOM-2 frame which is started while a U_{PN}-frame is received, after a code violation has been detected. The reduced length of the FSC-signal provides synchronization between the TE- and the TR-transceiver to gain the shortest delays on the U_{PN} T-channel data forwarding.

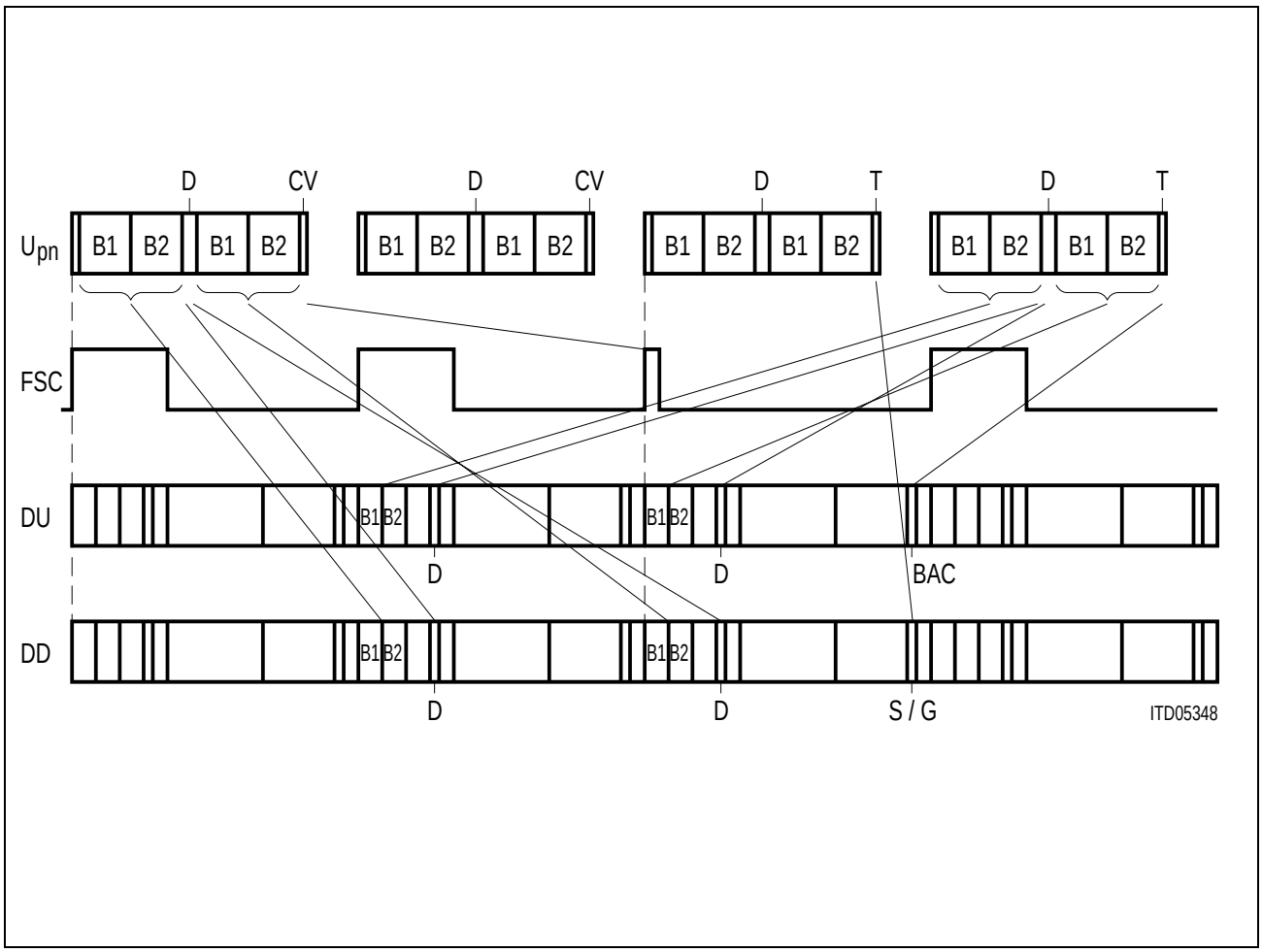


Figure 22
U_{PN}-Transceiver Timing in TE-Mode

Control of the U_{PN}-Transceiver

An incorporated finite state machine controls the activation / deactivation procedures and communications with the layer-2 section via the lOM-Command / Indicate (C/I) channel 0.

Diagnostics Functions

Two test loops allow the local or the remote test of the transceiver function.

Test loop 3 is a local loop which loops the transmit data of the transmitter to its receiver. The information of the IOM-2 upstream B- and D-channels is looped back to the downstream B- and D-channels. The M-bit is also transparent which means that the state of the BAC-bit is looped back to the S/G- or A/B-bit.

Test loop 2 is activated by the U_{PN}-interface and loops the received data back to the U_{PN}-interface. The D-channel information received from the line-card is transparently forwarded to the downstream IOM-2 D-channel. The B-channel information received from the line-card may not be forwarded to the IOM-2 interface. Instead, “1” is output on DD during time-slots B1 and B2 if programmed.

2.1.4 D-Channel Arbitration in TE-Mode

The ISAC-P TE supports different kinds of D-channel arbitration in order to share the upstream D-channel by several communication controllers and to allocate the D-channel from the U_{PN}-interface.

The following functions are performed:

– Allocation of the upstream D-channel bits on the IOM-2 interface via the TIC-bus.
– Control of the HDLC-transmitter by the stop/go bit.

TIC-Bus Access

The terminal IC bus provides an access mechanism to share the D-channel in upstream direction by several communication controllers (ICC, ISAC, ISAC) connected to one layer-1 device. The Bus Accessed bit (BAC) is used to indicate that the TIC-bus is currently occupied and other devices have to wait. The different communication controllers use individual TIC-bus addresses in the range of “0” to “7”. A collision detection mechanism checks each bit of the TIC-bus address for congestion. Since a “0” has higher priority against a “1”, a TIC-bus address of “0” has the highest priority and “7” has the lowest one.

TIC-Bus Access Mechanism

During idle state, the Bus Accessed bit (BAC) is set to “1” and the TIC-Bus Address (TBA) is “7”.

If a communication controller needs access to the D-channel bits, it will check the state of the BAC-bit. If BAC is “1” (idle) it will place its TIC-bus address on the TAD2-0 bits. After each bit has been outputted, it checks for collision and stops transmitting if a collision is detected (“1” transmitted, “0” detected on the DU-line). If the TIC-bus address has been transmitted successfully, the D-channel and C/I0-channel are controlled from

the controller in the next frame and the BAC-bit is set to “0”. After the TIC-bus access is completed, the TIC-bus returns to the idle state (BAC = “1”, TAD = “111”) and other devices can gain access.

A device which has detected a collision during the transmission of the TIC-bus address will restart after the BAC-bit becomes idle “1” again. In order to provide access to all controllers, the device which has gained successful access to the TIC-bus will wait for two idle frames before it starts another access.

Stop/Go Bit

The Stop/Go bit controls the transmitter output of the D-channel HDLC-controller if selected by the SGE-bit. The transmitter is active, as long as the Stop/Go bit indicates Go (“0”).

The S/G-bit is checked before a HDLC-frame is started and monitored during the whole HDLC-frame.

The Stop/Go bit can be controlled by the downstream T-bit which indicates the receive capability of the line card or by the SBCX in case a So-adapter is plugged onto the IOM-2 interface.

HDLC-Controller Access Modes

The access mode of the D-channel HDLC-controller is programmable.

If the HDLC-controller is set to a mode where the S/G-bit is evaluated, the transmission is started if the D-channel idle condition is detected and stopped if the D-channel is not available anymore.

If the D-channel becomes not available before the final bit of the closing flag has been sent, the transmission is aborted. It is automatically restarted if the D-channel becomes not available during the transmission of the contents of the first FIFO-data. Otherwise, an interrupt is generated and the microcontroller has to repeat the complete frame again.

2.1.5 Layer-2 Functions for HDLC

The HDLC-controller in the ISAC-P TE is responsible for the data link layer using HDLC/ SDLC based protocols.

The ISAC-P TE can be made to support the data link layer to a degree that best suits system requirements. When programmed in auto mode, it handles elements of procedure of an acknowledged, balanced class of HDLC-protocol autonomously (window size equal to “1”). Multiple links may be handled simultaneously due to the address recognition capabilities, as explained in **section 2.1.5.1**.

The ISAC-P TE supports point-to-point protocols such as LAPB (Link Access Procedure Balanced) used in X.25 networking.

For ISDN, one particularly important protocol is the **Link Access Procedure for the D-channel** (LAPD).

LAPD, layer 2 of the ISDN D-channel protocol (CCITT I.441) includes functions for:

– Provision of one or more data link connections on a D-channel (multiple LAP). Discrimination between the data link connections is performed by means of a data link connection identifier (DLCI = SAPI + TEI)
– HDLC-framing
– Application of a balanced class of procedure in point-multipoint configuration.

The simplified block diagram in **figure 3**, shows the functional blocks of the ISAC-P TE which support the LAPD-protocol.

The HDLC-transceiver in the ISAC-P TE performs the framing functions used in HDLC/ SDLC based communication: flag generation/recognition, bit stuffing, CRC-check and address recognition.

The FIFO-structure with two 64-byte pools for transmit and receive directions and an intelligent FIFO-controller permit flexible transfer of protocol data units to and from the µC-system.

2.1.5.1 Message Transfer Modes

The HDLC-controller can be programmed to operate in various modes, which are different in the treatment of the HDLC-frame in receive direction. Thus, the receive data flow and the address recognition features can be programmed in a flexible way, to satisfy different system requirements.

In the auto-mode the ISAC-P TE handles elements of procedure of the LAPD (S- and I-frames) according to CCITT I.441 fully autonomously.

For the address recognition the ISAC-P TE contains four programmable registers for individual SAPI- and TEI-values SAP1-2 and TEI1-2, plus two fixed values for “group” SAPI and TEI, SAPG and TEIG.

There are 5 different operating modes which can be set via the MODE register:

Auto-mode (MDS2, MDS1 = 00)

Characteristics:

– Full address recognition (1 or 2 bytes).
– Normal (mod 8) or extended (mod 128) control field format.
– Automatic processing of numbered frames of an HDLC-procedure (**see 2.1.5.2**).

If a 2-byte address field is selected, the high address byte is compared with the fixed value FE_H or FC_H (group address) as well as with two individually programmable values in SAP1- and SAP2-registers. According to the ISDN LAPD-protocol, bit 1 of the high byte address will be interpreted as COMMAND/RESPONSE bit (C/R) dependent on the setting of the CRI-bit in SAP1, and will be excluded from the address comparison.

Similarly, the low address byte is compared with the fixed value FF_H (group TEI) and two compare values programmed in special registers (TEI1, TEI2). A valid address will be recognized in case the high and low byte of the address field match one of the compare values. The ISAC-P TE can be called (addressed) with the following address combinations:

– SAP1/TEI1
– SAPl/FF_H
– SAP2/TEI2
– SAP2/FF_H
– FE_H(FC_H)/TEI1
– FE_H(FC_H)/TEI2
– FE_H(FC_H)/FF_H

Only the logical connection identified through the address combination SAP1, TEI1 will be processed in the auto mode, all others are handled as in the non-auto mode. The logical connection handled in the auto mode must have a window size 1 between transmitted and acknowledged frames. HDLC-frames with address fields that do not match with any of the address combinations, are ignored by the ISAC-P TE.

In case of a 1-byte address, TEI1 and TEI2 will be used as compare registers. According to the X.25 LAPB-protocol, the value in TEI1 will be interpreted as COMMAND and the value in TEI2 as RESPONSE.

The control field is stored in RHCR-register and the l-field in RFIFO. Additional information is available in RSTA.

Non-Auto Mode (MDS2, MDS1 = 01)

Characteristics: Full address recognition (1 or 2 bytes)
Arbitrary window sizes

All frames with valid addresses (address recognition identical to auto mode) are accepted and the bytes following the address are transferred to the µP via RHCR and RFIFO. Additional information is available in RSTA.

Transparent Mode 1 (MDS2, MDS1, MDS0 = 101).

Characteristics: TEI-recognition

A comparison is performed only on the second byte after the opening flag, with TEI1, TEI2 and group TEI (FF_H). In case of a match, the first address byte is stored in SAPR, the (first byte of the) control field RHCR, and the rest of the frame in the RFIFO. Additional information is available in RSTA.

Transparent Mode 2 (MDS2, MDS1, MDS0 = 110).

Characteristics: non address recognition.

Every received frame is stored in RFIFO (first byte after opening flag to CRC-field). Additional information can be read from RSTA.

Transparent Mode 3 (MDS2, MDS1, MDS0 = 111)

Characteristics: SAPI-recognition.

A comparison is performed on the first byte after the opening flag with SAP1, SAP2 and group SAPI (FE/FC_H). In the case of a match, all the following bytes are stored in RFIFO. Additional information can be read from RSTA.

2.1.5.2 Protocol Operations (auto-mode)

In addition to address recognition all S- and I-frames are processed in hardware in the auto-mode. The following functions are performed:

- update of transmit and receive counter
- evaluation of transmit and receive counter
- processing of S-commands
- flow control with RR/RNR
- response generation
- recognition of protocol errors
- transmission of S-commands, if an acknowledgement is not received
- continuous status query of remote station after RNR has been received
- programmable timer/repeater functions.

The processing of frames in auto-mode is described in detail in section **2.1.6**.

2.1.5.3 Reception of Frames

A 2×32-byte FIFO-buffer (receive pools) is provided in the receive direction.

The control of the data transfer between the CPU and the ISAC-P TE is handled via interrupts.

There are two different interrupt indications concerned with the reception of data:

– RPF (**R**eceive **P**ool **F**ull) interrupt, indicating that a 32-byte block of data can be read from the RFIFO and the received message is not yet complete.
– RME (**R**eceive **M**essage **E**nd) interrupt, indicating that the reception of one message is completed, i.e. either

- one message ≤ 32 bytes, or
- the last part of a message ≥ 32 bytes

is stored in the RFIFO.

Depending on the message transfer mode the address and control fields of received frames are processed and stored in the receive FIFO or in special registers as depicted in **figure 23**.

The organization of the RFIFO is such that, in the case of short (≤ 32 bytes), successive messages, up to two messages with all additional information can be stored. The contents of the RFIFO would be, for example, as shown in **figure 24**.

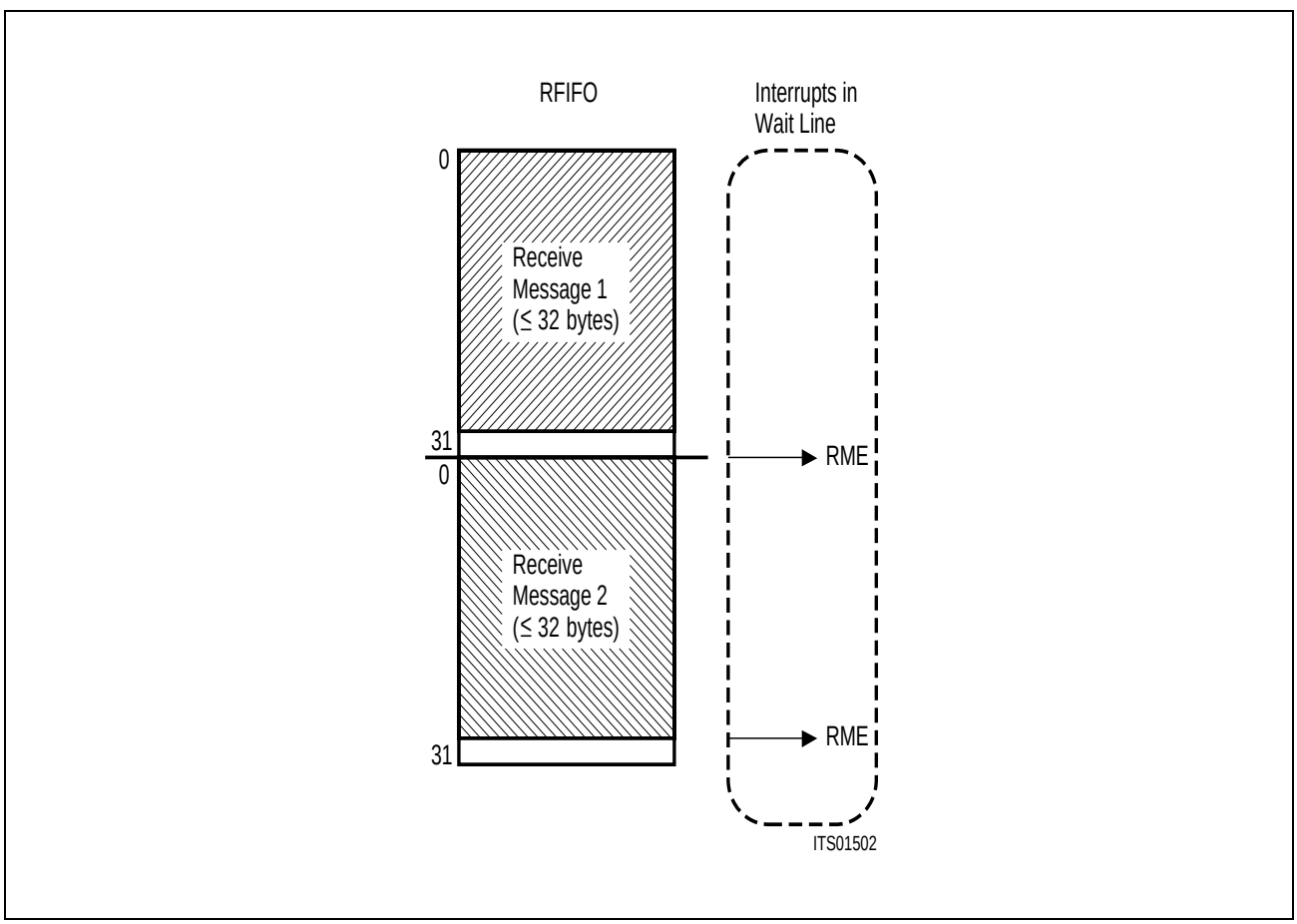


Figure 23
Contents of RFIFO (short message)

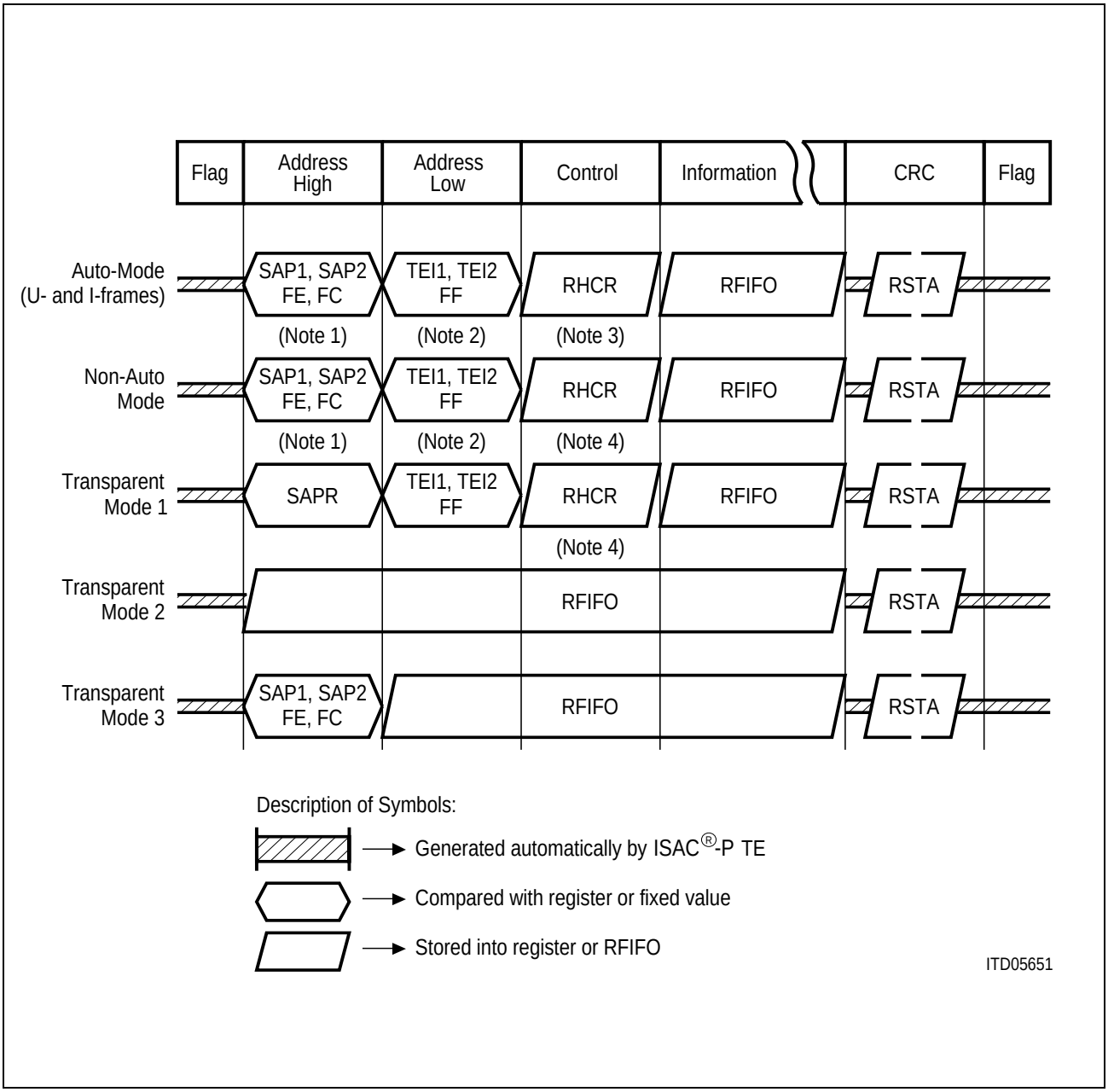


Figure 24
Receive Data Flow

Note 1 Only if a 2-byte address field is defined (MDS0 = 1 in MODE register).

Note 2 Comparison with Group TEI (FF_H) is only made if a 2-byte address field is defined (MDS0 = 1 in MODE register).

Note 3 In the case of an extended, modulo 128 control field format (MCS = 1 in SAP2-register) the control field is stored in RHCR in compressed form (I-frames).

Note 4 In the case of extended control field, only the first byte is stored in RHCR, the second in RFIFO.

When 32 bytes of a message longer than that are stored in RFIFO, the CPU is prompted to read out the data by an RPF interrupt. The CPU must handle this interrupt before more than 32 additional bytes are received, which would cause a “data overflow” (**figure 25**). This corresponds to a maximum CPU-reaction time of 16 ms (data rate 16 kbit/s).

After a remaining block of less than or equal to 16 bytes has been stored, it is possible to store the first 16 bytes of a new message (**see figure 25**).

The internal memory is now full. The arrival of additional bytes will result in “data overflow” and a third new message in “frame overflow”.

The generated interrupts are inserted together with all additional information into a wait line to be individually passed to the CPU.

After an RPF- or RME-interrupt has been processed, i.e. the received data has been read from the RFIFO, this must be explicitly acknowledged by the CPU issuing a RMC (Receive Message Complete) command.

The ISAC-P TE can then release the associated FIFO-pool for new data. If there is an additional interrupt in the wait line it will be generated after the RMC-acknowledgment.

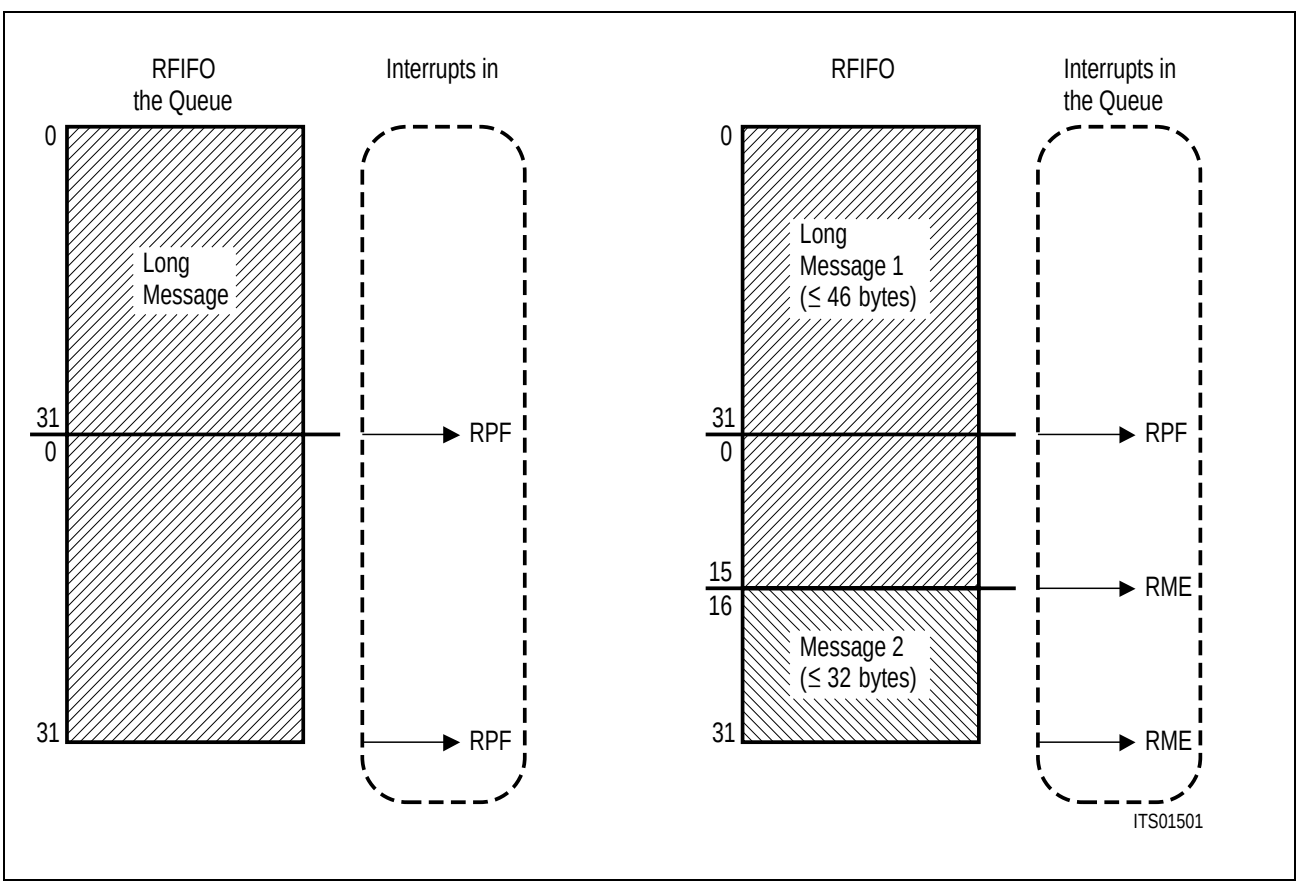


Figure 25
Contents of RFIFO (long message)

Information about the received frame is available for the µP when the RME-interrupt is generated, as shown in **table 3**.

Table 3
Receive Information at RME-Interrupt

Information	Register	Bit	Mode
First byte after flag (SAPI of LAPD-address field)	SAPR	–	Transparent mode 1
Control field	RHCR	–	Auto-mode, I-(modulo 8) and U-frames
Compressed control field	RHCR	–	Auto-mode, I-frames (modulo 128)
2nd byte after	RHCR	–	Non-auto mode, 1 byte address field
3rd byte after	RHCR	–	Non-auto mode, 2-byte address field Transparent mode 1
Type of frame (Command/ Response)	STAR	C/R	Auto-mode, 2-byte address field Non-auto mode, 2-byte address field Transparent mode 3
Recognition of SAPI	STAR	SA1-0	Auto-mode, 2-byte address field Non-auto mode, 2-byte address field Transparent mode 3
Recognition of TEI	STAR	TA	All expect Transparent mode 2,3
Result of CRC-check (correct/ incorrect)	STAR	CRC	ALL
Data available in RFIFO (yes/no)	STAR	RDA	ALL
Abort condition detected (yes/no)	STAR	RAB	ALL
Data overflow during reception of a frame (yes/no)	STAR	RDO	ALL
Number of bytes received in RFIFO	RBCL	RBC4-0	ALL
Message length	RBCL RBCH	RBC11- OV	ALL

2.1.5.4 Transmission of Frames

A 2 × 32 byte FIFO-buffer (transmit pools) is provided in the transmit direction.

If the transmit pool is ready (which is true after an XPR-interrupt or if the XFW bit in STAR is set), the CPU can write a data block of up to 32 bytes to the transmit FIFO. After this, data transmission can be initiated by command.

Two different frame types can be transmitted:

– Transparent frames (command: XTF), or
– I-frames (command: XIF)

as shown in **figure 26**.

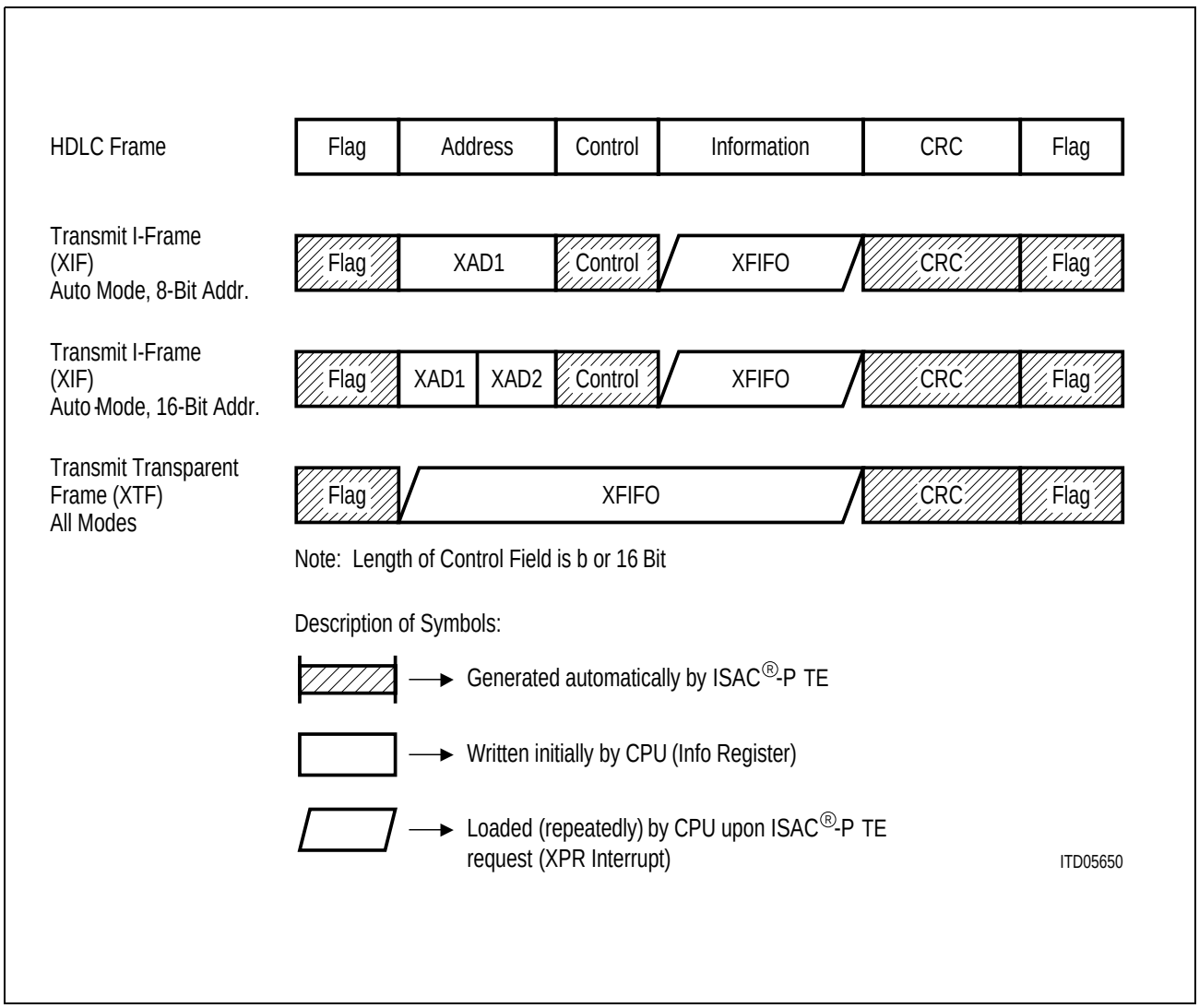


Figure 26
Transmit Data Flow

For transparent frames, the whole frame including address and control field must be written to the XFIFO.

The transmission of **I-frames** is possible only if the ISAC-P TE is operating in the auto-mode. The address and control field is autonomously generated by the ISAC-P TE and appended to the frame, only the data in the information field must be written to the XFIFO.

If a 2-byte address field has been selected, the ISAC-P TE takes the contents of the XAD 1 register to build the high byte of the address field, and the contents of the XAD 2 register to build the low byte of the address field.

Additionally the C/R-bit (bit 1 of the high byte address, as defined by LAPD-protocol) is set to “1” or “0” dependent on whether the frame is a command or a response.

In the case of a 1-byte address, the ISAC-P TE takes either the XAD 1 or XAD 2 register to differentiate between command or response frame (as defined by X.25 LAP B).

The control field is also generated by the ISAC-P TE including the receive and send sequence number and the poll/final (P/F) bit. For this purpose, the ISAC-P TE internally manages send and receive sequence number counters.

In the auto-mode, S-frames are sent autonomously by the ISAC-P TE. The transmission of U-frames, however, must be done by the CPU. U-frames must be sent as transparent frames (XTF), i.e. address and control field must be defined by the CPU.

Once the data transmission has been initiated by command (XTF or XIF), the data transfer between CPU and ICC is controlled by interrupts.

The ISAC-P TE repeatedly requests another data packet or block by means of an XPR-interrupt, every time no more than 32 bytes are stored in the XFIFO.

The processor can then write further data to the XFIFO and enable the continuation of frame transmission by issuing an XIF/XTF-command.

If the data block which has been written last to the XFIFO completes the current frame, this must be indicated additionally by setting the XME (Transmit Message End) command bit. The ISAC-P TE then terminates the frame properly by appending the CRC and closing flag.

If the CPU fails to respond to an XPR-interrupt within the given reaction time, a data underrun condition occurs (XFIFO holds no further valid data). In this case, the ISAC-P TE automatically aborts the current frame by sending seven consecutive “ones” (ABORT sequence).

The CPU is informed about this via an XDU-(Transmit Data Underrun) interrupt.

It is also possible to abort a message by software by issuing an XRES-(Transmitter RESet) command, which causes an XPR-interrupt.

After an end of message indication from the CPU (XME-command), the termination of the transmission operation is indicated differently, depending on the selected message transfer mode and the transmitted frame type.

If the ISAC-P TE is operating in the auto-mode, the window size (= number of outstanding unacknowledged frames) is limited to 1; therefore an acknowledgment is expected for every I-frame sent with an XIF-command. The acknowledgment may be provided either by a received S- or I-frame with corresponding receive sequence number (**see figure 23**).

If no acknowledgment is received within a certain time (programmable), the ISAC-P TE requests an acknowledgment by sending an S-frame with the poll bit set (P = 1) (RR or RNR). If no response is received again, this process is repeated in total CNT-times (retry count, programmable via TIMR-register).

The termination of the transmission operation may be indicated either with:

– XPR-interrupt, if a positive acknowledgment has been received,
– XMR-interrupt, if a negative acknowledgment has been received, i.e. the transmitted message must be repeated (XMR =Transmit Message Repeat),
– TIN-interrupt, if no acknowledgment has been received at all after CNT-times the expiration of the time period t_1 (TIN = Timer INterrupt, XPR-interrupt is issued additionally).

Note: Prerequisite for sending I-frames in the auto-mode (XIF) is that the internal operational mode of the timer has been selected in the MODE register (TMD bit = 1).

The transparent transmission of frames (XTF-command) is possible in all message transfer modes. The successful termination of a transparent transmission is indicated by the XPR-interrupt.

In the case where an IOM-interface mode is programmed (**see section 2.1.3**), a transmission may be aborted from the outside by setting stop/go bit to 1, provided DIM2-0 are programmed appropriately. An example of this is the occurrence of an S-bus D-channel collision. – If this happens before the first FIFO-pool has been completely transmitted and released, the ISAC-P TE will retransmit the frame automatically as soon as transmission is enabled again. Thus no µP-interaction is required.

On the other hand, if a transmission is inhibited by the stop/go bit after the first pool has already been released (and XPR generated), the ISAC-P TE aborts the frame and requests the processor to repeat the frame with an XMR-interrupt.

2.1.6 Documentation of the Auto-Mode

The Auto-Mode of the ISAC-P TE is only applicable for the states 7 and 8 of the LAPD-protocol. All other states (1 to 6) have to be performed in Non-Auto Mode (NAM). Therefore this documentation gives an overview of how the device reacts in the states 7 and 8, which reactions require software programming and which are done by the hardware itself, when interrupts and status register contents are set or change. The necessary software actions are also detailed in terms of command or mode register access.

The description is based on the SDL-Diagrams of the ETSI TS 46-20 dated 1989.

The diagrams are only annotated by documentary signs or texts (mostly register descriptions) and can therefore easily be interpreted by anyone familiar with the SDL-description of LAPD. All deviations that occur are specially marked and the impossible actions, path etc. are crossed out.

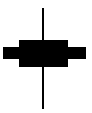
To get acquainted with this documentation, first read through the legend-description and the additional general considerations, then start with the diagrams, referring to the legend and the register description in the Technical Manual if necessary.

We hope you will profit from this documentation and use our software-saving auto-mode.

Legend of the Auto-Mode-Documentation

a) Symbols within a path

There are 3 symbols within a path

a.1. 

In the auto mode the device processes all subsequent state transitions branchings etc. up to the next symbol.

a.2. 

In the auto mode the device does not process the state transitions, branchings etc. Within the path appropriate directions are given with which the software can accomplish the required action.

a.3. 

A path cannot be implemented and no software or hardware action can change this. These paths are either optional or only applicable for window-size > 1.

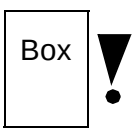
b) Symbols at a path

There is 1 symbol at a path

b.1.  marks the beginning of a path, for which a.3 applies.

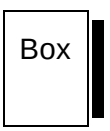
c) Symbols at an internal or external message box.

There are 2 symbols at a message box.

c.1. 

This symbol means, that the action described in the box is not possible. Either the action specified is not done at all or an additional action is taken (written into the box).

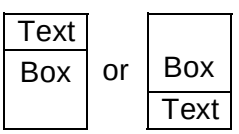
Note: The impossibility to perform the optional T203 timer-procedure is not explicitly mentioned; the corresponding actions are only crossed out.

c.2. 

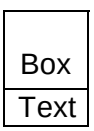
This symbol means, that within a software-path, by taking the prescribed register actions the contents of the box will be done automatically.

d) Text within boxes

Text within boxes can be grouped in one of two classes.

d.1. 

The text denotes an interrupt which is always associated with the event. (But can also be associated with other events). (See ISTA and EXIR register description in the Technical Manual for an interrupt description).

d.2. 

The text describes a register access

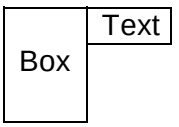
either a register read access to discriminate this state from others or to reach a branching condition

or a register write access to give a command.

The text is placed in the box that describes the functions for which the register access is needed.

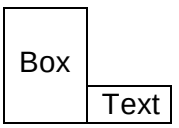
e) Text attached at the side of boxes

e.1.



The text describes an Interrupt associated with the contents of the box. The interrupt is always associated with the box contents, if the interrupt name is not followed by a "/", it is associated only under appropriate conditions if a "/" is behind it.

e.2.

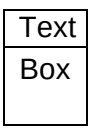


The text describes a possible or mandatory change of a bit in a status-register associated with the contents of the box.

(The attached texts can also be placed on the left side.)

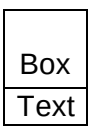
f) Text above and below boxes

f.1.



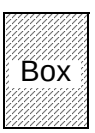
Text describes a mandatory action to be performed on the contents of the box.

f.2.



Text describes a mandatory action to be taken as a result of the contents of the box.
Action here means register access.

g) Shade boxes



The box describes an impossible state or action for the device.

Additional General Considerations when Using the Auto-Mode

a) Switching from Auto-Mode to Non-Auto Mode.

As mentioned in the introduction the Auto-Mode is only applicable in the states 7 and 8 of the LAPD. Therefore whenever these states have to be left (which is indicated by a “Mode:NAM” text) there are several actions to be taken that could not all be detailed in the SDL-diagrams:

a.1) Write Non-Auto Mode and TMD = 0 into the mode register.

a.2) Write the timer register with an arbitrary value to stop it. The timer T200 as specified in the LAPD-protocol is implemented in the hardware only in the states 7 and 8; in all other states this or any other timer-procedure has to be done by the software with the possible use of the timer in external timer mode.

a.3) Read the WFA-bit of the STAR2-register and store it in a software variable. The information in this bit may be necessary for later decisions. When switching from Auto-Mode to Non-Auto Mode XPR-interrupts may be lost.

a.4) In the Non-Auto Mode the software has to decode I-, U- and S-frames because I- and S-frames are only handled autonomously in the Auto-Mode.

a.5) The RSC- and PCE-interrupts, the contents of the STAR2-register and the RRNR bit in the STAR-register are only meaningful within the Auto-Mode.

a.6) Leave some time before RHR or XRES is written to reset the counters, as a currently sent frame may not be finished yet.

b) What has to be written to the XFIFO?

In the legend description when the software has to write contents of a frame to the XFIFO only “XFIFO” is shown in the corresponding box. We shall given here a general rule of what has to be written to the XFIFO:

a) For sending an I-frame with CMDR:XIF, only the information field content, i.e. no SAPI, TEI, control field should be written to the XFIFO.

b) For sending an U-frame or any other frame with CMDR:XTF, the SAPI, TEI and the control field has to be written to the XFIFO.

c) The interrupts XPR and XMR.

The occurrence of an XPR-interrupt in Auto-Mode after an XIF-command indicates that the I-frame sent was acknowledged and the next I-frame can be sent, if STAR2:TREC indicates state 7 and STAR:RRNR indicates Peer Rec not busy. If Peer Rec is busy after an XPR, the software should wait for the next RSC-interrupt before sending the next I-frame. If the XPR happens to be in the Timer Recovery state, the software has to poll the STAR2-register until the state Multiple Frame Established is reached or a TIN-interrupt is issued which requires Auto-Mode to be left (One of these two conditions will occur before the time T200 $\times$ N200). In Non-Auto Mode or after an XTF-command the XPR just indicates, that the frame was sent successfully.

The occurrence of an XMR-interrupt in Auto-Mode after an XIF-command indicates that the I-frame sent was either rejected by the Peer Entity or that a collision occurred on the S-interface. In both cases the I-frame has to be retransmitted (after an eventual waiting for the RSC-interrupt if the Peer Rec was busy; after an XMR the device will always be in the state 7). In Non-Auto Mode or after an XTF-command the XMR indicates that a collision occurred on the S-interface and the frame has to be retransmitted.

d) The resetting of the RC-variable:

The RC-variable is reset in the ISAC-P TE and ISAC-S when leaving the state Timer Recovery. The SLD-diagrams indicate a reset in the state Multiple Frame Established when T200 expires. There is no difference to the outside world between these implementations however our implementation is clearer.

e) The timer T203 procedure:

We do not fully support the optional timer T203 procedure, but we can still find out whether or not S-frames are sent on the link in the Auto-Mode. By polling the STAR2:SDET bit and (re)starting a software timer whenever a one is read we can build a quasi T203 procedure which handles approximately the same task. When T203 expires one is supposed to go into the Timer Recovery State with RC = 0. This is possible for the ISAC-P TE and ISAC-S by just writing the STI-bit in the CMDR register (Auto-Mode and Internal Timer Mode assumed).

f) The congestion procedure as defined in the 1 TR 6 of the “Deutsche Bundespost”.

In the 1 TR 6a variable N2 $\times$ 4 is defined for the maximum number of Peer Busy requests. The 1 TR is in this respect not compatible with the Q921 of CCITT or the ETSI 46 – 20 but it is, nevertheless, sensible to avoid getting into a hangup situation. With the ISAC-P TE and ISAC-S this procedure can be implemented:

After receiving an RSC-interrupt with RRNR set one starts a software – timer. The timer is reset and stopped if one either receives another RSC-interrupt with a reset RRNR, if one receives a TIN-interrupt or if other conditions occur that result in a reestablishment of the link. The timer expires after $N2 \times 4 \times T200$ and in this case the 1 TR 6 recommends a reestablishment of the link.

g) Dealing with error conditions: The SLD-diagrams do not give a very detailed description of how to deal with errors. Therefore we prepared a special Application Note: "How to deal with an error condition of the LAPD-protocol with your ISAC-P TE or ISAC-S".

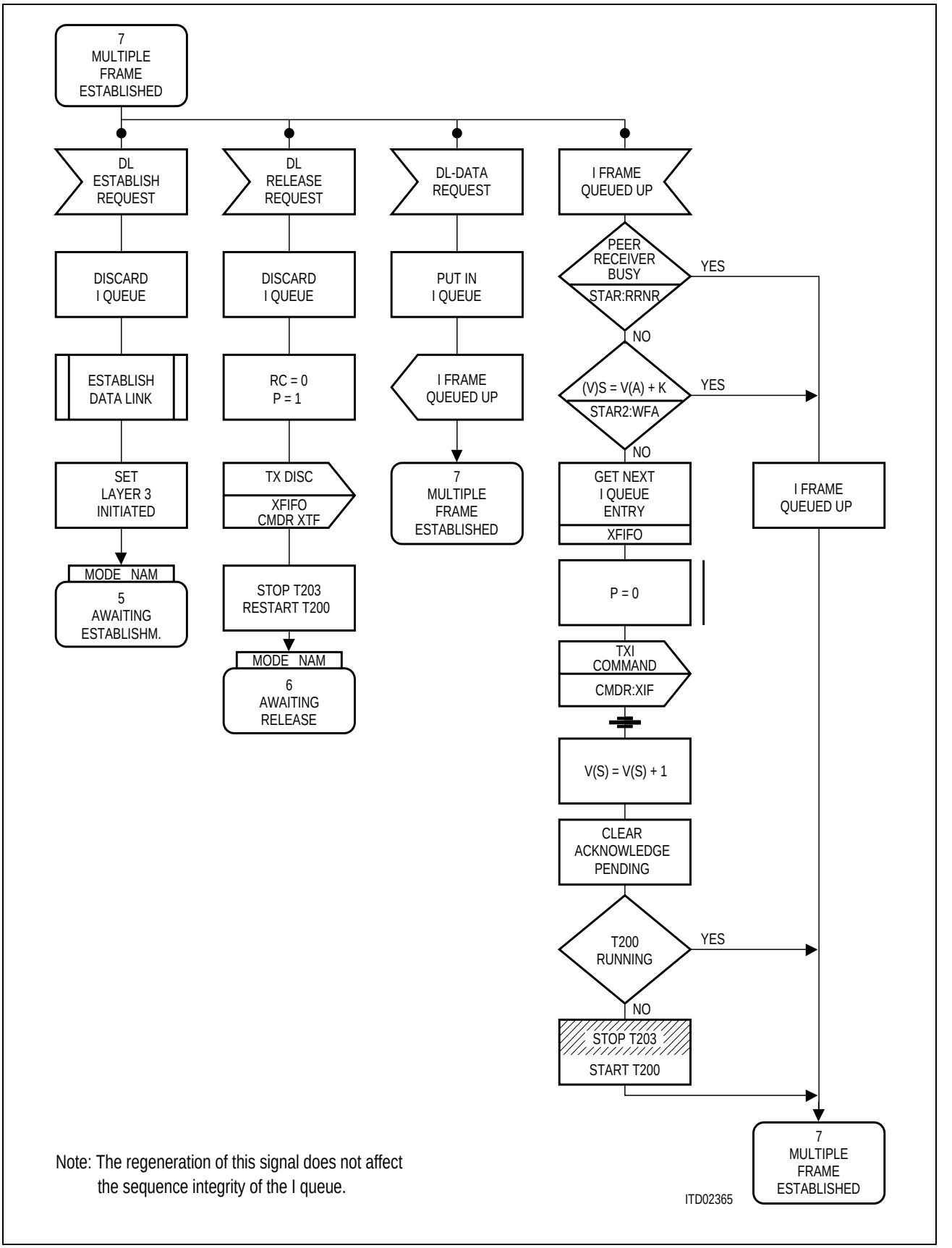

7
MULTIPLE
FRAME
ESTABLISHED
DL
ESTABLISH
REQUEST
DL
RELEASE
REQUEST
DL-DATA
REQUEST
I FRAME
QUEUED UP
DISCARD
I QUEUE
DISCARD
I QUEUE
PUT IN
I QUEUE
PEER
RECEIVER
BUSY
STAR:RRNR
YES
NO
ESTABLISH
DATA LINK
RC = 0
P = 1
I FRAME
QUEUED UP
(V)S = V(A) + K
STAR2:WFA
YES
NO
SET
LAYER 3
INITIATED
TX DISC
XFIFO
CMDR XTF
7
MULTIPLE
FRAME
ESTABLISHED
GET NEXT
I QUEUE
ENTRY
XFIFO
I FRAME
QUEUED UP
MODE NAM
5
AWAITING
ESTABLISHM.
STOP T203
RESTART T200
P = 0
MODE NAM
6
AWAITING
RELEASE
TXI
COMMAND
CMDR:XIF
V(S) = V(S) + 1
CLEAR
ACKNOWLEDGE
PENDING
T200
RUNNING
YES
NO
STOP T203
START T200
7
MULTIPLE
FRAME
ESTABLISHED
Note: The regeneration of this signal does not affect
the sequence integrity of the I queue.
ITD02365

Figure 27a

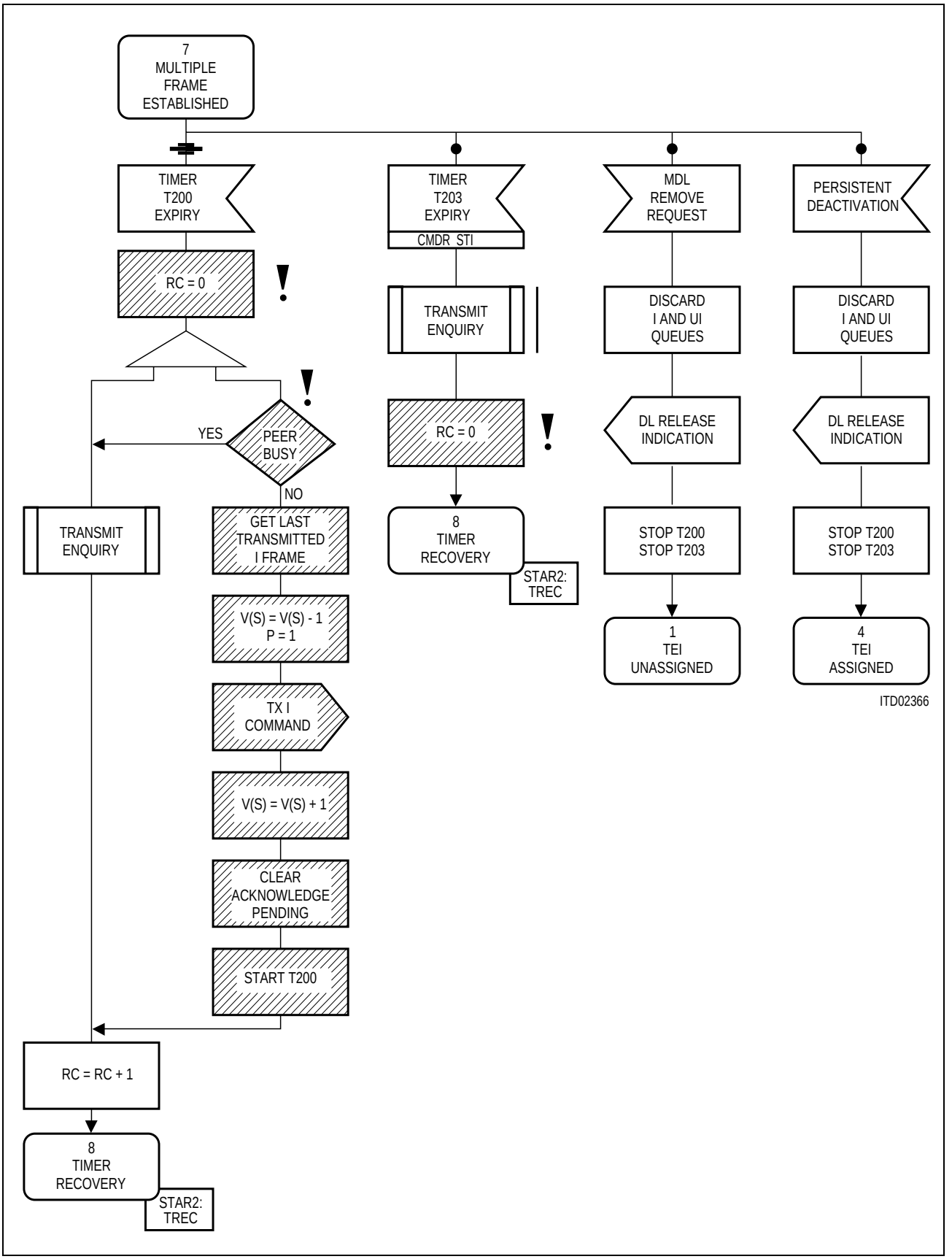

7
MULTIPLE
FRAME
ESTABLISHED
TIMER
T200
EXPIRY
RC = 0
!
YES
PEER
BUSY
!
NO
TRANSMIT
ENQUIRY
GET LAST
TRANSMITTED
I FRAME
V(S) = V(S) - 1
P = 1
TX I
COMMAND
V(S) = V(S) + 1
CLEAR
ACKNOWLEDGE
PENDING
START T200
RC = RC + 1
8
TIMER
RECOVERY
STAR2:
TREC
TIMER
T203
EXPIRY
CMDR STI
TRANSMIT
ENQUIRY
RC = 0
!
8
TIMER
RECOVERY
STAR2:
TREC
MDL
REMOVE
REQUEST
DISCARD
I AND UI
QUEUES
DL RELEASE
INDICATION
STOP T200
STOP T203
1
TEI
UNASSIGNED
PERSISTENT
DEACTIVATION
DISCARD
I AND UI
QUEUES
DL RELEASE
INDICATION
STOP T200
STOP T203
4
TEI
ASSIGNED
ITD02366

Figure 27b

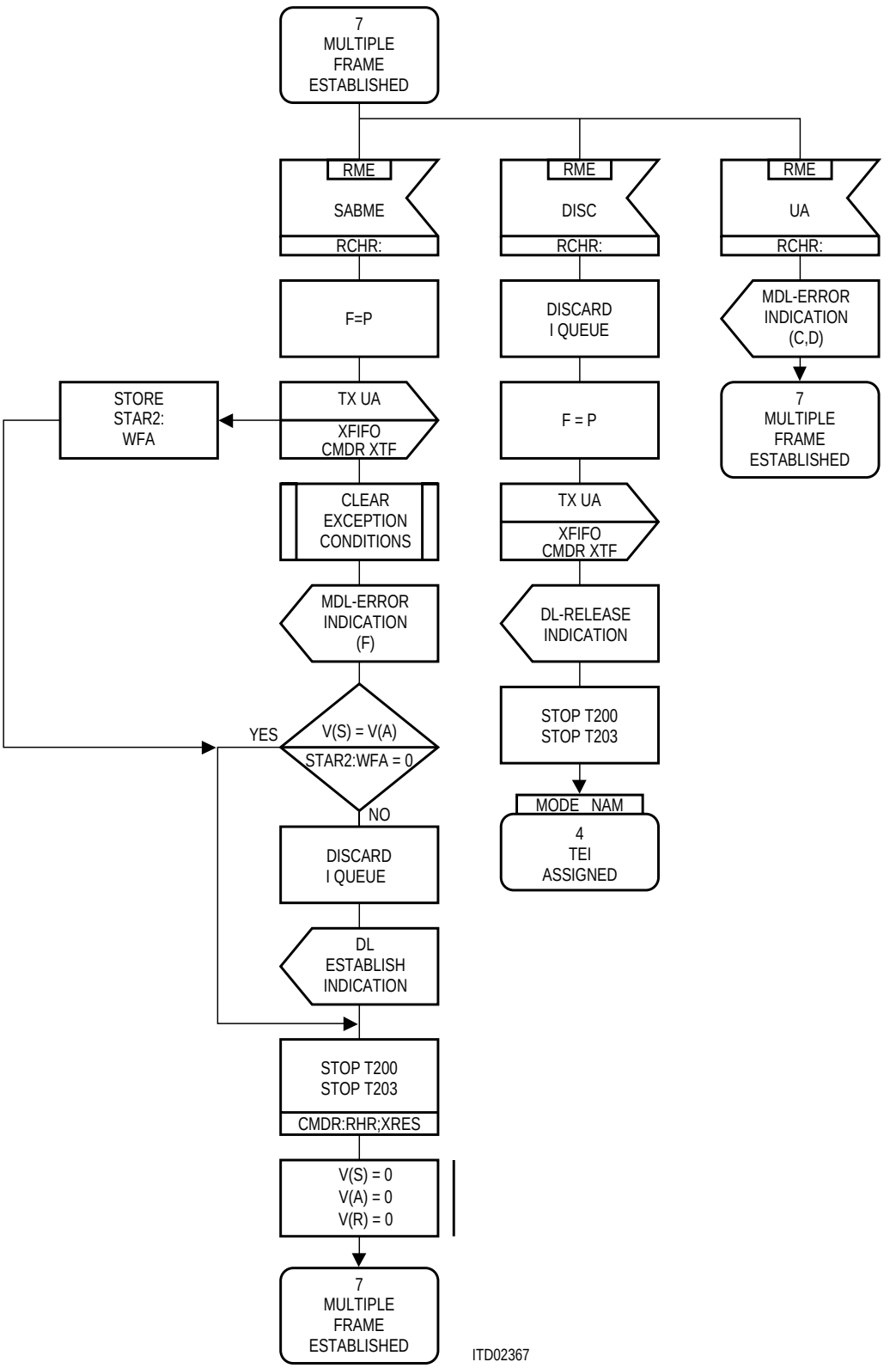

7
MULTIPLE
FRAME
ESTABLISHED
RME
SABME
RCHR:
F=P
TX UA
XFIFO
CMDR XTF
STORE
STAR2:
WFA
CLEAR
EXCEPTION
CONDITIONS
MDL-ERROR
INDICATION
(F)
YES
V(S) = V(A)
STAR2:WFA = 0
NO
DISCARD
I QUEUE
DL
ESTABLISH
INDICATION
STOP T200
STOP T203
CMDR:RHR;XRES
V(S) = 0
V(A) = 0
V(R) = 0
7
MULTIPLE
FRAME
ESTABLISHED
RME
DISC
RCHR:
DISCARD
I QUEUE
F = P
TX UA
XFIFO
CMDR XTF
DL-RELEASE
INDICATION
STOP T200
STOP T203
MODE NAM
4
TEI
ASSIGNED
RME
UA
RCHR:
MDL-ERROR
INDICATION
(C,D)
7
MULTIPLE
FRAME
ESTABLISHED
ITD02367

Figure 27c

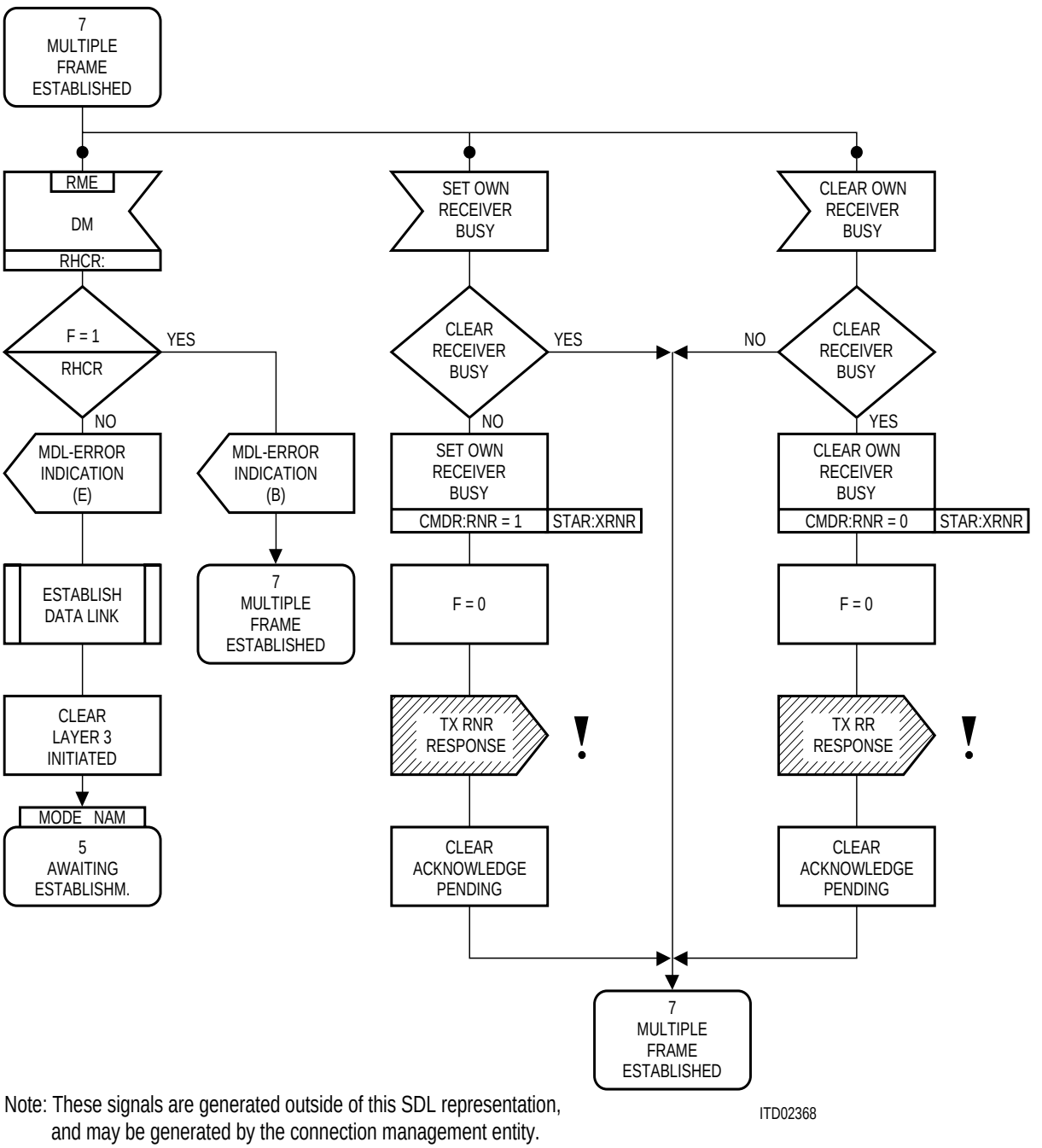

7
MULTIPLE
FRAME
ESTABLISHED
RME
DM
RHCR:
F = 1
RHCR
YES
NO
MDL-ERROR
INDICATION
(E)
MDL-ERROR
INDICATION
(B)
ESTABLISH
DATA LINK
7
MULTIPLE
FRAME
ESTABLISHED
CLEAR
LAYER 3
INITIATED
MODE NAM
5
AWAITING
ESTABLISHM.
SET OWN
RECEIVER
BUSY
CLEAR
RECEIVER
BUSY
YES
NO
SET OWN
RECEIVER
BUSY
CMDR:RNR = 1
STAR:XRNR
F = 0
TX RNR
RESPONSE
!
CLEAR
ACKNOWLEDGE
PENDING
CLEAR OWN
RECEIVER
BUSY
CLEAR
RECEIVER
BUSY
NO
YES
CLEAR OWN
RECEIVER
BUSY
CMDR:RNR = 0
STAR:XRNR
F = 0
TX RR
RESPONSE
!
CLEAR
ACKNOWLEDGE
PENDING
7
MULTIPLE
FRAME
ESTABLISHED
Note: These signals are generated outside of this SDL representation,
and may be generated by the connection management entity.
ITD02368

Figure 27d

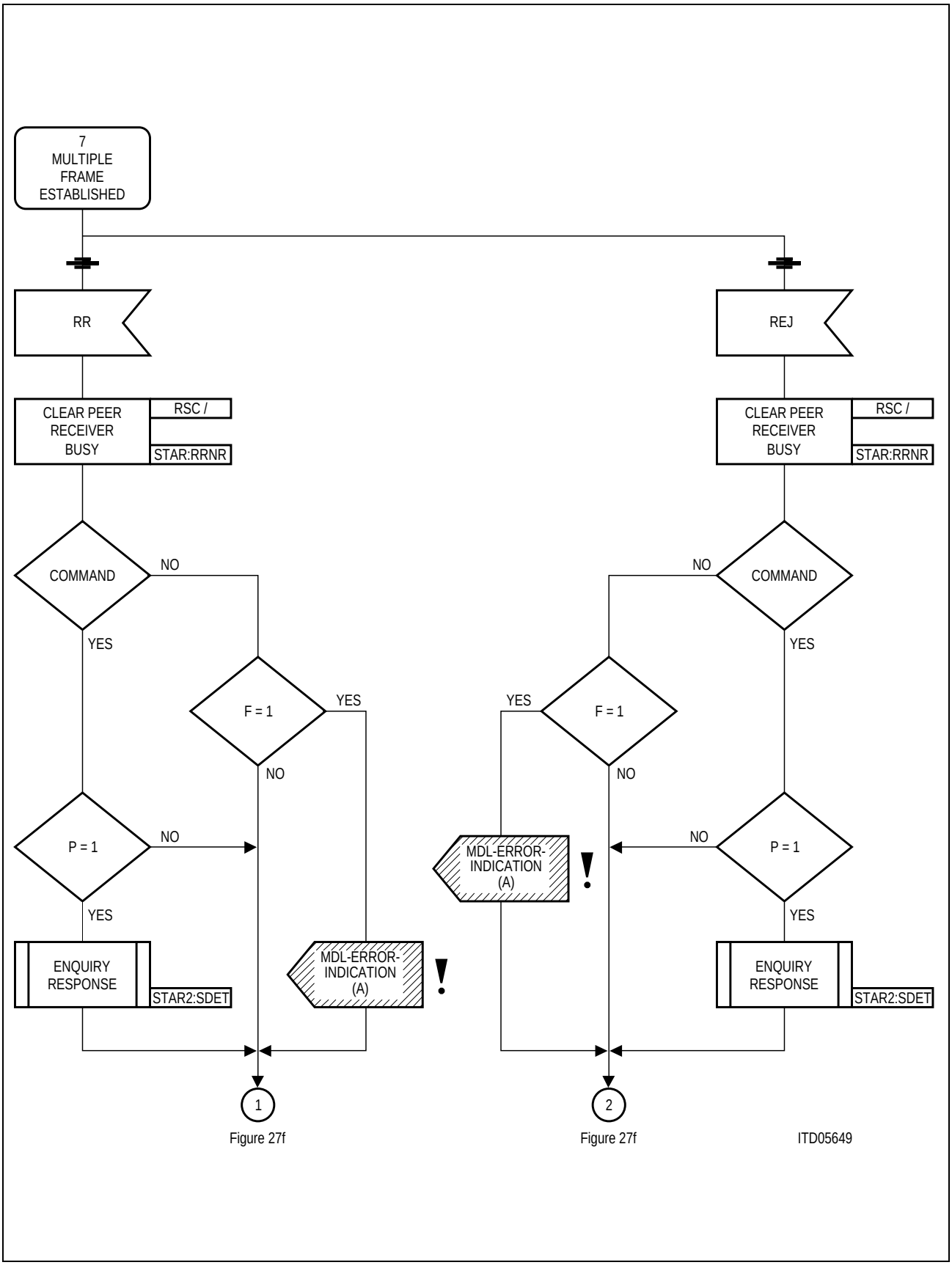

7
MULTIPLE
FRAME
ESTABLISHED
RR
REJ
CLEAR PEER
RECEIVER
BUSY
RSC /
STAR:RRNR
CLEAR PEER
RECEIVER
BUSY
RSC /
STAR:RRNR
COMMAND
NO
YES
COMMAND
NO
YES
F = 1
YES
NO
F = 1
YES
NO
P = 1
NO
YES
P = 1
NO
YES
MDL-ERROR-
INDICATION
(A)
!
ENQUIRY
RESPONSE
STAR2:SDET
MDL-ERROR-
INDICATION
(A)
!
ENQUIRY
RESPONSE
STAR2:SDET
1
2
Figure 27f
Figure 27f
ITD05649

Figure 27e

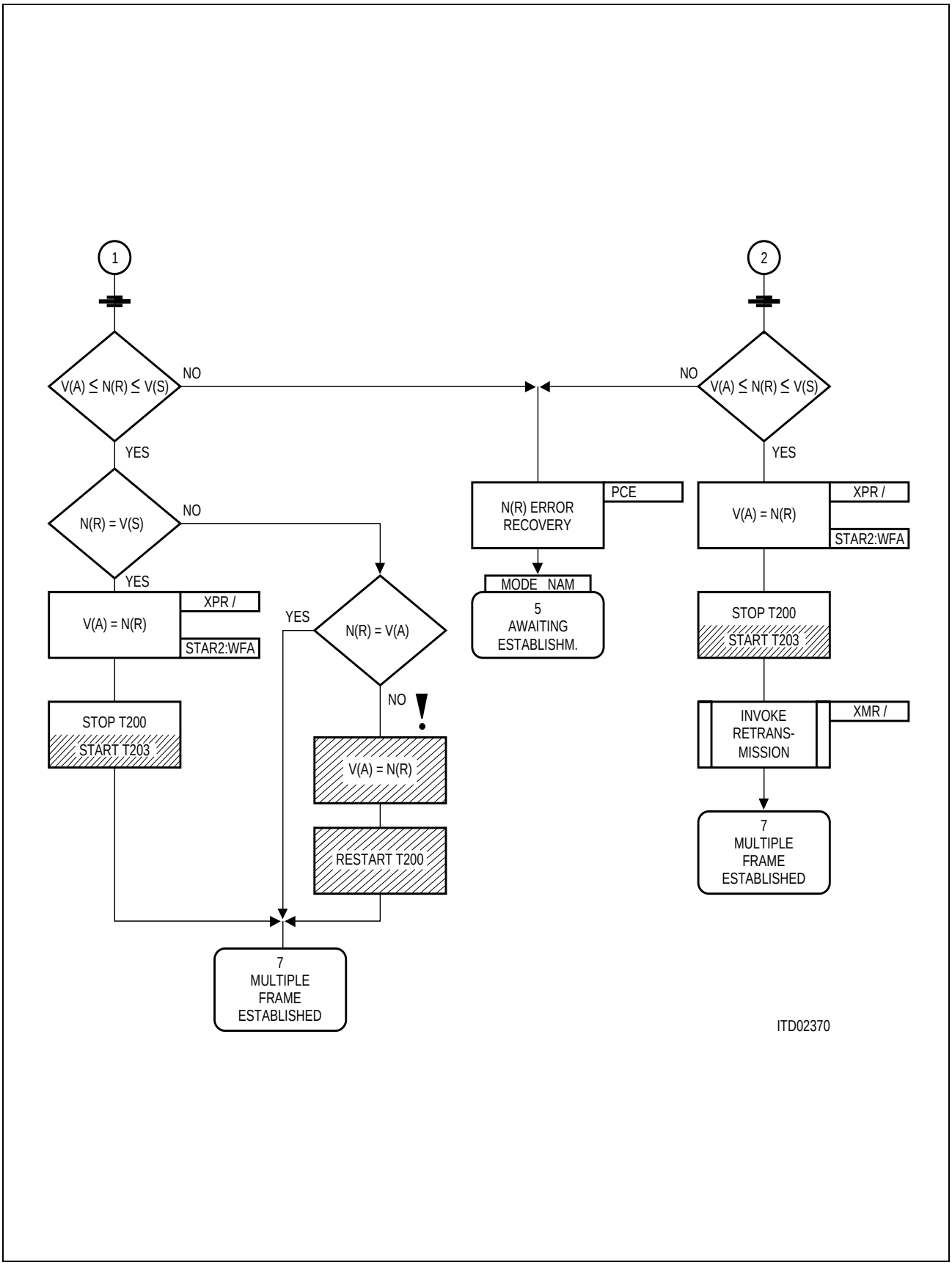

1
2
V(A) ≤ N(R) ≤ V(S)
NO
YES
N(R) = V(S)
NO
YES
V(A) = N(R)
XPR /
STAR2:WFA
STOP T200
START T203
YES
N(R) = V(A)
NO
!
V(A) = N(R)
RESTART T200
7
MULTIPLE
FRAME
ESTABLISHED
N(R) ERROR
RECOVERY
PCE
MODE NAM
5
AWAITING
ESTABLISHM.
NO
V(A) ≤ N(R) ≤ V(S)
YES
V(A) = N(R)
XPR /
STAR2:WFA
STOP T200
START T203
INVOKE
RETRANS-
MISSION
XMR /
7
MULTIPLE
FRAME
ESTABLISHED
ITD02370

Figure 27f

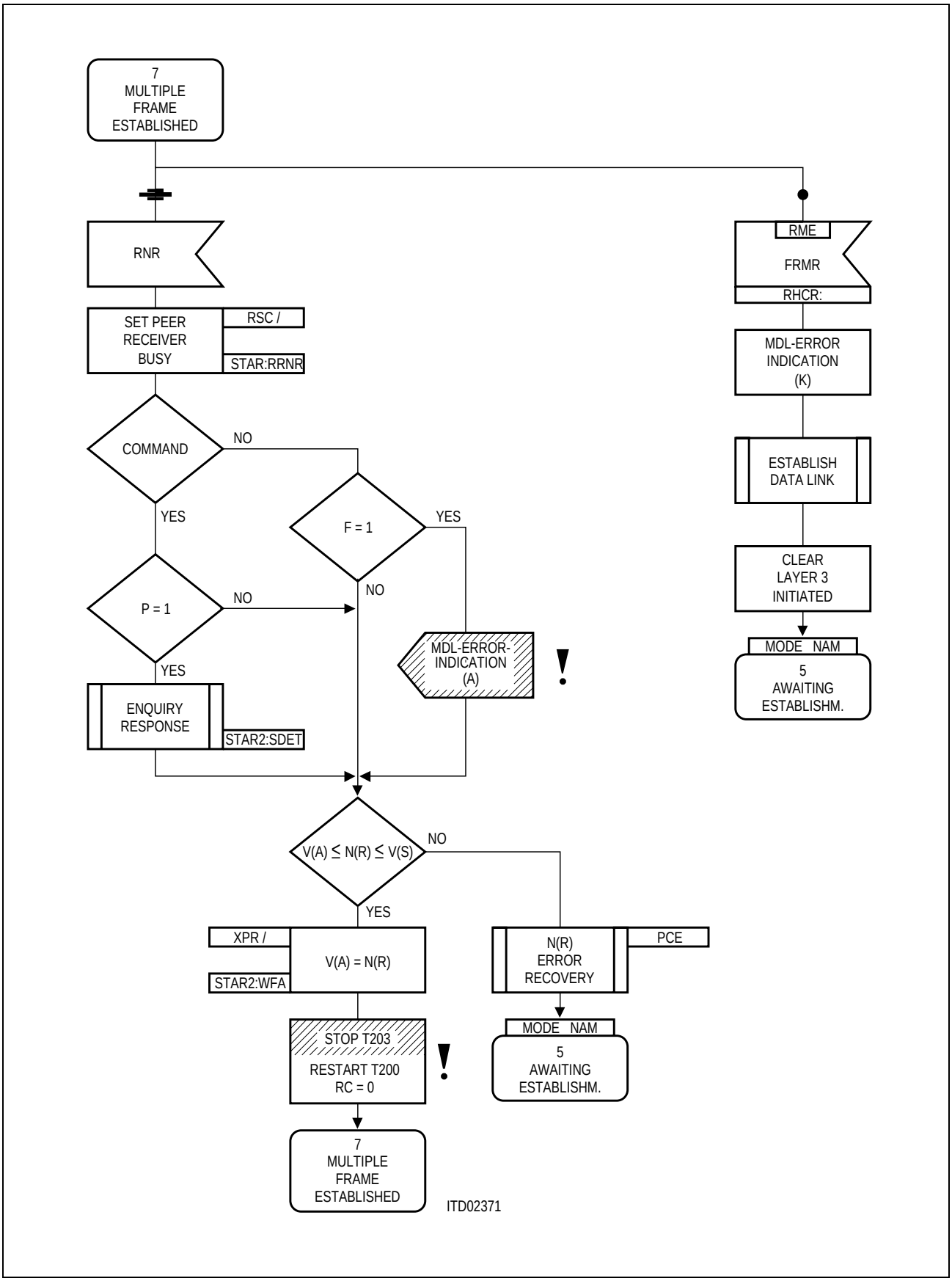

7
MULTIPLE
FRAME
ESTABLISHED
RNR
SET PEER
RECEIVER
BUSY
RSC /
STAR:RRNR
COMMAND
NO
YES
P = 1
NO
YES
ENQUIRY
RESPONSE
STAR2:SDET
F = 1
YES
NO
MDL-ERROR-
INDICATION
(A)
!
V(A) ≤ N(R) ≤ V(S)
NO
YES
XPR /
STAR2:WFA
V(A) = N(R)
STOP T203
RESTART T200
RC = 0
!
7
MULTIPLE
FRAME
ESTABLISHED
ITD02371
RME
FRMR
RHCR:
MDL-ERROR
INDICATION
(K)
ESTABLISH
DATA LINK
CLEAR
LAYER 3
INITIATED
MODE NAM
5
AWAITING
ESTABLISHM.
N(R)
ERROR
RECOVERY
PCE
MODE NAM
5
AWAITING
ESTABLISHM.

Figure 27g

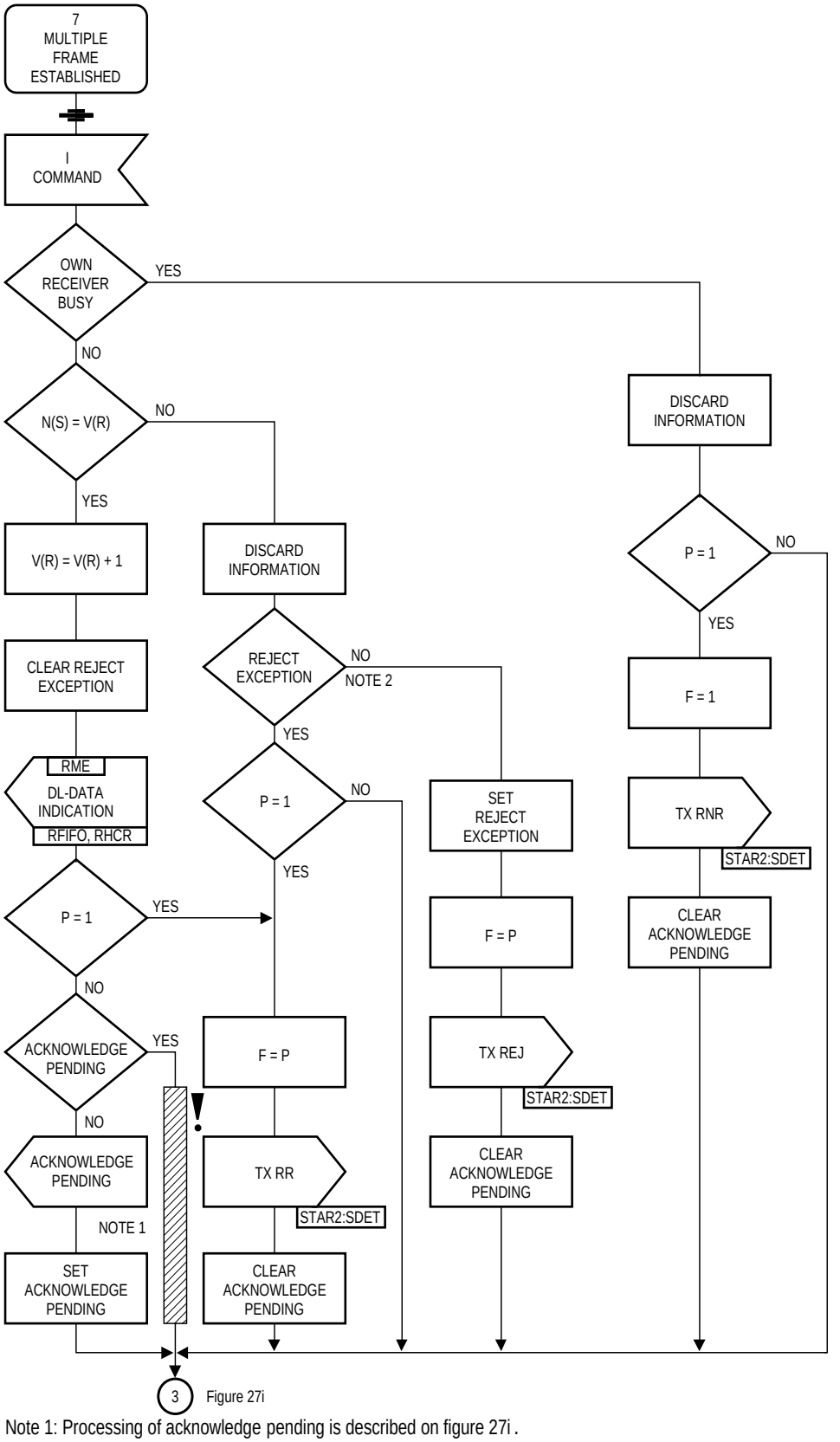

7
MULTIPLE
FRAME
ESTABLISHED
I
COMMAND
OWN
RECEIVER
BUSY
YES
NO
N(S) = V(R)
NO
YES
V(R) = V(R) + 1
CLEAR REJECT
EXCEPTION
RME
DL-DATA
INDICATION
RFIFO, RHCR
P = 1
YES
NO
ACKNOWLEDGE
PENDING
YES
NO
ACKNOWLEDGE
PENDING
NOTE 1
SET
ACKNOWLEDGE
PENDING
DISCARD
INFORMATION
REJECT
EXCEPTION
NO
NOTE 2
YES
P = 1
NO
YES
F = P
TX RR
STAR2:SDET
CLEAR
ACKNOWLEDGE
PENDING
SET
REJECT
EXCEPTION
F = P
TX REJ
STAR2:SDET
CLEAR
ACKNOWLEDGE
PENDING
DISCARD
INFORMATION
P = 1
NO
YES
F = 1
TX RNR
STAR2:SDET
CLEAR
ACKNOWLEDGE
PENDING
3
Figure 27i
Note 1: Processing of acknowledge pending is described on figure 27i .
Note 2: This SDL-representation does not include the optional procedure in Appendix I.
ITD05648

Figure 27h

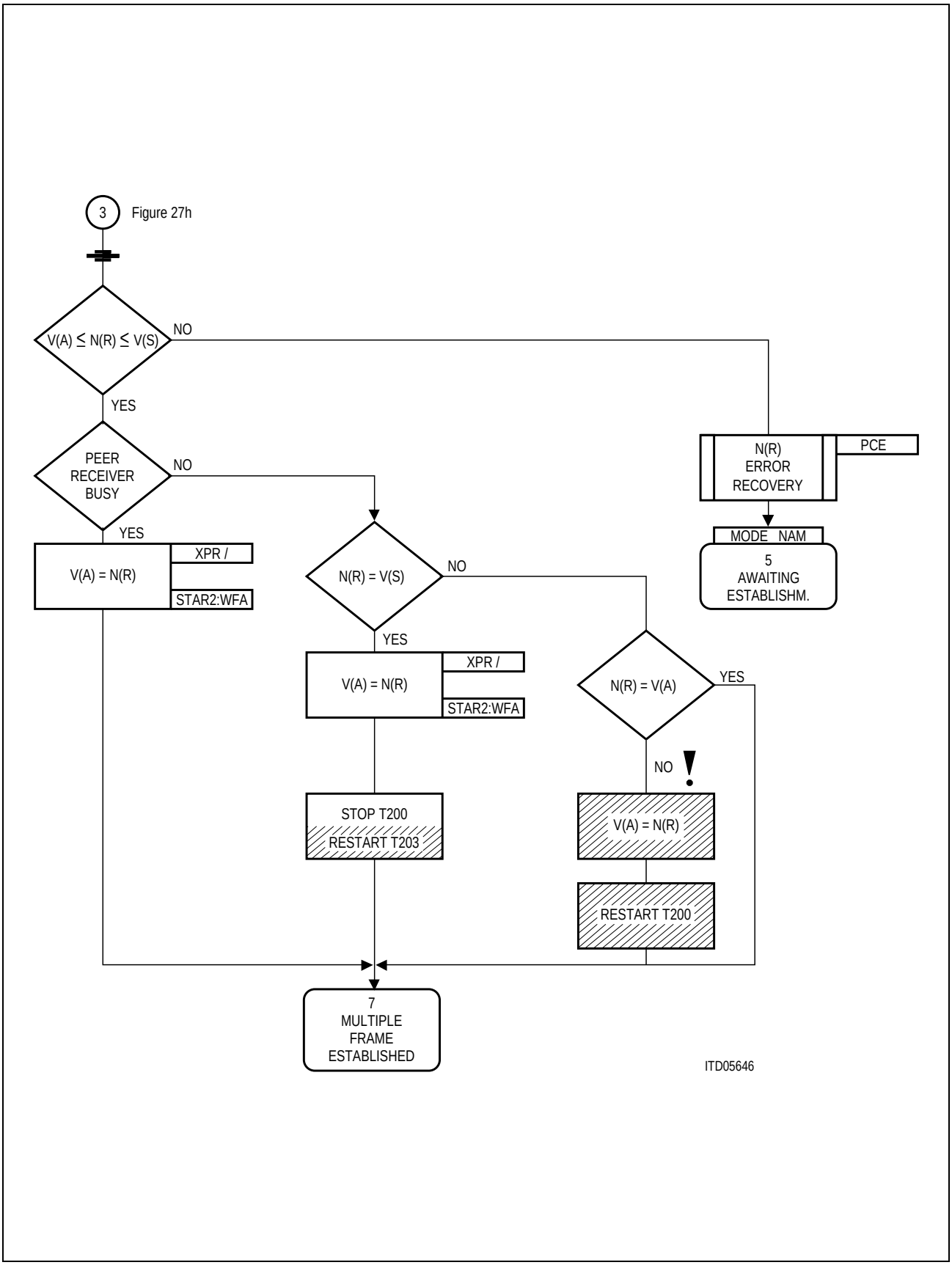

3
Figure 27h
V(A) ≤ N(R) ≤ V(S)
NO
YES
PEER RECEIVER BUSY
NO
YES
V(A) = N(R)
XPR /
STAR2:WFA
N(R) = V(S)
NO
YES
V(A) = N(R)
XPR /
STAR2:WFA
STOP T200
RESTART T203
N(R) = V(A)
YES
NO
V(A) = N(R)
RESTART T200
N(R) ERROR RECOVERY
PCE
MODE NAM
5
AWAITING ESTABLISHM.
7
MULTIPLE FRAME ESTABLISHED
ITD05646

Figure 27i

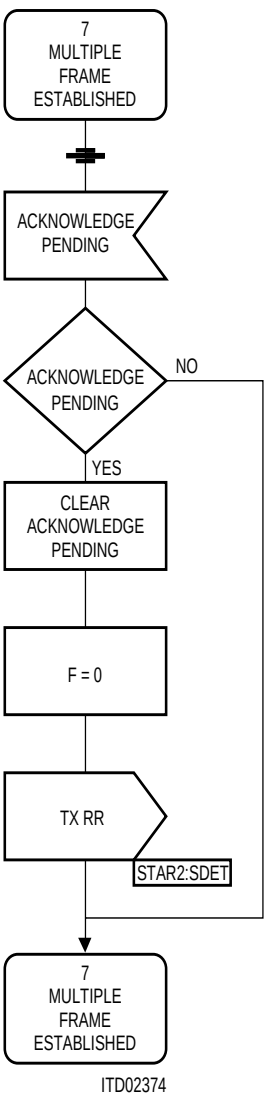

7
MULTIPLE
FRAME
ESTABLISHED
ACKNOWLEDGE
PENDING
ACKNOWLEDGE
PENDING
NO
YES
CLEAR
ACKNOWLEDGE
PENDING
F = 0
TX RR
STAR2:SDET
7
MULTIPLE
FRAME
ESTABLISHED
ITD02374

Figure 27j

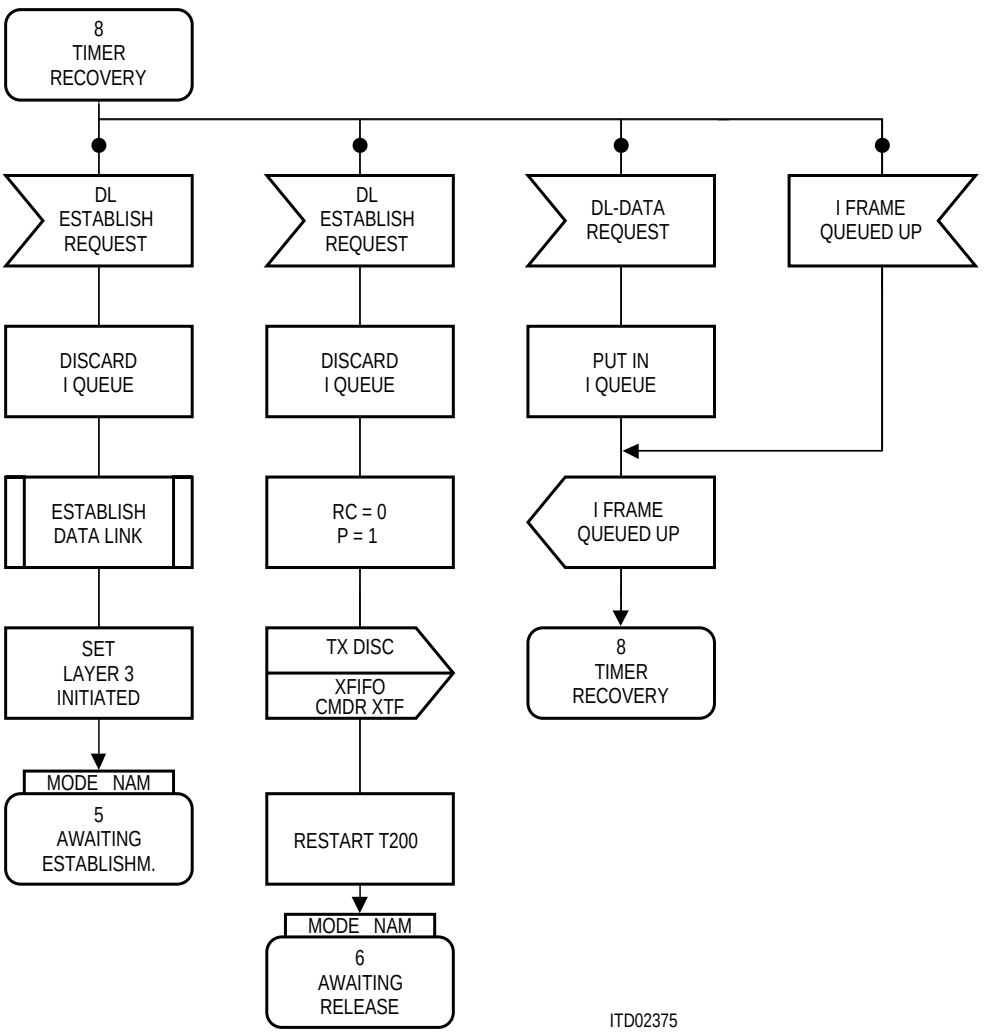

8
TIMER
RECOVERY
DL
ESTABLISH
REQUEST
DL
ESTABLISH
REQUEST
DL-DATA
REQUEST
I FRAME
QUEUED UP
DISCARD
I QUEUE
DISCARD
I QUEUE
PUT IN
I QUEUE
ESTABLISH
DATA LINK
RC = 0
P = 1
I FRAME
QUEUED UP
SET
LAYER 3
INITIATED
TX DISC
XFIFO
CMDR XTF
8
TIMER
RECOVERY
MODE NAM
5
AWAITING
ESTABLISHM.
RESTART T200
MODE NAM
6
AWAITING
RELEASE
ITD02375

Figure 28a

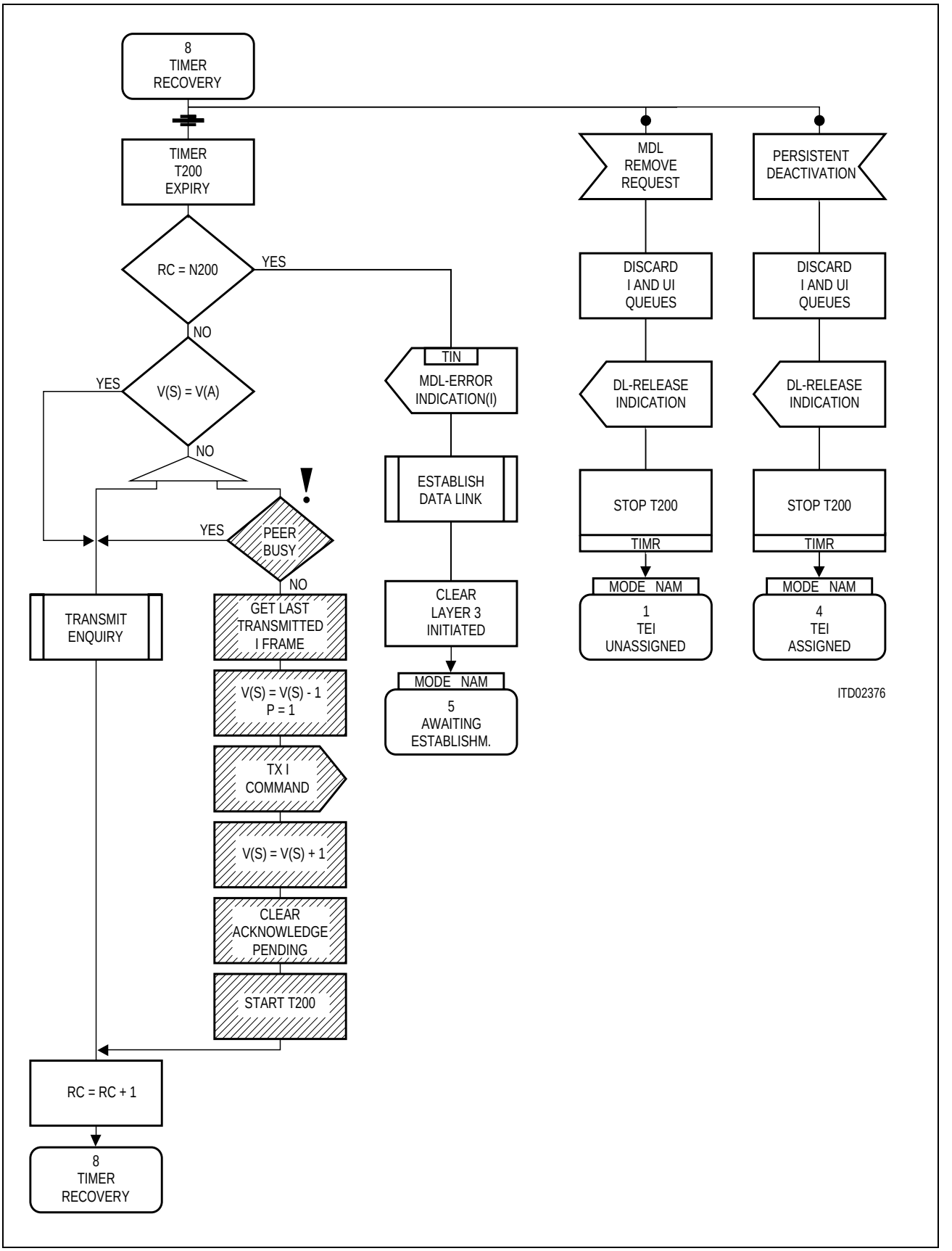

8
TIMER
RECOVERY
TIMER
T200
EXPIRY
RC = N200
YES
NO
V(S) = V(A)
YES
NO
PEER
BUSY
YES
NO
TRANSMIT
ENQUIRY
GET LAST
TRANSMITTED
I FRAME
V(S) = V(S) - 1
P = 1
TX I
COMMAND
V(S) = V(S) + 1
CLEAR
ACKNOWLEDGE
PENDING
START T200
RC = RC + 1
8
TIMER
RECOVERY
TIN
MDL-ERROR
INDICATION(I)
ESTABLISH
DATA LINK
CLEAR
LAYER 3
INITIATED
MODE NAM
5
AWAITING
ESTABLISHM.
MDL
REMOVE
REQUEST
DISCARD
I AND UI
QUEUES
DL-RELEASE
INDICATION
STOP T200
TIMR
MODE NAM
1
TEI
UNASSIGNED
PERSISTENT
DEACTIVATION
DISCARD
I AND UI
QUEUES
DL-RELEASE
INDICATION
STOP T200
TIMR
MODE NAM
4
TEI
ASSIGNED
ITD02376

Figure 28b

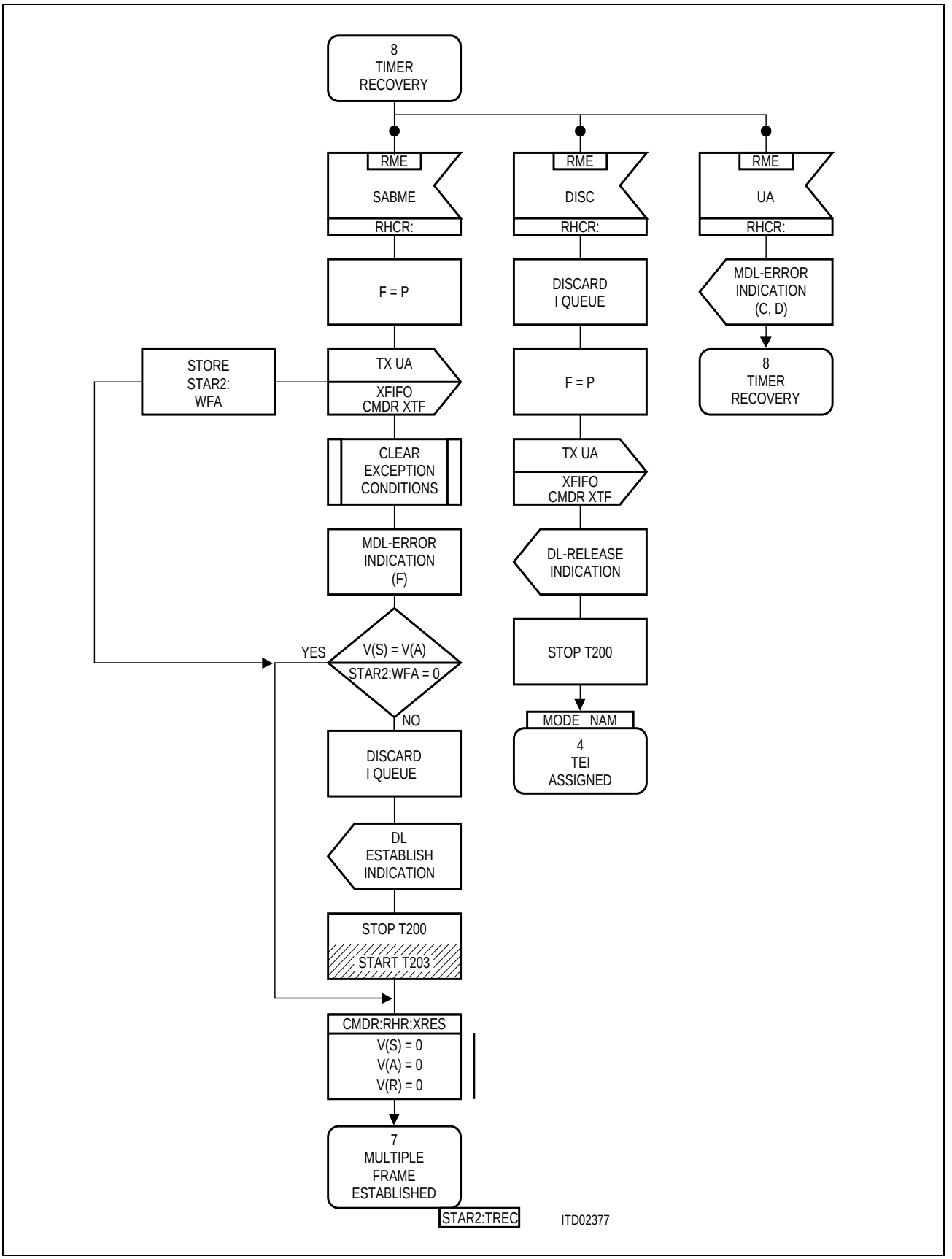

8
TIMER
RECOVERY
RME
SABME
RHCR:
F = P
TX UA
XFIFO
CMDR XTF
STORE
STAR2:
WFA
CLEAR
EXCEPTION
CONDITIONS
MDL-ERROR
INDICATION
(F)
YES
V(S) = V(A)
STAR2:WFA = 0
NO
DISCARD
I QUEUE
DL
ESTABLISH
INDICATION
STOP T200
START T203
CMDR:RHR;XRES
V(S) = 0
V(A) = 0
V(R) = 0
7
MULTIPLE
FRAME
ESTABLISHED
STAR2:TREC
RME
DISC
RHCR:
DISCARD
I QUEUE
F = P
TX UA
XFIFO
CMDR XTF
DL-RELEASE
INDICATION
STOP T200
MODE NAM
4
TEI
ASSIGNED
RME
UA
RHCR:
MDL-ERROR
INDICATION
(C, D)
8
TIMER
RECOVERY
ITD02377

Figure 28c

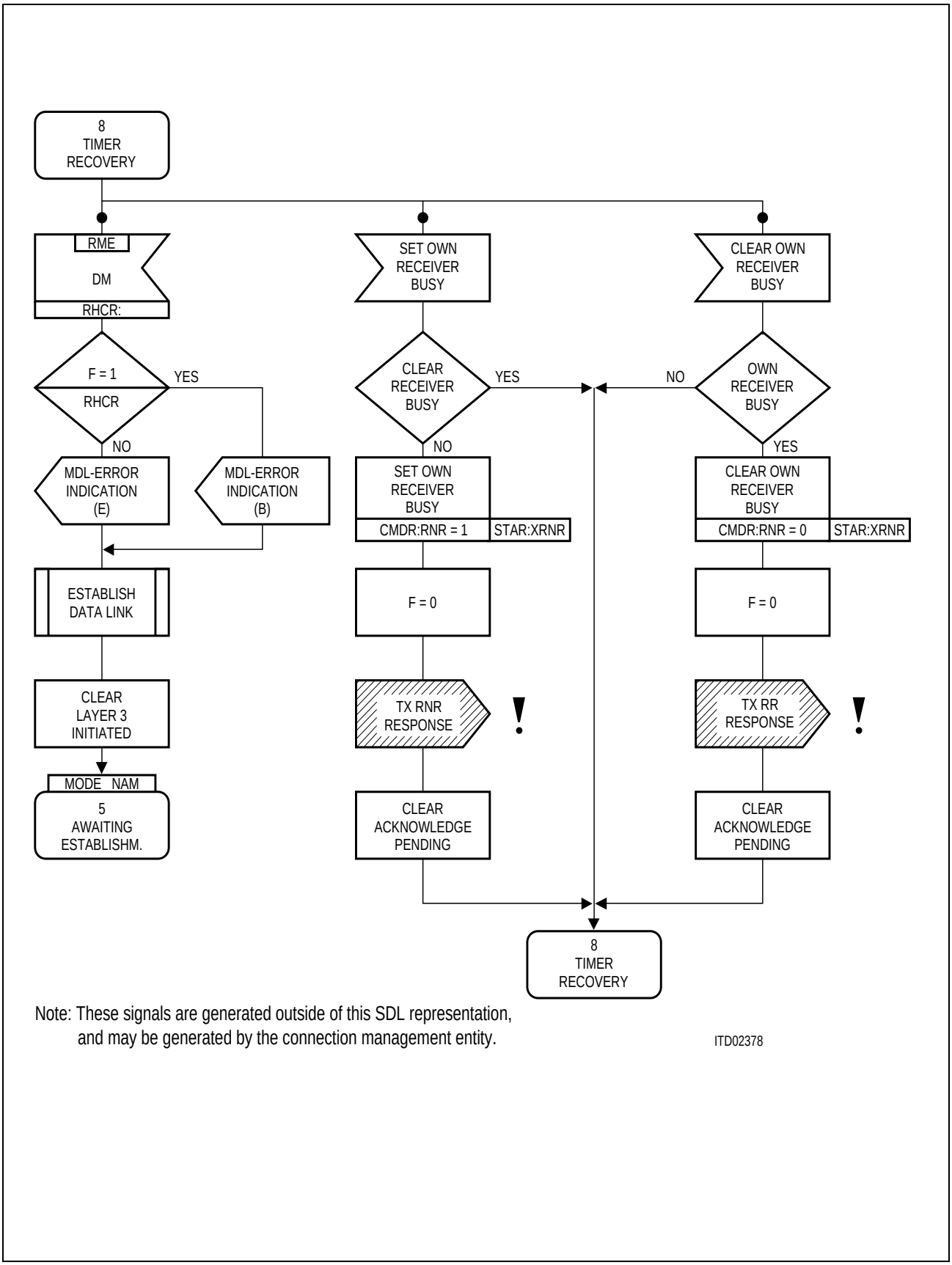

8
TIMER
RECOVERY
RME
DM
RHCR:
F = 1
RHCR
YES
NO
MDL-ERROR
INDICATION
(E)
MDL-ERROR
INDICATION
(B)
ESTABLISH
DATA LINK
CLEAR
LAYER 3
INITIATED
MODE NAM
5
AWAITING
ESTABLISHM.
SET OWN
RECEIVER
BUSY
CLEAR
RECEIVER
BUSY
YES
NO
SET OWN
RECEIVER
BUSY
CMDR:RNR = 1
STAR:XRNR
F = 0
TX RNR
RESPONSE
!
CLEAR
ACKNOWLEDGE
PENDING
CLEAR OWN
RECEIVER
BUSY
OWN
RECEIVER
BUSY
NO
YES
CLEAR OWN
RECEIVER
BUSY
CMDR:RNR = 0
STAR:XRNR
F = 0
TX RR
RESPONSE
!
CLEAR
ACKNOWLEDGE
PENDING
8
TIMER
RECOVERY
Note: These signals are generated outside of this SDL representation,
and may be generated by the connection management entity.
ITD02378

Figure 28d

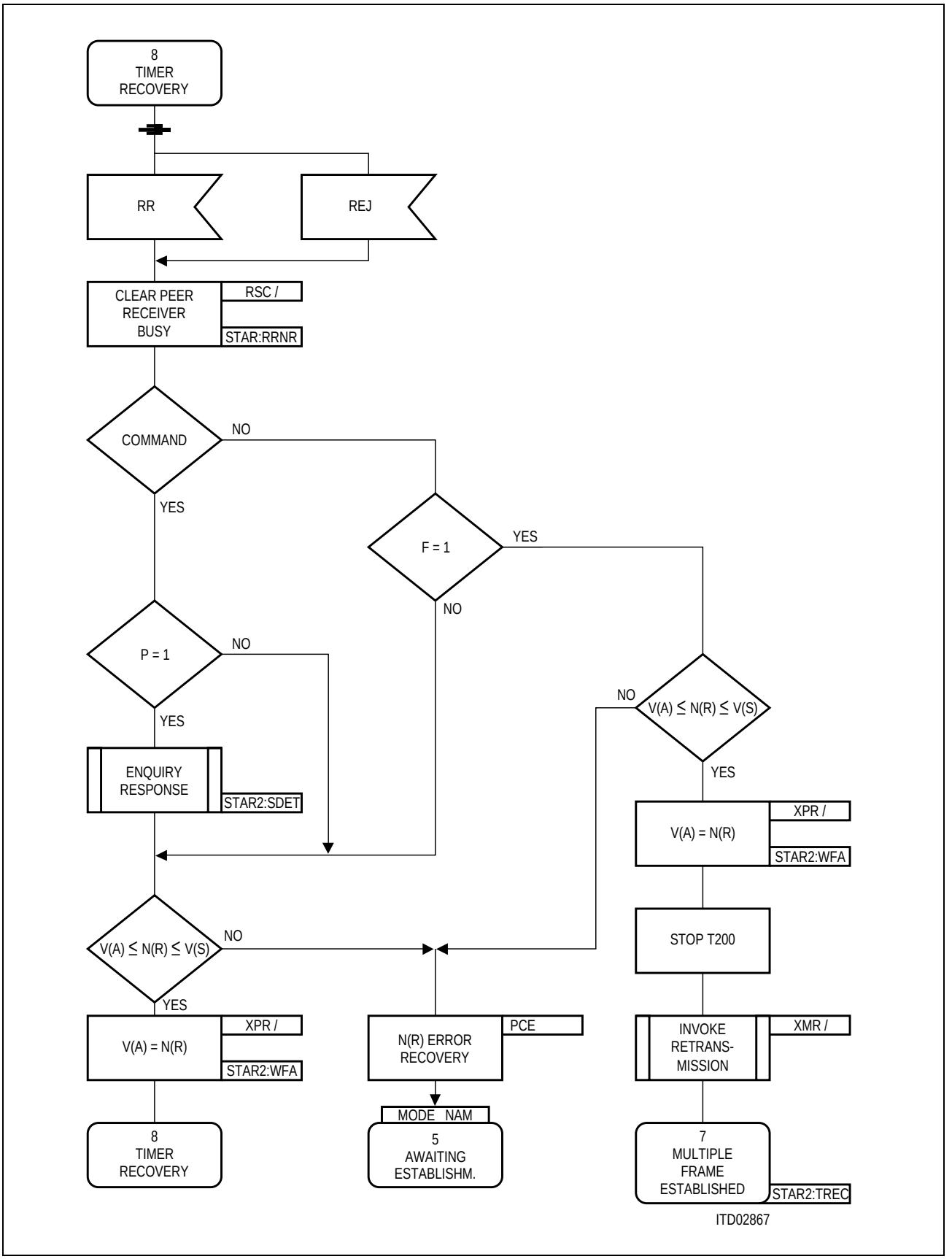

8
TIMER
RECOVERY
RR
REJ
CLEAR PEER
RECEIVER
BUSY
RSC /
STAR:RRNR
COMMAND
NO
YES
F = 1
YES
NO
P = 1
NO
YES
ENQUIRY
RESPONSE
STAR2:SDET
NO
V(A) ≤ N(R) ≤ V(S)
YES
V(A) = N(R)
XPR /
STAR2:WFA
STOP T200
V(A) ≤ N(R) ≤ V(S)
NO
YES
V(A) = N(R)
XPR /
STAR2:WFA
N(R) ERROR
RECOVERY
PCE
INVOKE
RETRANS-
MISSION
XMR /
MODE NAM
8
TIMER
RECOVERY
5
AWAITING
ESTABLISHM.
7
MULTIPLE
FRAME
ESTABLISHED
STAR2:TREC
ITD02867

Figure 28e

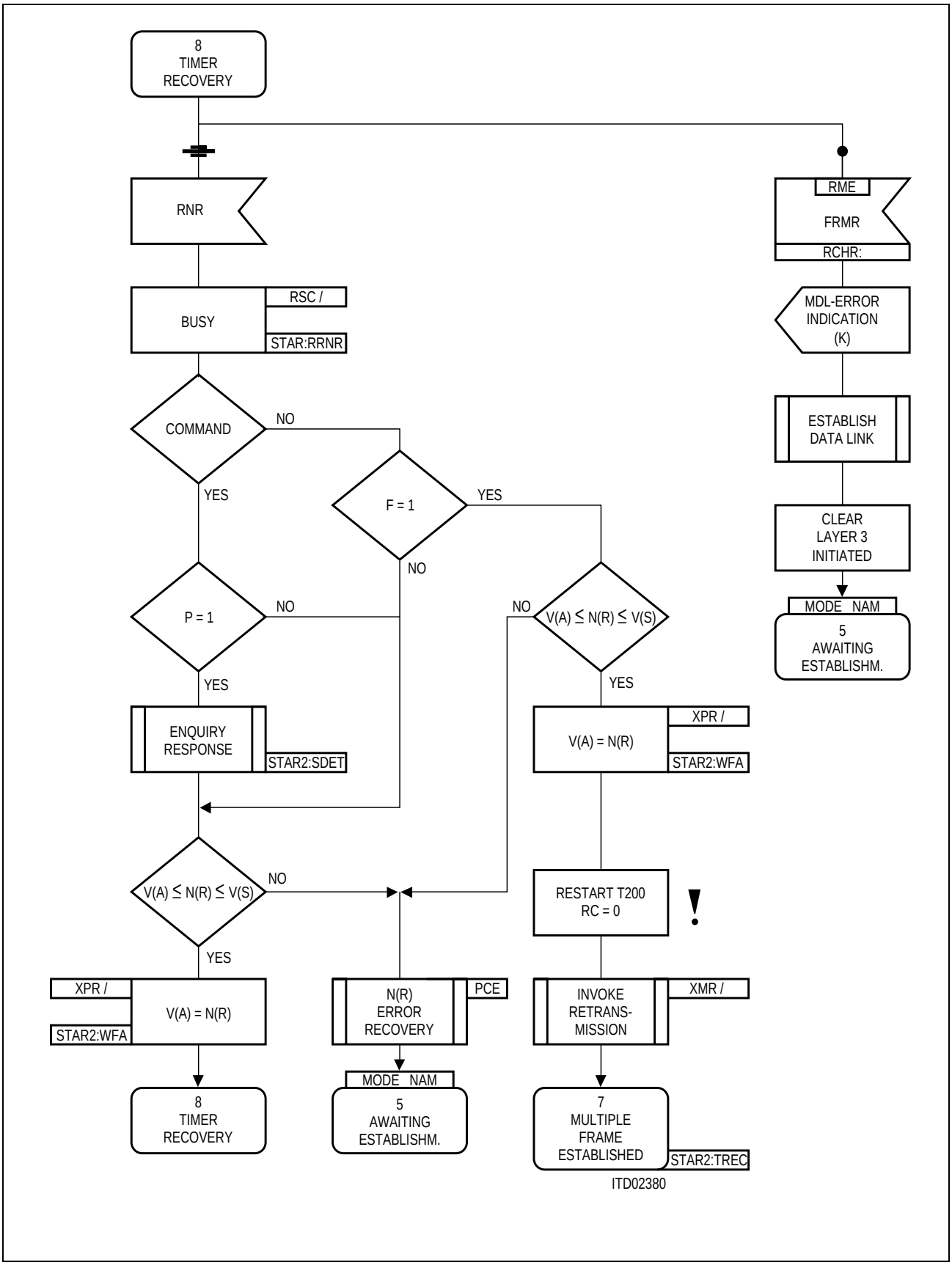

8
TIMER
RECOVERY
RNR
BUSY
RSC /
STAR:RRNR
COMMAND
NO
YES
P = 1
NO
YES
ENQUIRY
RESPONSE
STAR2:SDET
F = 1
YES
NO
V(A) ≤ N(R) ≤ V(S)
NO
YES
V(A) = N(R)
XPR /
STAR2:WFA
RESTART T200
RC = 0
!
INVOKE
RETRANS-
MISSION
XMR /
7
MULTIPLE
FRAME
ESTABLISHED
STAR2:TREC
V(A) ≤ N(R) ≤ V(S)
NO
YES
XPR /
V(A) = N(R)
STAR2:WFA
8
TIMER
RECOVERY
N(R)
ERROR
RECOVERY
PCE
MODE NAM
5
AWAITING
ESTABLISHM.
RME
FRMR
RCHR:
MDL-ERROR
INDICATION
(K)
ESTABLISH
DATA LINK
CLEAR
LAYER 3
INITIATED
MODE NAM
5
AWAITING
ESTABLISHM.
ITD02380

Figure 28f

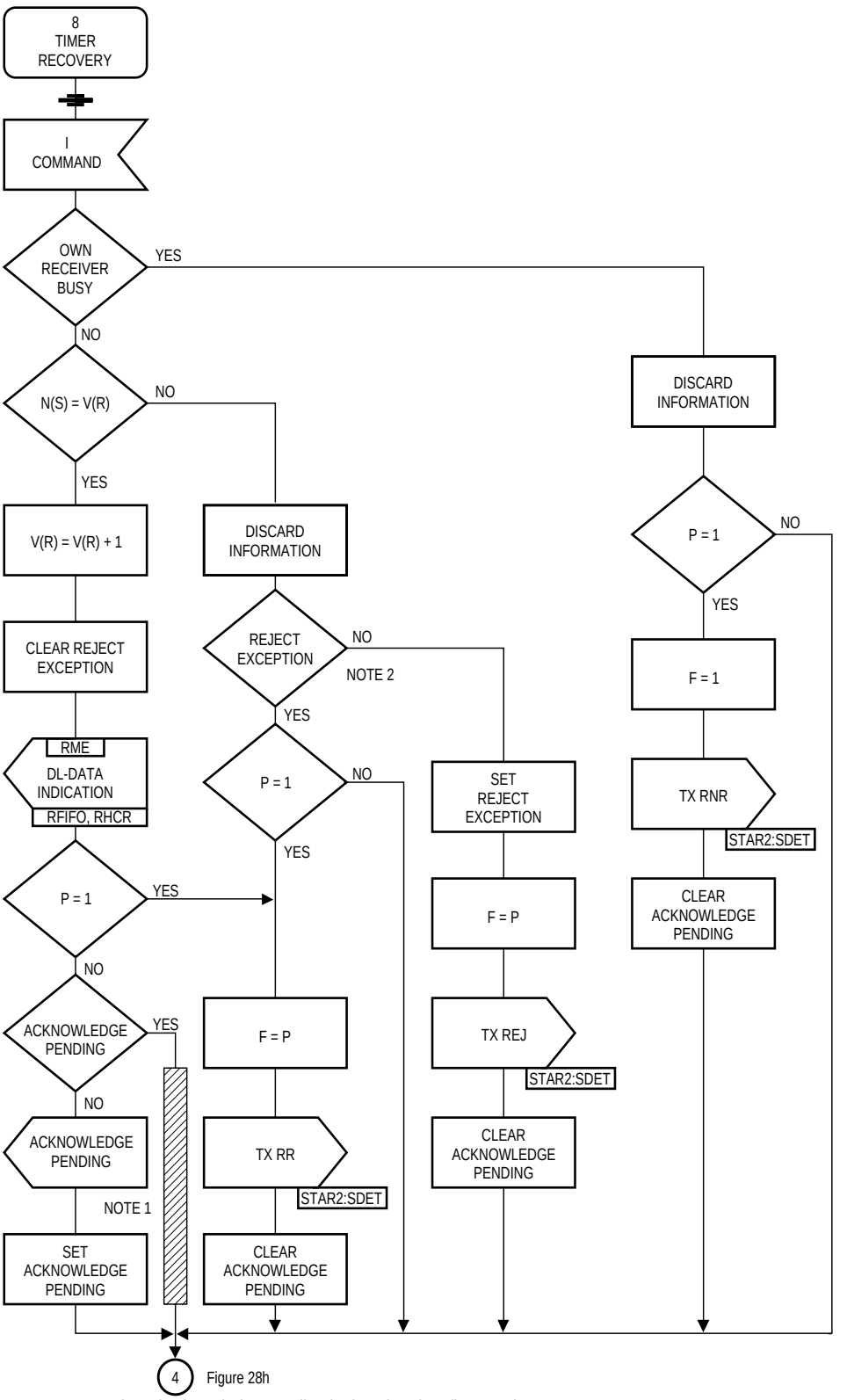

8
TIMER
RECOVERY
I
COMMAND
OWN
RECEIVER
BUSY
YES
NO
N(S) = V(R)
NO
YES
V(R) = V(R) + 1
CLEAR REJECT
EXCEPTION
RME
DL-DATA
INDICATION
RFIFO, RHCR
P = 1
YES
NO
ACKNOWLEDGE
PENDING
YES
NO
ACKNOWLEDGE
PENDING
NOTE 1
SET
ACKNOWLEDGE
PENDING
DISCARD
INFORMATION
REJECT
EXCEPTION
NO
NOTE 2
YES
P = 1
NO
YES
F = P
TX RR
STAR2:SDET
CLEAR
ACKNOWLEDGE
PENDING
SET
REJECT
EXCEPTION
F = P
TX REJ
STAR2:SDET
CLEAR
ACKNOWLEDGE
PENDING
DISCARD
INFORMATION
P = 1
NO
YES
F = 1
TX RNR
STAR2:SDET
CLEAR
ACKNOWLEDGE
PENDING
4
Figure 28h
Note 1: Processing of acknowledge pending is descripted on figure 28i .
Note 2: This SDL-representation does not include the optional procedure in Appendix I.
ITD05647

Figure 28g

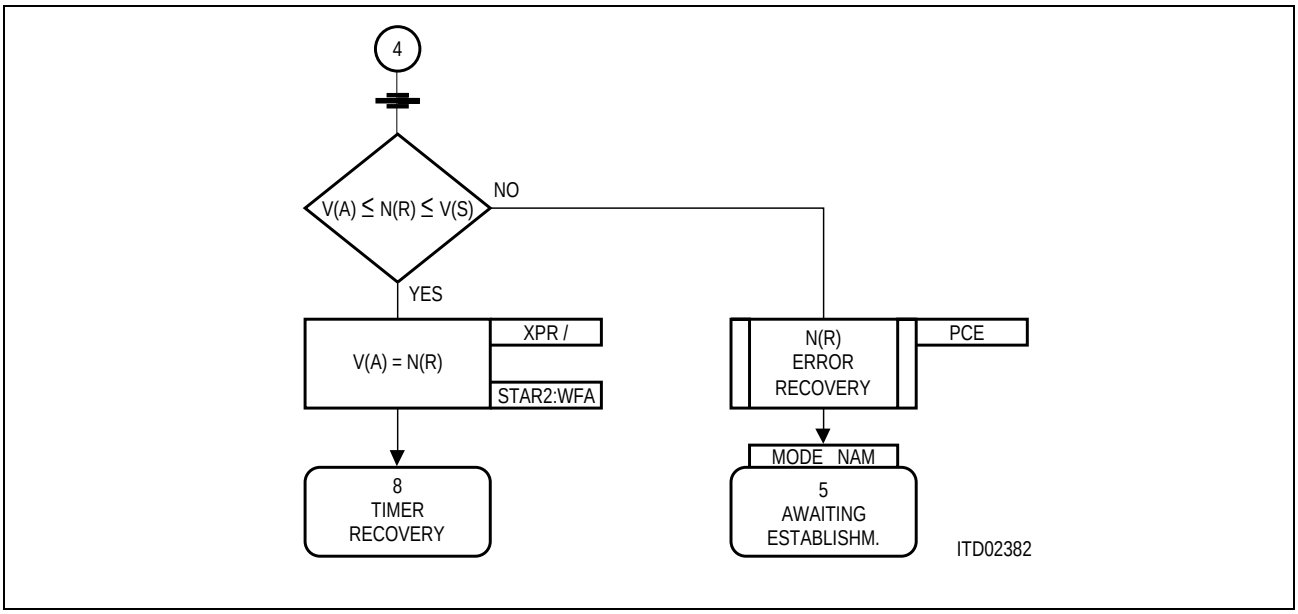


Figure 28h

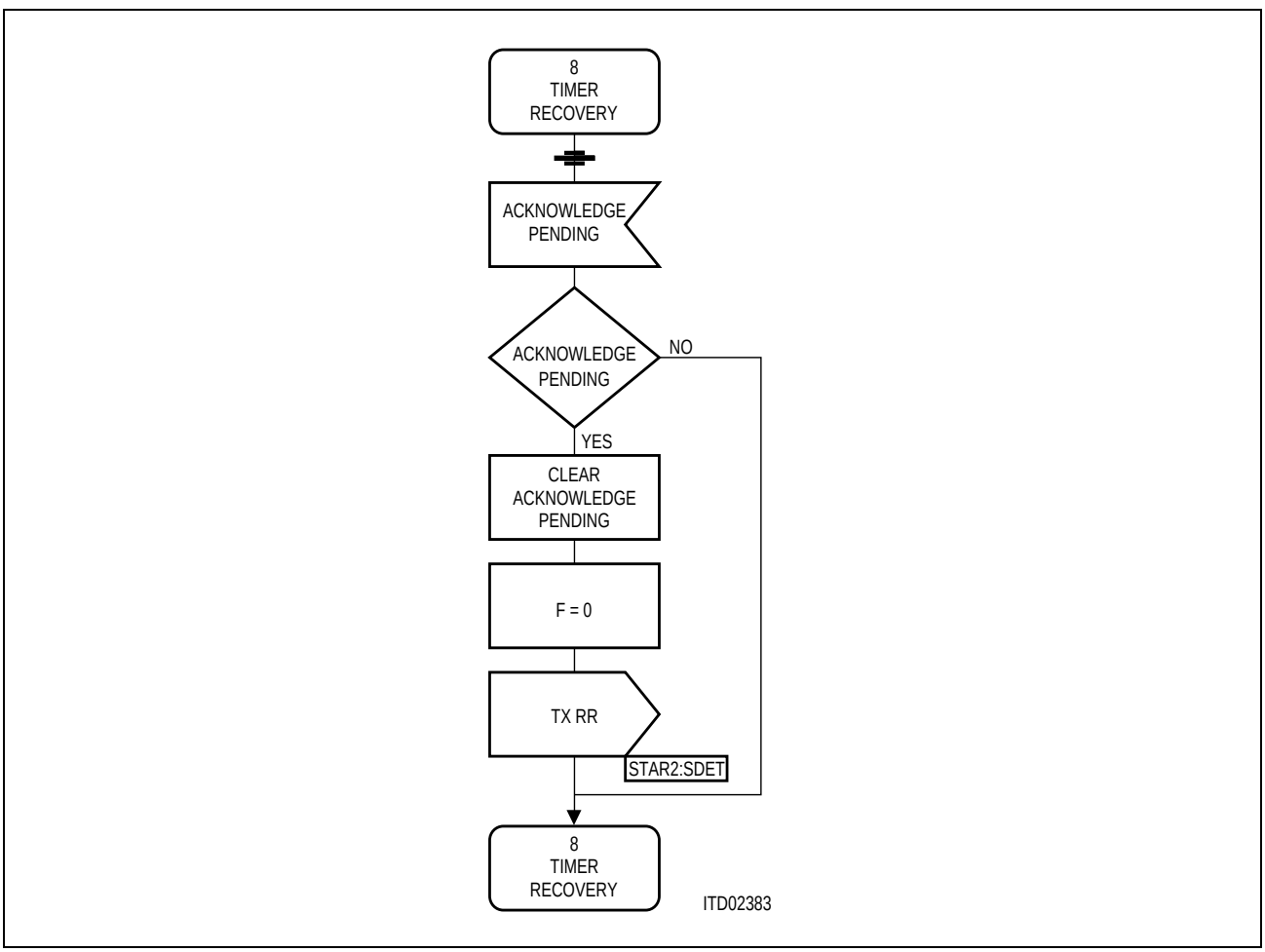
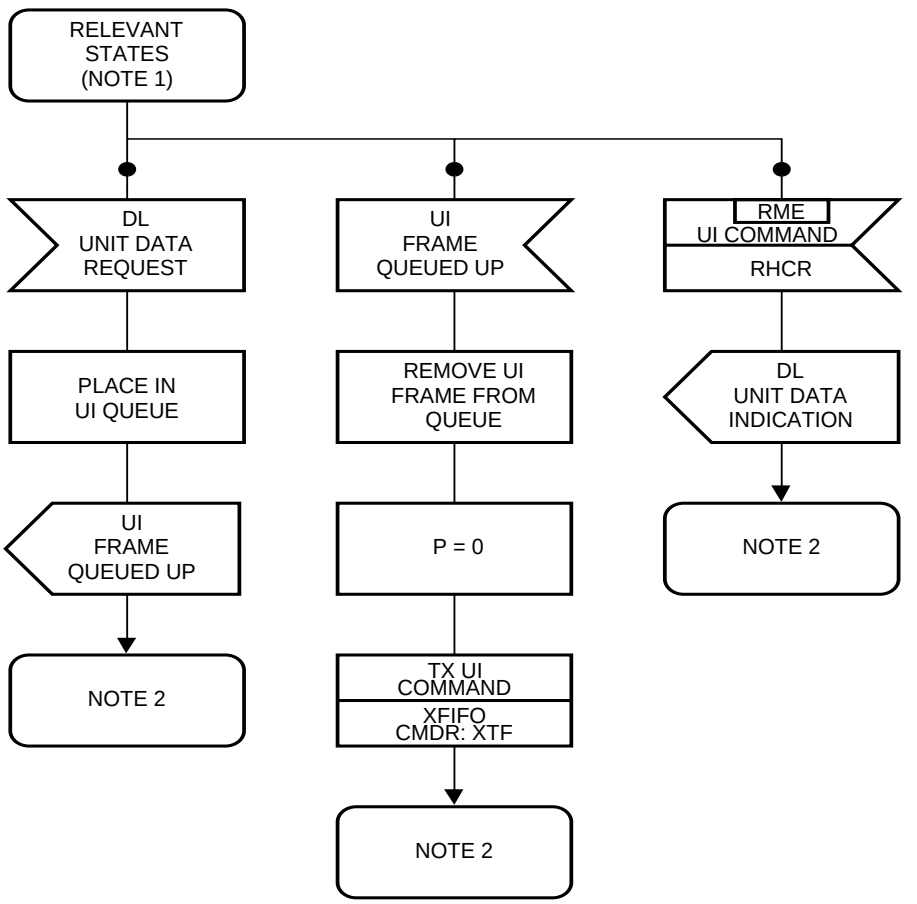


Figure 28i



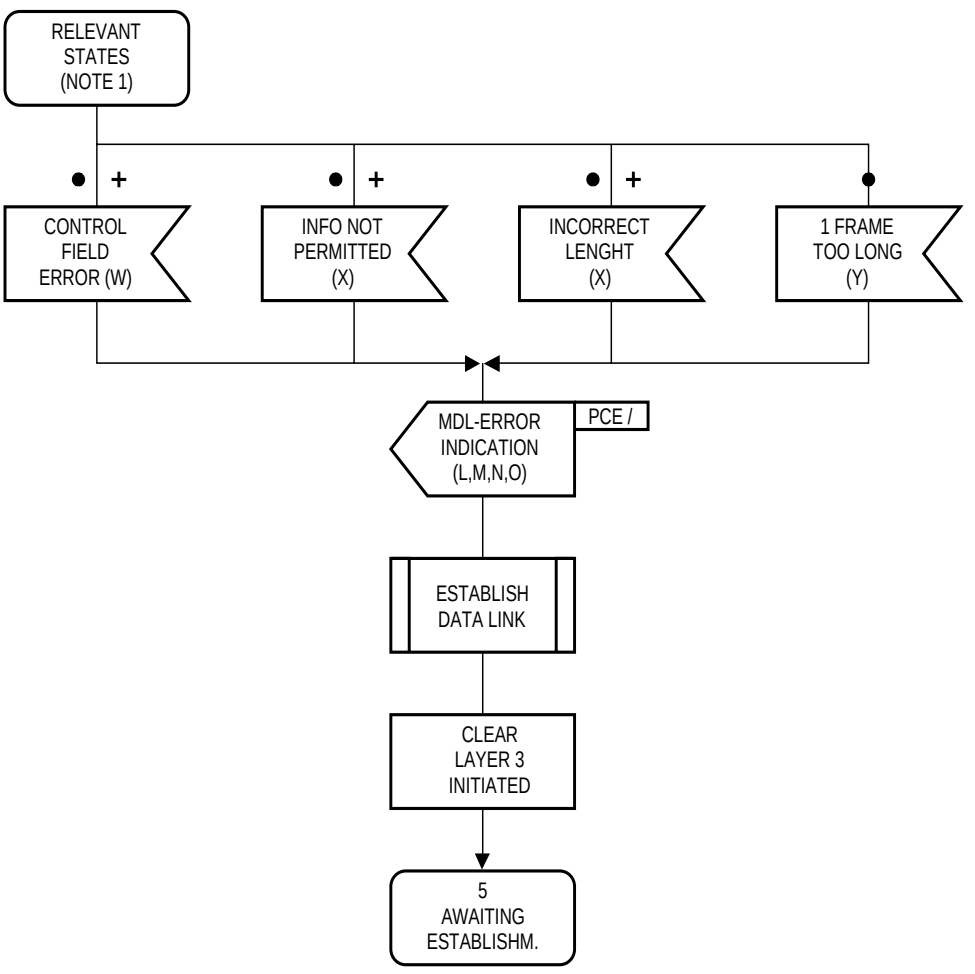
Note 1: The relevant states are as follows

4 TEI-assigned
5 Awaiting-establishement
6 Awaiting-release
7 Multiple-frame-established
8 Timer-recovery

Note 2: The data link layer returns to the state it was in prior to the events shown.

ITD02384

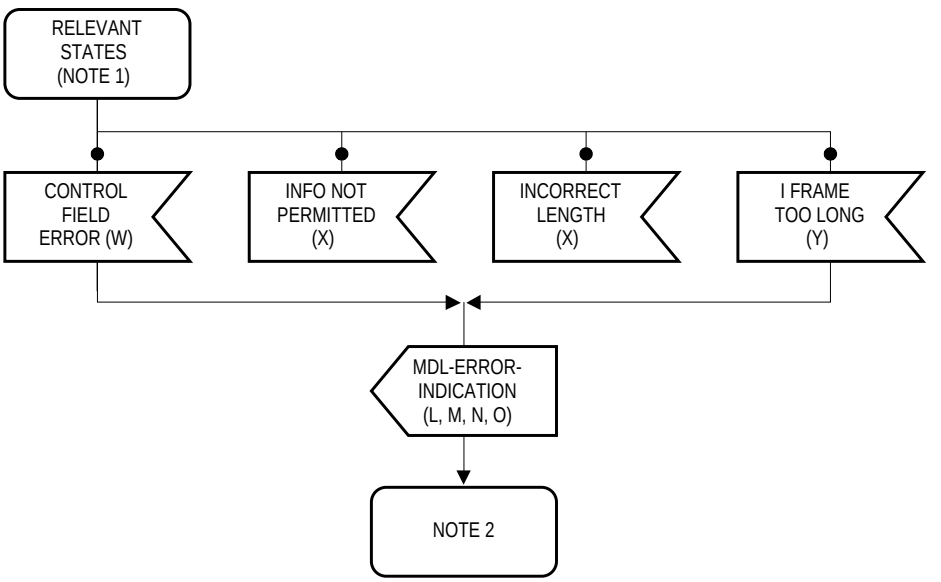
Figure 29a



Note 1: The relevant states are as follows
7 Multiple-frame-established
8 Timer-recovery

ITD02385

Figure 29b



Note 1: The relevant states are as follows:
4 TEI-assigned
5 Awaiting-establishment
6 Awaiting-release

Note 2: The data link layer returns to the state it was in prior to the events shown

ITD02577

Figure 29c

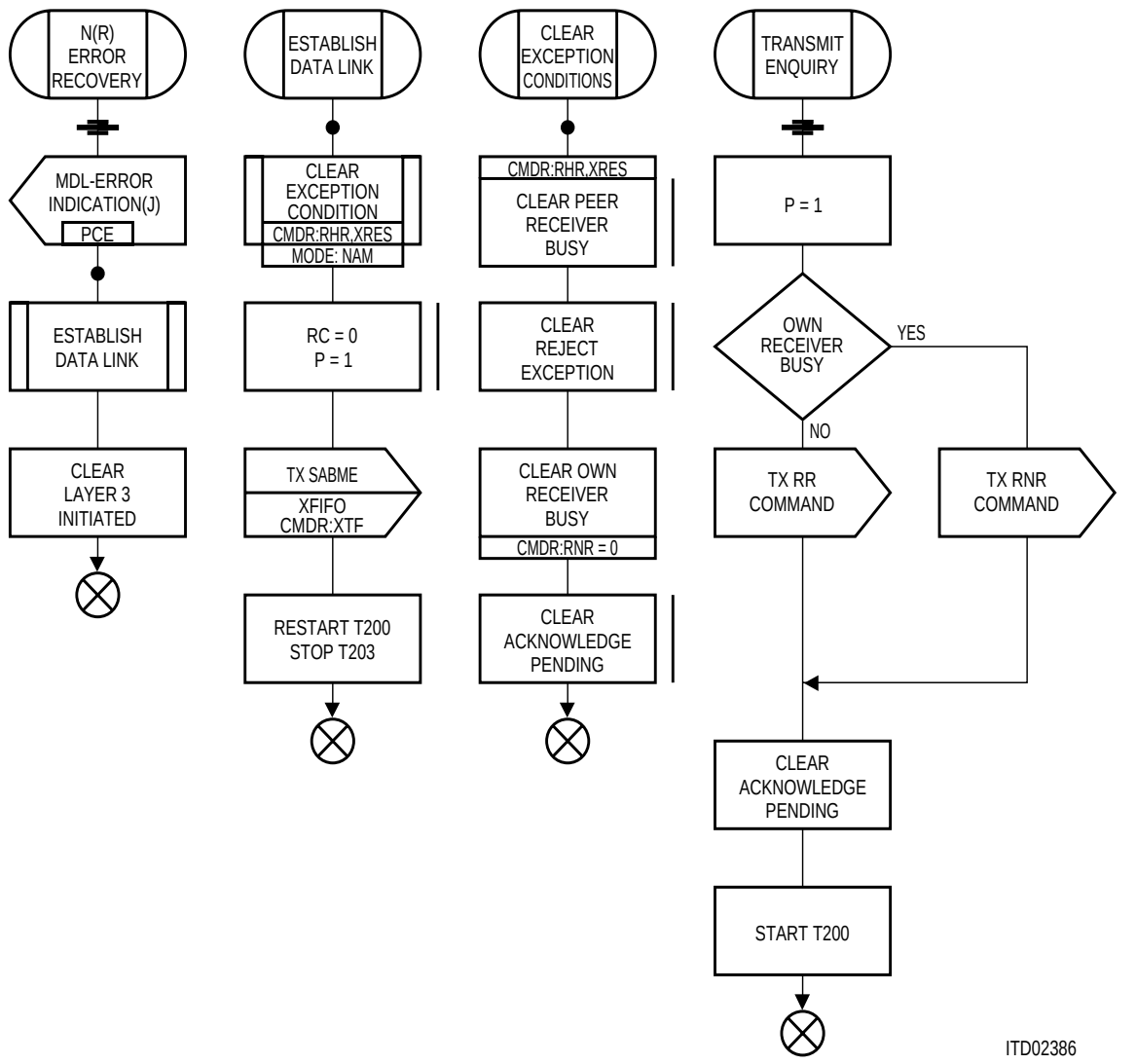
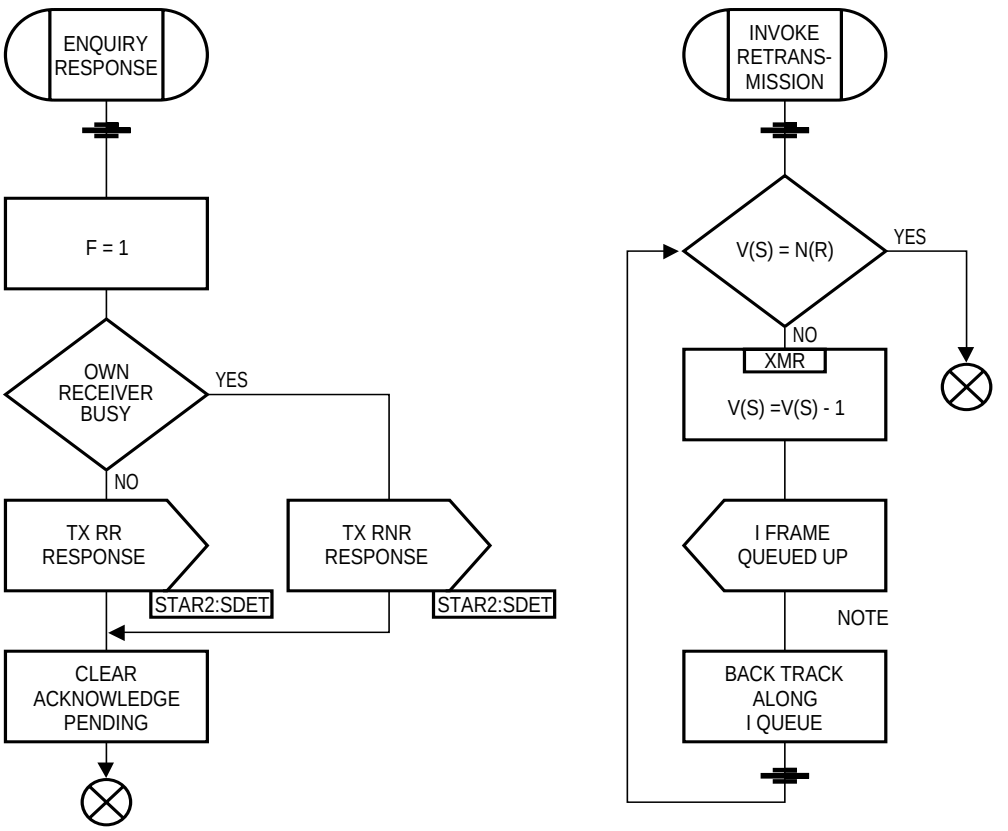

N(R)
ERROR
RECOVERY
MDL-ERROR
INDICATION(J)
PCE
ESTABLISH
DATA LINK
CLEAR
LAYER 3
INITIATED
ESTABLISH
DATA LINK
CLEAR
EXCEPTION
CONDITION
CMDR:RHR,XRES
MODE: NAM
RC = 0
P = 1
TX SABME
XFIFO
CMDR:XTF
RESTART T200
STOP T203
CLEAR
EXCEPTION
CONDITIONS
CMDR:RHR,XRES
CLEAR PEER
RECEIVER
BUSY
CLEAR
REJECT
EXCEPTION
CLEAR OWN
RECEIVER
BUSY
CMDR:RNR = 0
CLEAR
ACKNOWLEDGE
PENDING
TRANSMIT
ENQUIRY
P = 1
OWN
RECEIVER
BUSY
YES
NO
TX RR
COMMAND
TX RNR
COMMAND
CLEAR
ACKNOWLEDGE
PENDING
START T200
ITD02386

Figure 29d



Note: The generation of the correct number of signals in order to cause the required retransmission of I frames does not alter their sequence integrity.

ITD02387

Figure 29e

2.1.7 Terminal Specific Functions

2.1.7.1 LED-Interface

The LED-interface of the PSB 2196 ISAC-P TE provides the control of a LED-matrix up to 16 LED's. The matrix consists of four lines by four columns (**figure 30**). The LED interface includes the timing control to multiplex the line information for each column. The line drivers are turned on and off with a delay to reduce the power consumption while switching.

Each line output driver is able to drive 12 mA with a minimum output voltage of V_{DD} – 1 V.

The LED-interface may be configured to support a 6 × 4 LED matrix. Therefore, the outputs C3 and C4 are used to provide the line information for line 5 and 6. An external transistor is necessary to provide the current of 12 mA. The column outputs C1 and C2 are connected to an external 2:4 decoder which provides the information for the column drivers. The selection between both configurations is done via the GCR:LEM-bit.

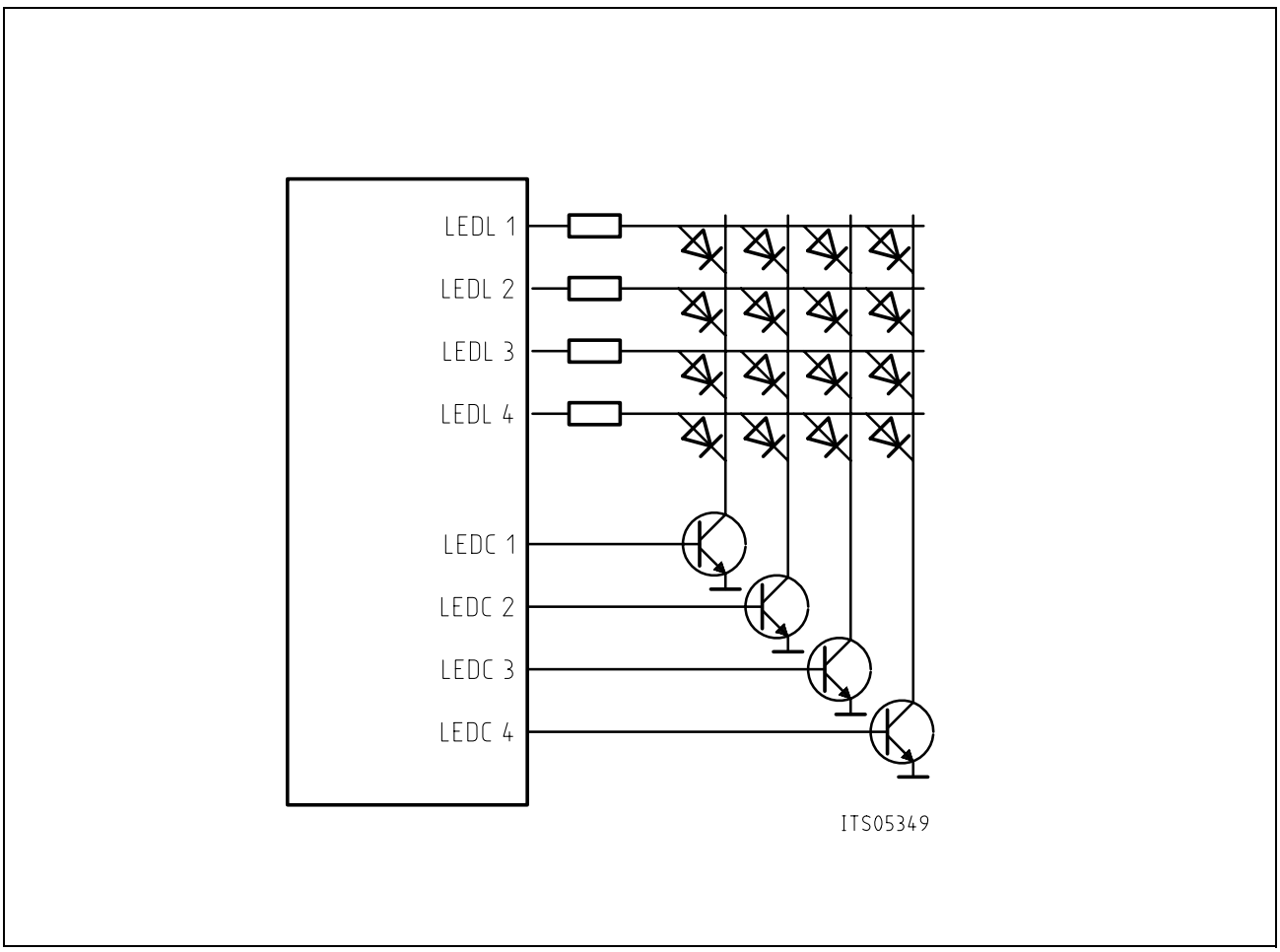


Figure 30
LED-Matrix Control (4 × 4)

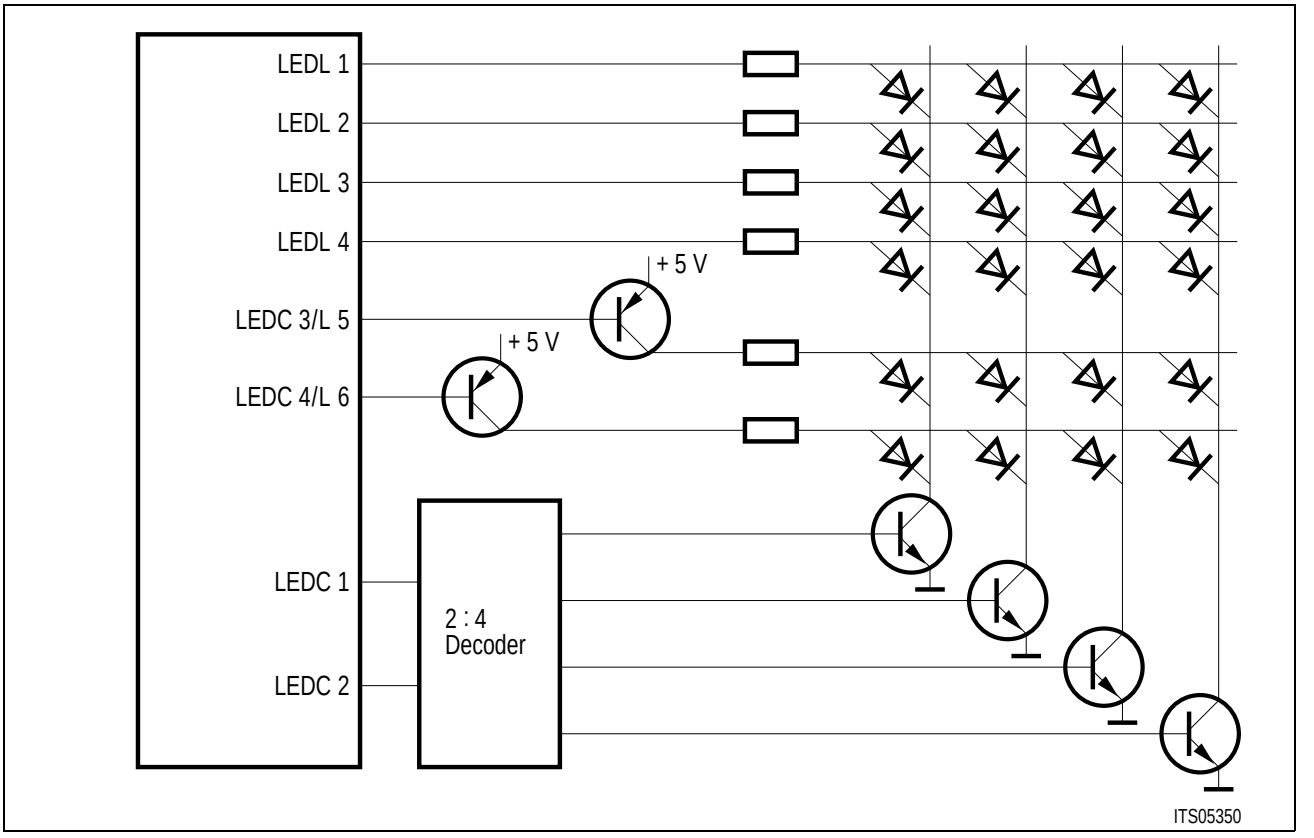


Figure 31
LED-Matrix Control (6 × 4)

The timing of the LED-interface is shown in **figure 32**. Each line is turned on and off with an offset of 130 ns in regard to the previous line. The line driver is active for a period of 2.13 ms.

The column driver is turned off 130 ns after the last line has been turned off.

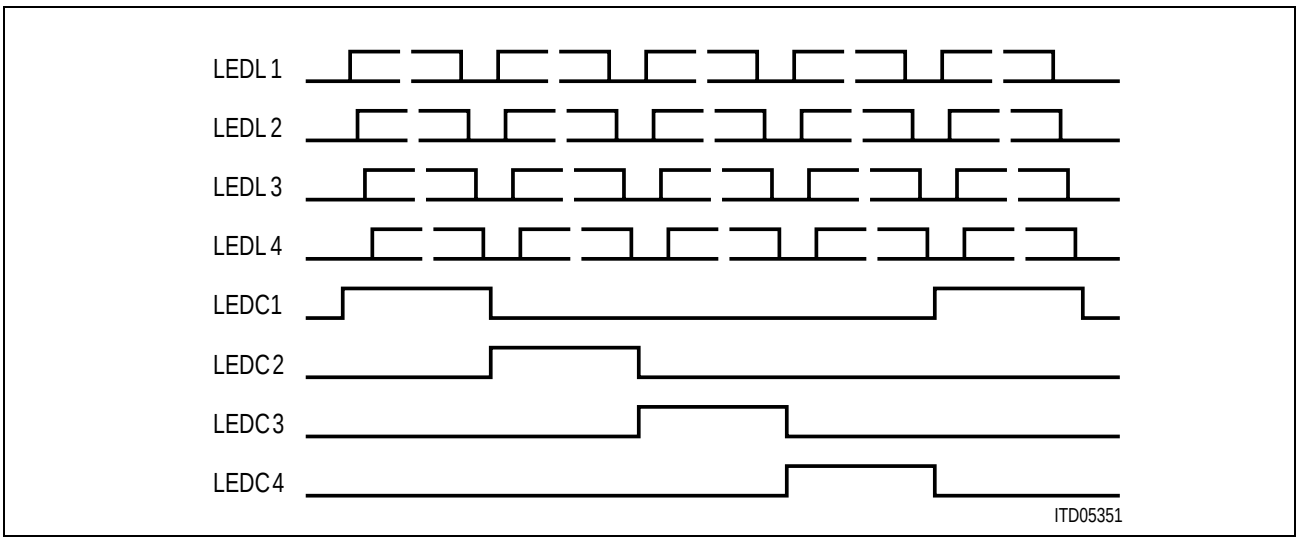


Figure 32
LED-Interface Timing (4 × 4)

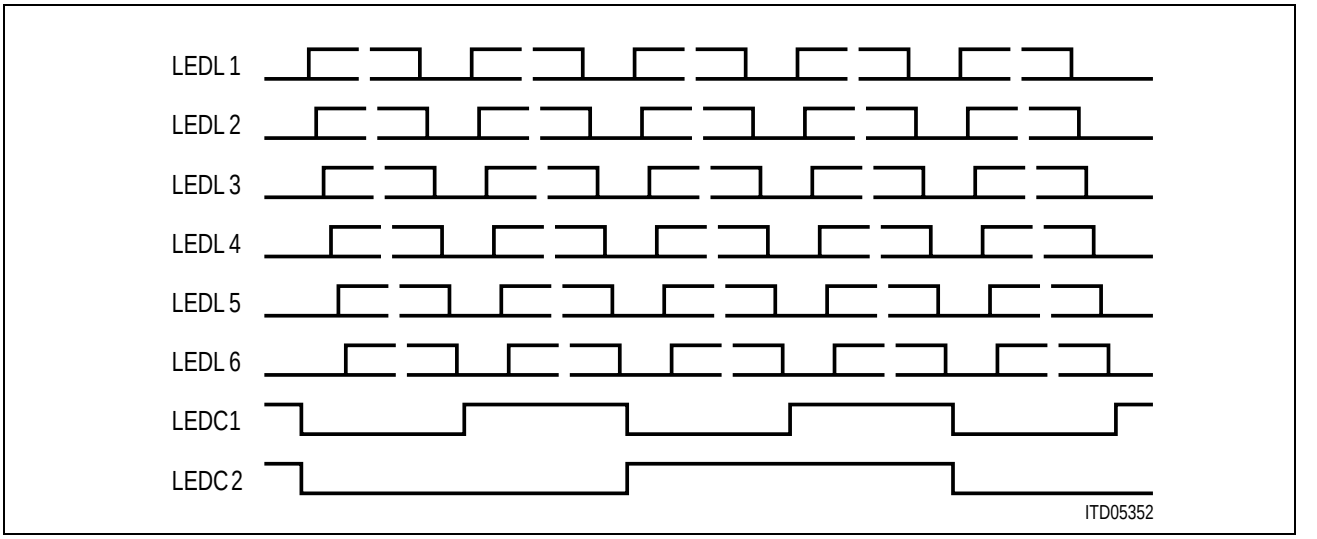


Figure 33
LED-Interface Timing (6 × 4)

2.1.7.2 LCD-Contrast Control

The LCD-contrast control output provides a pulse width modulated signal which can be varied in 14 linear steps between OFF and ON. The repetition frequency is 8.98 kHz. The output of the PWM is filtered by a low pass filter and transformed to the required voltage range by an external transistor as shown in **figure 34**.

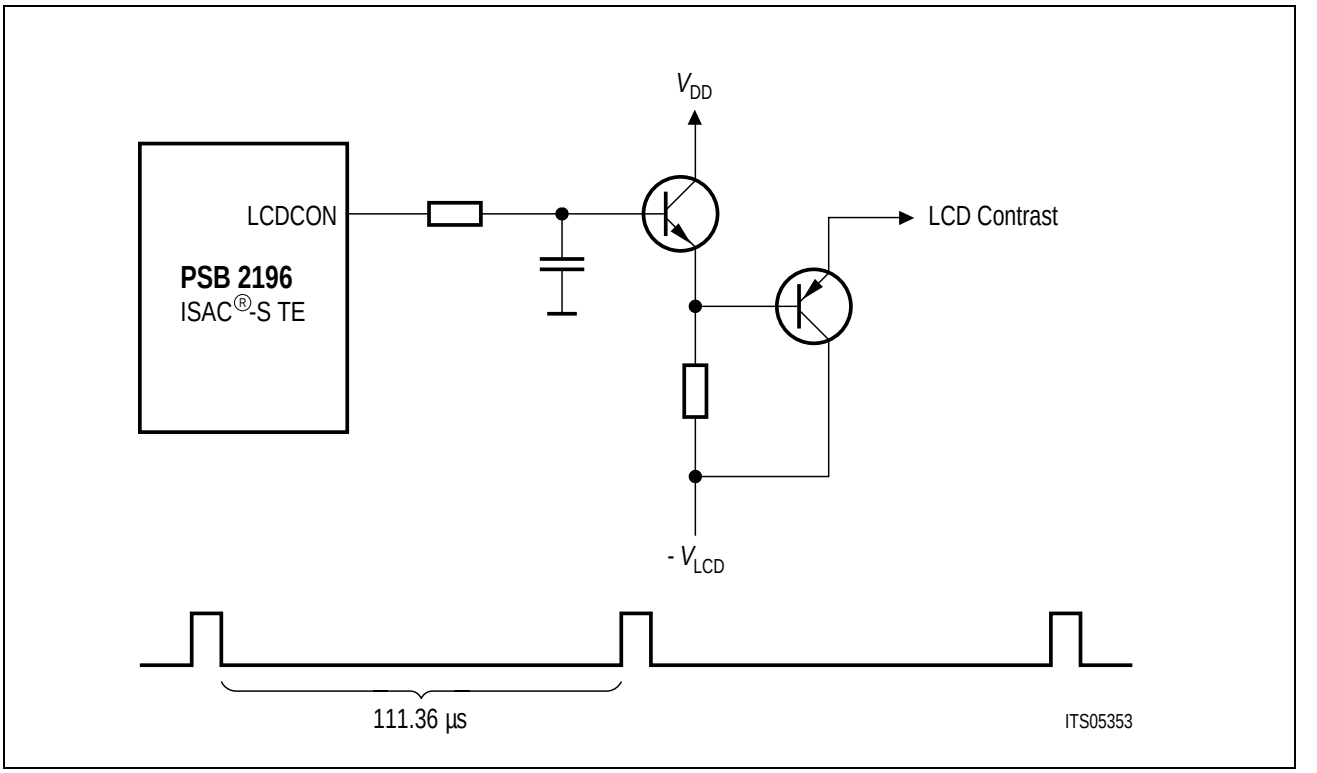


Figure 34
LCD-Contrast Control

2.2 Terminal Repeater (TR) Mode

2.2.1 General Functions and Device Architecture (TR-mode)

In TR-mode the following functions are provided:

- U_{PN}-interface transceiver, functionally fully compatible to both PEB 2095 IBC and PEB 2096 OCTAT-P, also features the terminal repeater mode
- IOM-2 interface for terminal application

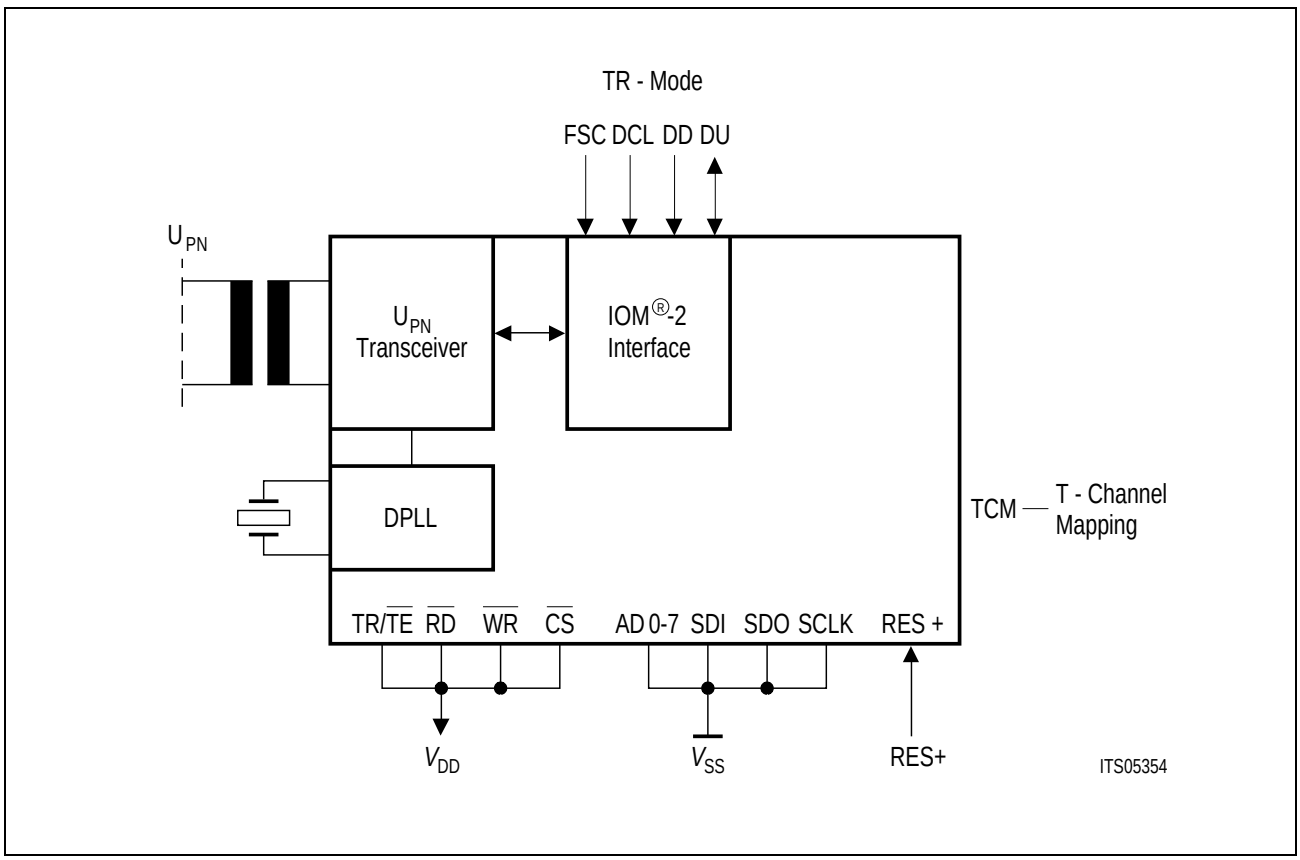


Figure 35
Device Architecture in TR-Mode

2.2.2 Clock Generation (TR-mode)

In TR-mode, the oscillator is used to generate a 15.36-MHz clock signal. This signal is used by the DPLL to synchronize U_{PN}-frames to the received IOM-2 clocks (FSC, DCL). No other clocks are generated.

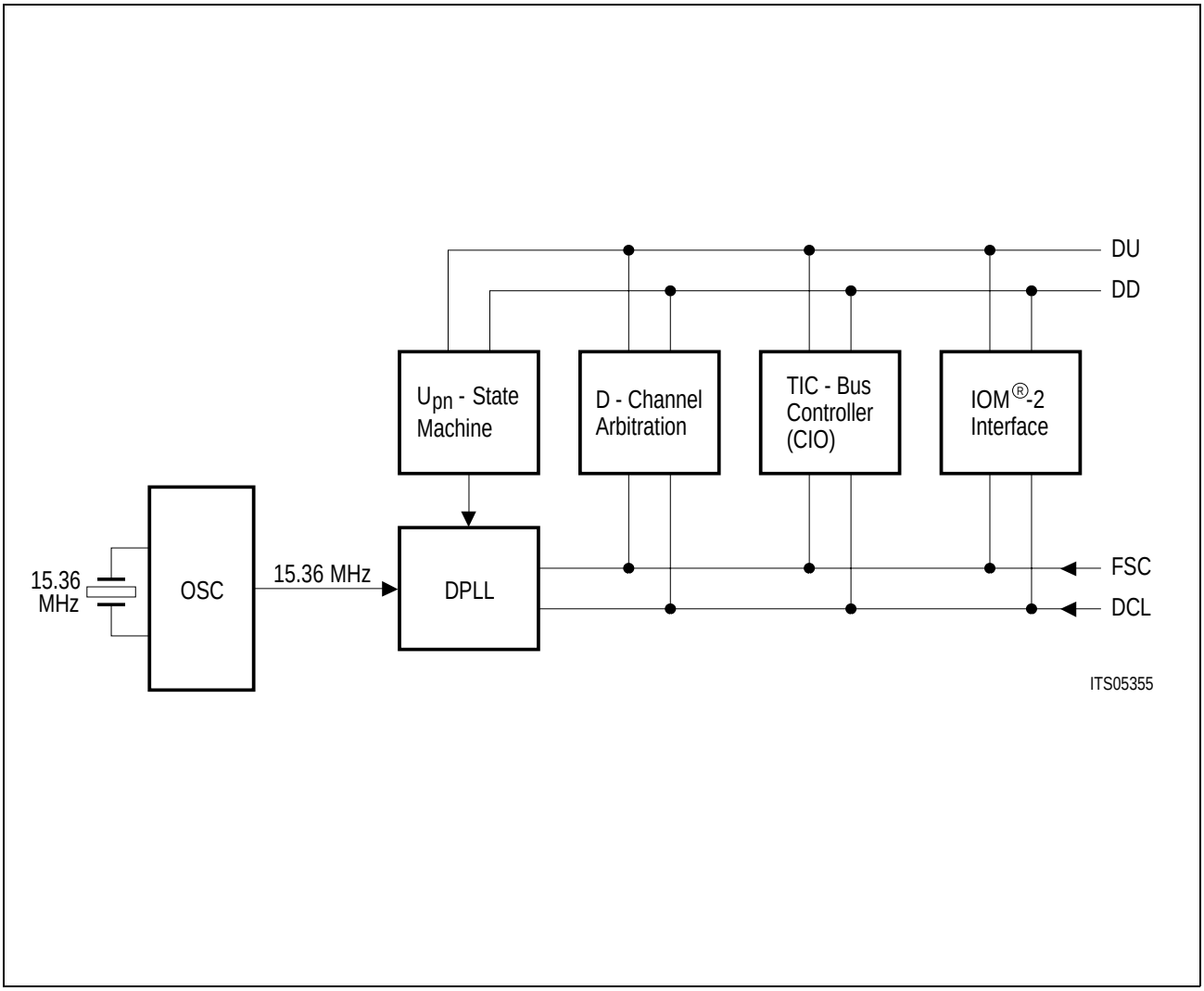


Figure 36
Clock Generation in TR-Mode

2.2.3 Interfaces (TR-mode)

In TR-mode, two interfaces are active:

- IOM-2 interface: as a universal backplane for terminals
- U_{PN}-interface towards the two-wire slave subscriber line

2.2.3.1 IOM®-2 Interface in TR-Mode

The ISAC-P TE supports the IOM-2 terminal mode. The interface consists of four lines: FSC, DCL, DD and DU. FSC and DCL provide the clock inputs to synchronize the U_{PN}-transceiver to the IOM-2 interface. DU has an open drain output, DD serves as input only.

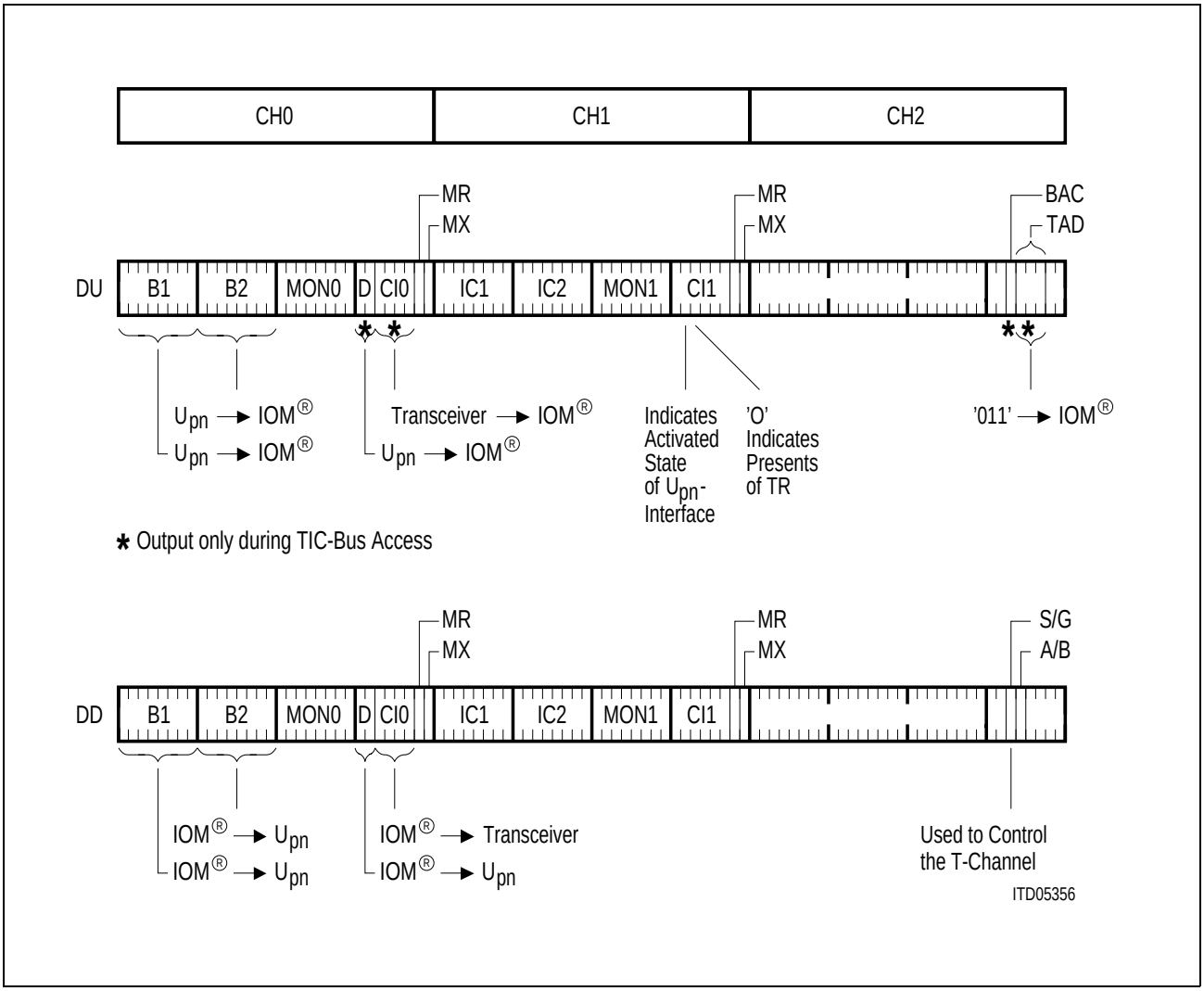


Figure 37
IOM®-2 Frame Structure in TR-Mode

The ISAC-P TE transfers the B-channel information between the IOM-2 and the U_{PN}-interface during the activated state. During all other states, “FF” is output. The C/I0-channel as well as the upstream D-bits are occupied by the TR ISAC-P TE after a TIC-bus access has been performed. The BAC- and TAD-bits are used for the TIC-bus access.

Bit 6 of the upstream CI1-channel is controlled by the ISAC-P TE in TR-mode. It is set to “0” if the U_{PN}-interface is in the activated state. Otherwise, the bit remains “1”.

The mapping of the downstream T-channel depends on the setting of TCM. If TCM = “0”, the T-channel transmits the value of the S/G-bit. If TCM = “1”, the T-channel is permanently set to “1”.

2.2.3.2 U_{PN}-Interface in TR-Mode

U_{PN}-Transceiver

The transmitter uses the received FSC-signal to start the generation of a U_{PN} -frame. If a short FSC-length (1 × DCL) is detected, the superframe counter is reset and the next U_{PN}-frame will transmit the CV in the M-bit. During normal length of the FSC-signal (64 DCL clocks), the superframe counter counts continuously.

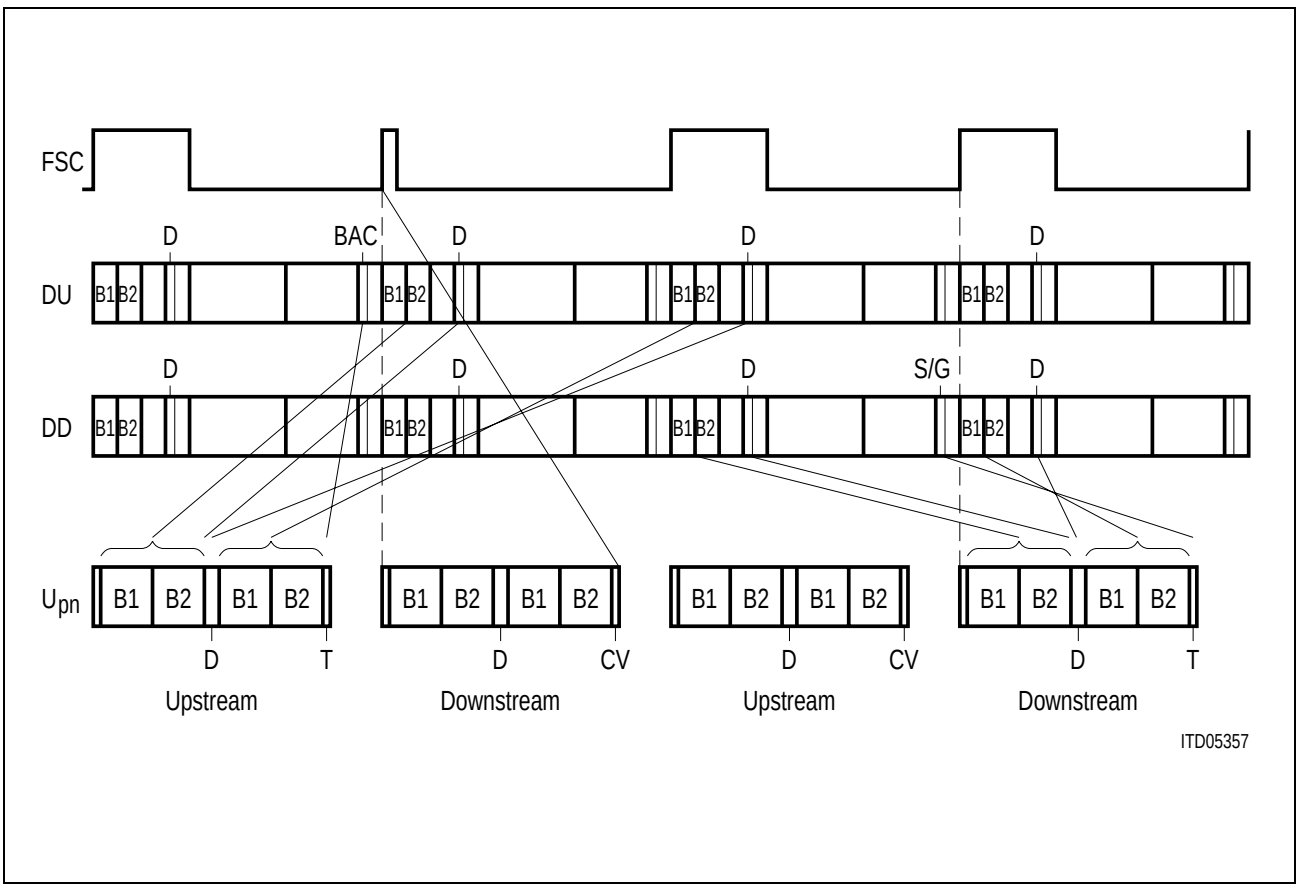


Figure 38
U_{PN}-Transceiver Timing

Control of the U_{PN}-Transceiver

An incorporated finite state machine controls the activation/deactivation procedures and communications with the layer-2 section via the IOM-Command/Indicate (CI) channel 0.

In TR-mode, activation from the terminal side is started by a power up sequence in case the FSC- and DCL-clocks are turned off. After that, a TIC-bus access is performed and activation is started by outputting the C/I-code “AR”. After that, the U_{PN}-interface is activated and after completion of the procedure, the C/I-code “AI” is output.

2.2.4 D-Channel Arbitration in TR-Mode

The D-channel access in TR-mode depends on the T-channel information. If a “0” bit is detected in the received T-channel, a TIC-bus request is started.

The received D-bits from the U_{PN}-interface are output to the D-channel of the data upstream line as long as the TIC-bus is idle (BAC = 1 and TAD = 111) or as long as the TR ISAC-P TE occupies the TIC-bus.

The downstream T-channel transmits the state of the S/G-bit while the TIC-bus is idle (BAC = 1, TAD = 111) or the TR ISAC-P TE occupies the TIC-bus.

In case the TIC-bus is occupied by another D-channel controller (TAD < > “111” or BAC = “0”), only “11” is output to the DU-line independent of the received D-bit information of the U_{PN}-interface. At the same time, the downstream T-channel is set to “0” which indicates the blocked condition.

The TIC-bus address which is used by the ISAC-P TE in TR-mode is “011”.

2.2.5 Reset

In TR-mode, the undervoltage detection is not active. To reset the ISAC-P TE in TR-mode an external reset signal must be applied on the RES + input. The reset will deactivate the U_{PN}-transceiver and it will abort any TIC-bus access currently in progress. The TIC-bus returns to idle.

3 Operational Description

3.1 TE-Mode

3.1.1 Interrupt Structure and Logic

Since the ISAC-P TE provides only one interrupt request output ($\overline{INT}$), the cause of an interrupt is determined by the microprocessor by reading the Interrupt Status Register (ISTA). In this register, four interrupt sources can be read directly. The LSB of ISTA points to five non-critical interrupt sources which are indicated in the Extended Interrupt Register EXIR (**figure 39**).

Reading the ISTA-register clears all bits except EXI and CIC. Reading the EXIR-register clears the EXIR-register and the EXI-bit in the ISTA-register, CIC is cleared by reading the CIR0-register.

When all bits in ISTA are cleared, the interrupt line is deactivated.

Each interrupt source in ISTA can be selectively masked by setting the corresponding bit position in the MASK registers to “1”. Masked interrupt status bits are not indicated when the ISTA is read. Instead, they remain internally stored and pending until the mask bit is set to “0”. Reading the ISTA while a masked status bit is active has no effect on the pending interrupt.

In the event of an extended interrupt EXI is set even if the corresponding mask bit in MASK is active, but no interrupt is generated. In the event of a C/I-channel interrupt CIC is set, even when the corresponding mask bit in MASK is active, but no interrupt is generated.

MONITOR Channel Status Interrupt Logic

The MONITOR Data Receive (MDR) and the MONITOR End of Reception (MER) interrupt status bits have two enable bits, MONITOR Receive interrupt Enable (MRE) and MR-bit Control (MRC). The MONITOR channel Data Acknowledged (MDA) and MONITOR channel Data Abort (MAB) interrupt status bits have a common enable bit MONITOR interrupt Enable (MXE).

MRE prevents the occurrence of the MDR-status, including when the first byte of a packet is received. When MRE is active (1) but MRC is inactive, the MDR-interrupt status is generated only for the first byte of a receive packet. When both MRE and MRC are active, MDR is generated and all received monitor bytes – marked by a 1-to-0 transition in MX-bit – are stored. (Additionally, an active MRC enables the control of the MR-handshake bit according to the MONITOR channel protocol.)

Control of Edge-Triggered Interrupt Controllers

The $\overline{INT}$-output is level active. It stays active until all interrupt sources have been serviced. If a new status bit is set while an interrupt is serviced, the $\overline{INT}$-line stays active. This may cause problems if the ISAC-P TE is connected to edge-triggered interrupt controllers (**figure 40**).

To avoid these problems, it is recommended to mask all interrupts at the end of the interrupt service program and to enable the interrupts again. This is done by writing FF_H to the MASK register and to write back the old value of the MASK register (**figure 41**).

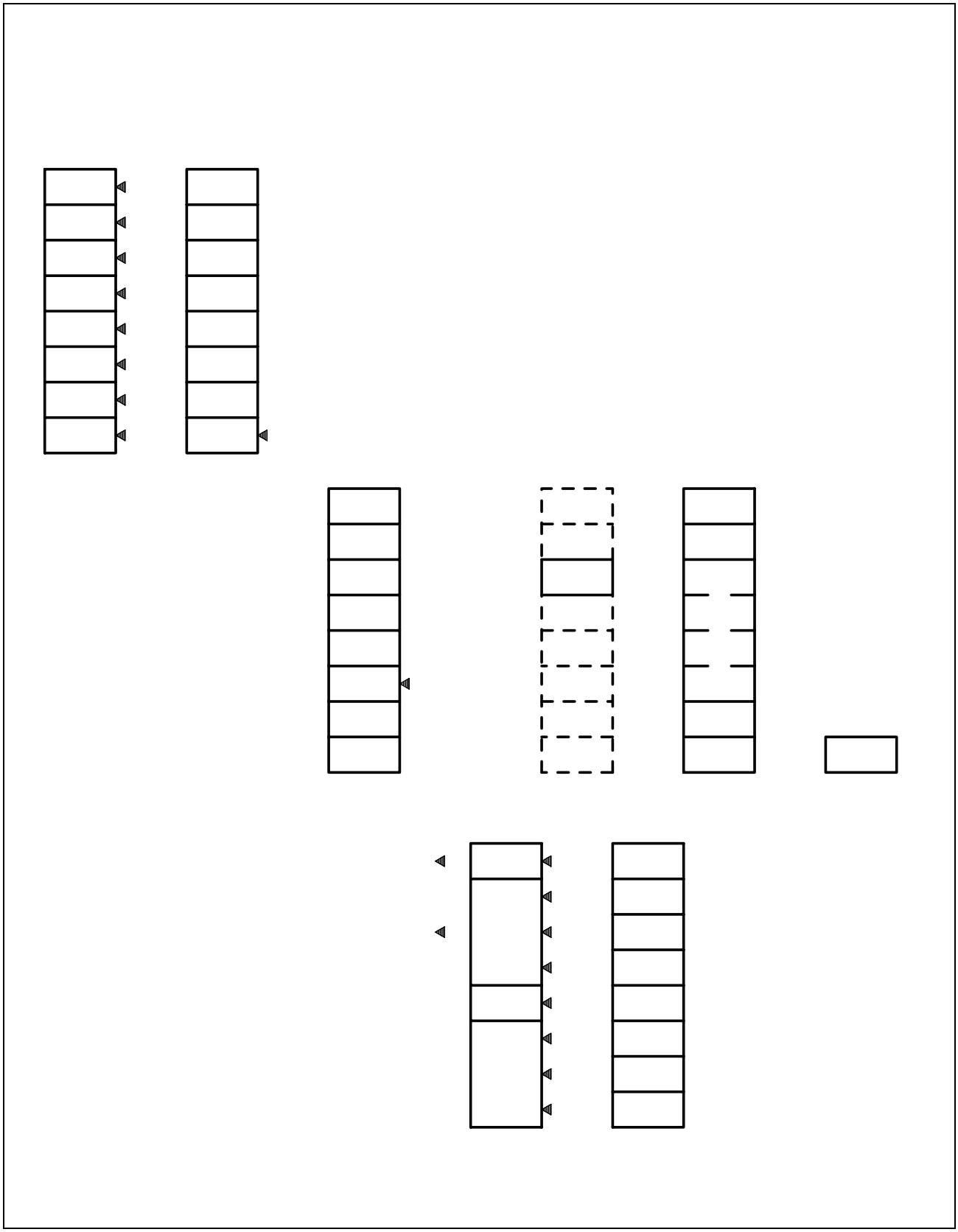
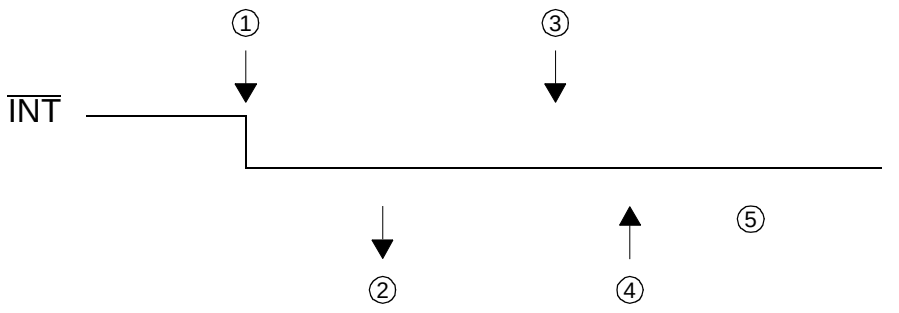


Figure 39
ISAC®-P TE Interrupt Structure



① A status bit is set. This causes an interrupt.

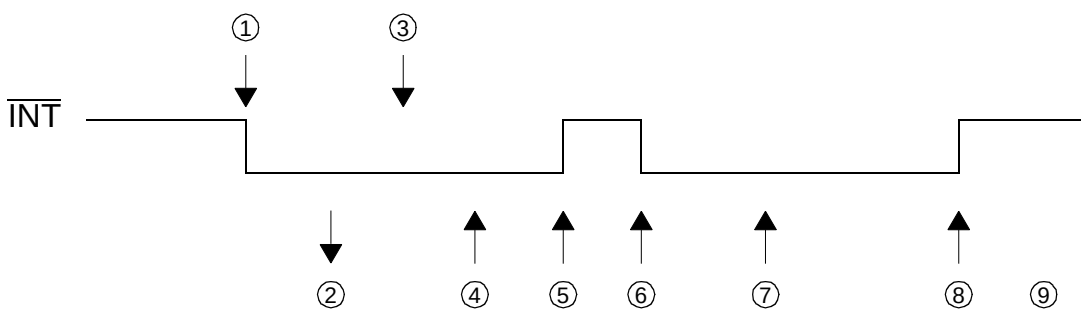
② The microprocessor starts its service routine and reads the status registers.

③ A new status bit is set before the first status bit has been read.

④ The first status bit is read.

⑤ The $\overline{INT}$-output stays active but the interrupt controller will not serve the interrupt (edge triggered).

Figure 40
$\overline{INT}$-Handling



① to ④ see above

⑤ "FF" is written to the MASK register. This masks all interrupts and returns the INT output to its inactive state.

⑥ The old value is written to the MASK register. This will activate the $\overline{INT}$-output if an interrupt source is still active.

⑦ The microprocessor starts a new interrupt service program.

⑧ The last status bit is read.

⑨ The $\overline{INT}$-output is inactive.

Figure 41
Service Program for Edge-Triggered Interrupt Controllers

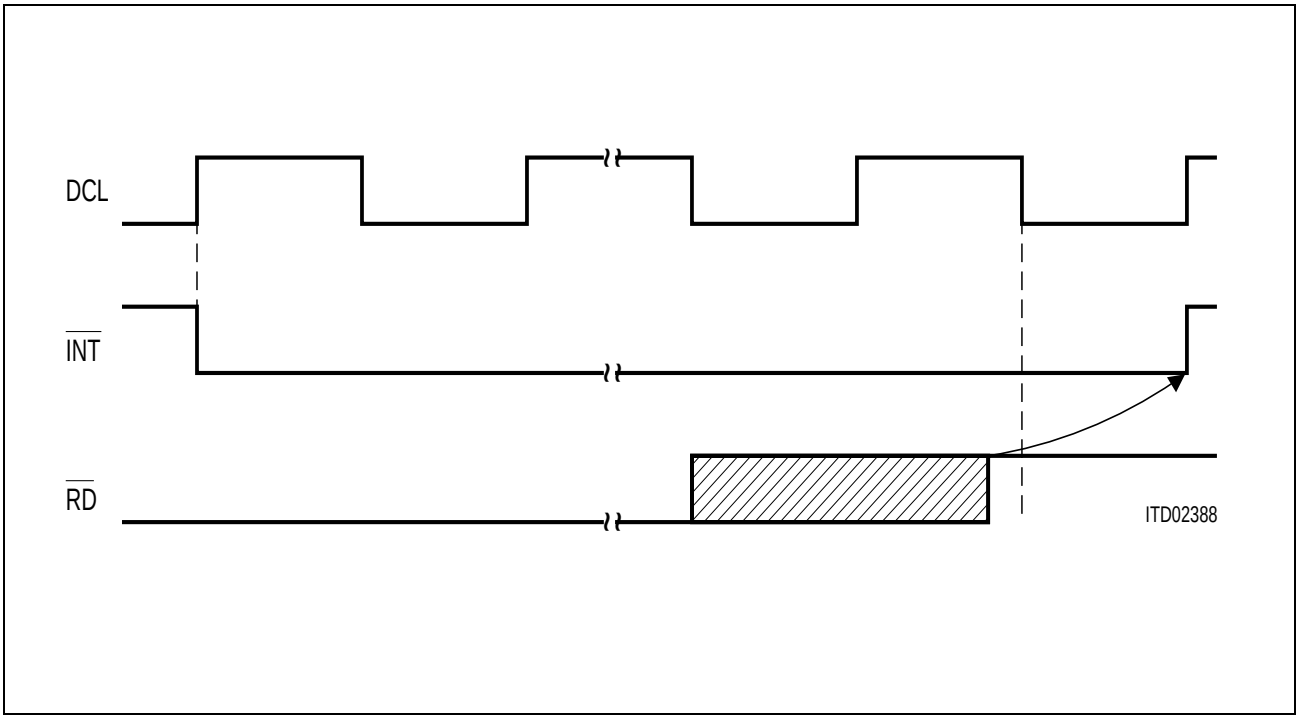


Figure 42
Timing of INT-Pin

The INT-line is switched with the rising edge of DCL. If no pending interrupts are internally stored, a reading of ISTA respectively EXIR or CIR0 switches the INT-line to high as indicated in **figure 42**.

Table 4
Interrupts from ICC HDLC-Controller

Mnemonic	Register	Meaning	Reaction
Layer-2 Receive			
RPF	ISTA	Receive Pool Full. Request to read received octets of an uncompleted HDLC-frame from RFIFO.	Read 32 octets from RFIFO and acknowledge with RMC.
RME	ISTA	Receive Message End. Request to read received octets of a complete HDLC-frame (or the last part of a frame) from RFIFO.	Read RFIFO (number of octets given by RBCL4-0) and status information and acknowledge with RMC.

Interrupts from ICC HDLC-Controller (cont'd)

Mnemonic	Register	Meaning	Reaction
Layer-2 Receive			
RFO	EXIR	Receive Frame Overflow. A complete frame has been lost because storage space in RFIFO was not available.	Error report for statistical purposes. Possible cause: deficiency in software.
PCE	EXIR	Protocol Error. S- or I-frame with incorrect N (R) or S-frame with I-field received (in auto-mode only).	Link re-establishment. Indication to layer 3.
Layer-2 Transmit			
XPR	ISTA	Transmit Pool Ready. Further octets of an HDLC-frame can be written to XFIFO. If XIFC was issued (auto mode), indicates that the message was successfully acknowledged with S-frame.	Write data bytes in the XFIFO if the frame currently being transmitted is not finished or a new frame is to be transmitted, and issue an XIF, XIFC, XTF or XTFC-command.
XMR	EXIR	Transmit Message Repeat. Frame must be repeated because of a transmission error (all HDLC-message transfer modes) or a received negative acknowledgement (auto-mode only) from peer station.	Transmission of the frame must be repeated. No indication to layer 3.
XDU	EXIR	Transmit Data Underrun. Frame has been aborted because the XFIFO holds no further data and XME (XIFC or XTFC) was not issued.	Transmission of the frame must be repeated. Possible cause: excessively long software reaction times.

Interrupts from ICC HDLC-Controller (cont'd)

Mnemonic	Register	Meaning	Reaction
Layer-2 Transmit			
RSC	ISTA	Receive Status Change. A status change from peer station has been received (RR- or RNR-frame), auto-mode only.	Stop sending new I-frames.
TIN	ISTA	Timer Interrupt. External timer expired or, in auto-mode, internal timer (T200) and repeat counter (N200) both expired.	Link re-established. Indication to layer 3. (Auto-mode)

Table 5
List of Commands

Command Mnemonic	HEX	Bit 7 … 0	Meaning
RMC	80	1000 0000	**Receive Message Complete.** Acknowledges a block (RPF) or a frame (RME) stored in the RFIFO.
RRES	40	0100 0000	**Reset HDLC-Receiver.** The RFIFIO is cleared. The transmit and receive counters (V(S), V(R)) are reset (auto-mode).
RNR	20	0010 0000	**Receiver Not Ready (auto-mode).** An I- or S-frame will be acknowledged with RNR-frame.
STI	10	0001 0000	**Start Timer.**
XTFC	0A	0000 1010	**Transmit Transparent Frame and Close.** Enables the "transparent" transmission of the block entered last in the XFIFO. The frame is closed with a CRC and a flag.
XIFC	06	0000 0110	**Transmit I-Frame and Close.** Enables the "auto-mode" transmission of the block entered last in the XFIFO. The frame is closed with a CRC and a flag.

List of Commands (cont'd)

Command Mnemonic	HEX	Bit 7 … 0	Meaning
XTF	08	0000 1000	**Transmit Transparent Frame.** Enables the "transparent" transmission of the block entered last in the XFIFO without closing the frame.
XIF	04	0000 0100	**Transmit I-Frame.** Enables the "auto-mode" transmission of the block entered last in the XFIFO without closing the frame.
XRES	01	0000 0001	**Reset HDLC-Transmitter.** The XFIFO is cleared.

3.1.2 Control of the U_{PN}-Transceiver

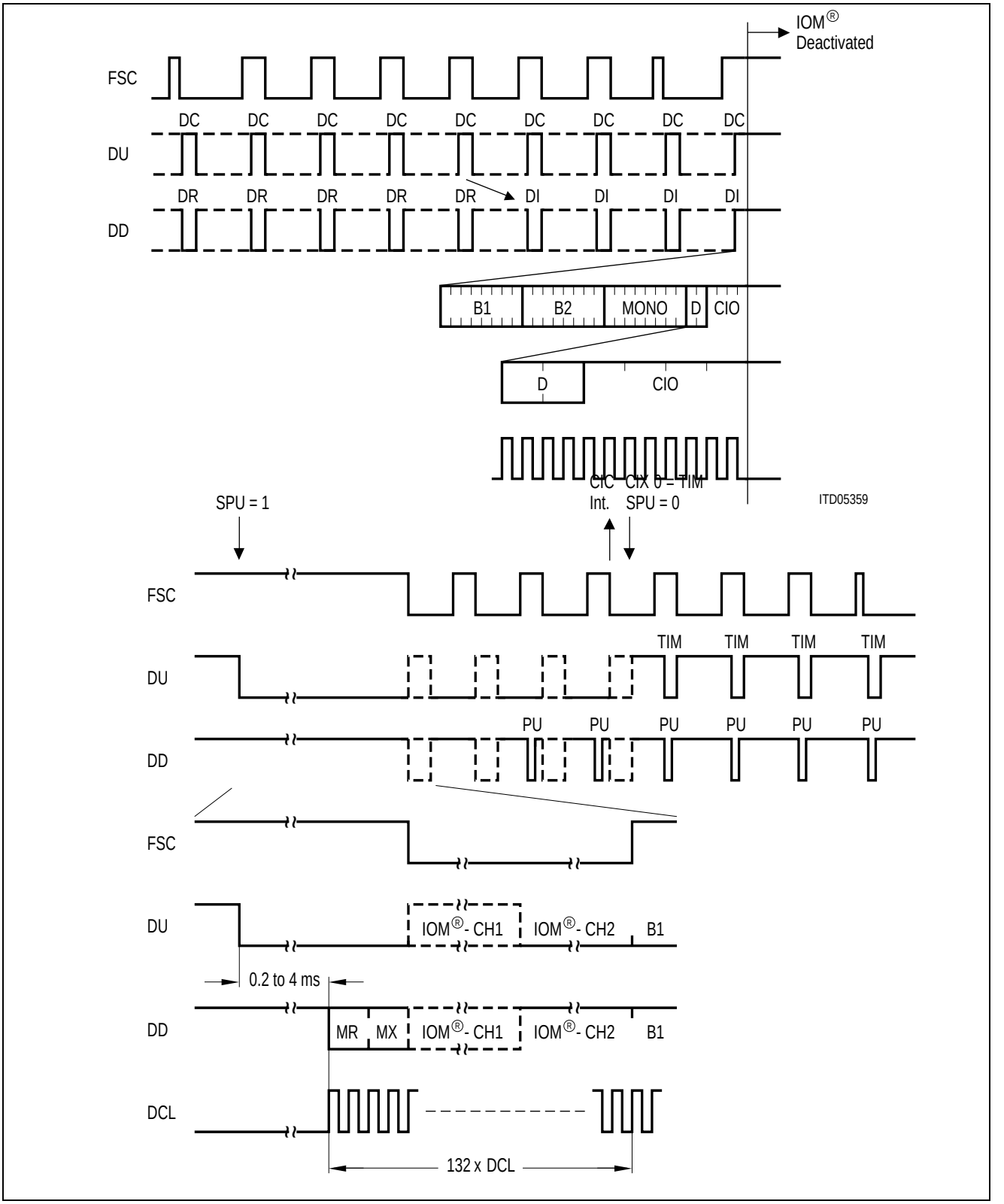
3.1.2.1 Activation / Deactivation of the IOM®-2 Interface

In order to reduce power consumption in the non-operational status the IOM-interface is brought into power down while the U_{PN}-transceiver is in the deactivated state. The clocks are stopped at bit position 30 (starting with 1). FSC remains high, DCL remains at low voltage level, the data lines remaining pulled up by the external pull-up resistors.

Since the length of the FSC-signal is reduced every eight frames, the oscillator stops only during the regular length of a FSC-signal.

The state of BCL and SDS remain low during the deactivated state.

During power-down state (C/I = 1111), only the IOM-clock signals are turned off. The oscillator, the U_{PN}-awake detector is active as well as the microcontroller clock, pulse width modulator clock and watchdog counter.



Note: DU is input and DD is low during IOM-CH1 if IDC = 1
DD is input and DU is low during IOM-CH1 if IDC = 0

Figure 43
IOM®-2 Power-Down/Activation

3.1.2.2 Activation / Deactivation of the U_{PN}-Interface

The U_{PN}-transceiver functions are controlled by commands issued in the CIX0-register. These commands are transmitted over the C/I-channel 0 and trigger certain procedures such as activation / deactivation and switching of test loops. Indications from layer 1 are obtained by evaluating the C/I0 receive register (CIR0) after a CIC-status (ISTA).

3.1.2.3 Layer-1 Command/Indication Codes in TE-Mode

Command (Upstream)	Abbr.	Code	Remarks
Timing	TIM	0000	Layer-2 device requires clocks to be activated
Reset	RES	0001	Software reset
Send Single Pulses	SSP	0010	Ones (AMI) pulses transmitted at 2 kHz
Send Continuous Pulses	SCP	0011	Ones (AMI) pulses transmitted at 192 kHz
Activate Request	AR	1000	
Activate Request Loop 3	ARL	1001	Local analog loop
Deactivation Indication	DI	1111	

Indication (Downstream)	Abbr.	Code	Remarks
Deactivation Request	DR	0000	
Power-Up	PU	0111	
Test Mode Acknowledge	TMA	0010	Acknowledge for both SSP and SCP
Resynchronization	RSY	0100	Receiver not synchronous
Activation Request	AR	1000	Receiver synchronized
Activation Request Loop 3	ARL	1001	Local loop synchronized
Activation Request Loop 2	ARL2	1010	Remote loop synchronized
Activation Indication	AI	1100	
Activation Indication Loop 3	AIL	1101	Local loop activated
Activation Indication Loop 2	AIL2	1110	Remote loop activated
Deactivation Confirmation	DC	1111	

3.1.2.4 State Diagrams

Clocking, Reset and Initialization

The link between the layer-1 (U_{PN}) part and the other functional blocks is done via the IOM-interface. The interface is synchronized by the double bit clock DCL and the frame synchronization FSC.

The layer-1 (U_{PN}) part of the PSB 2196 ISAC-P TE in TE-mode is the clock master of the IOM-interface. It activates the IOM-interface upon activation signals from the U_{PN}-interface or a low level at the data upstream line of the IOM-interface, which is maintained after the clocks are running at least in C/I0-channel, i.e. command timing (TIM) or an activation command (AR, ARL).

B1-, B2-Channels

The IOM-interface B-channels are used to convey the two 64-kbit/s user channels in both directions. However, the PSB 2196 ISAC-P TE only transfers the data transparently in the activated state (incl. analog loop activated) while the data are set to “1” in any non activated state (cf. state descriptions).

D-Channel

Similar to the B-channels the layer-1 (U_{PN}) part of the PSB 2196 ISAC-P TE transfers the D-channel transparently in both directions in the activated state.

MONITOR 0

The MONITOR channel 0 can be accessed by the ISAC-P TE, but the U_{PN}-transceiver doesn’t provide any information via this channel.

MONITOR 1

The MONITOR channel 1 can be controlled by the ISAC-P TE to program members of the ARCOFI codec family (PSB 2160, 2165) or for intercommunication with the ITAC PSB 2110.

C/I1-Channel

In TE-mode the PSB 2196 ISAC-P TE can influence the downstream C/I1-channel via the CI1X-register bits.
It receives all bits of the upstream C/I1-channel and stores their value in the CI1R-register.

T-Bit Transfer

In TE-mode the layer-1 (U_{PN}) part of the PSB 2196 ISAC-P TE conveys the T-bit position of the U_{PN}-interface to either the S/G-bit position or the A/B-bit position according to the register programming. The exact bit polarities are as follows:

Downstream ($U_{PN} \rightarrow$ IOM)
T to A/B mapping (GCR:TCM = 1):

T = 0:	A/B = 0	S/G = 1	blocked
T = 1:	A/B = 1	S/G = 1	available

T to S/G mapping (GCR:TCM = 0):

T = 0:	A/B = 1	S/G = 1	blocked
T = 1:	A/B = 1	S/G = 0	available

Upstream (IOM $\rightarrow$ U_{PN})
In upstream direction the inverse value of the BAC bit is transmitted in the U_{PN} T-bit position:
BAC to T mapping:

BAC = 1	T = 0	no D-channel request
BAC = 0	T = 1	D-channel request

Activation/Deactivation

The internal finite state machine of the PSB 2196 ISAC-P TE controls the activation/ deactivation procedures. Such actions can be initiated by signals on the U_{PN}-transmission line (INFO's) or by control (C/I) codes sent over the C/I0-channel of the IOM-interface.

The exchange of control information in the C/I-channel is state oriented. This means that a code in the C/I-channel is repeated in every IOM-frame until a change is necessary. A new code must be recognized in two consecutive IOM-frames to be considered valid (double last look criterion).

In the state diagrams a notation is employed which explicitly specifies the inputs and outputs on the U_{PN}-interface and in the C/I0-channel.

3.1.2.5 TE-Mode State Description

Reset, Pending Deactivation

State after reset or deactivation from the U_{PN}-interface by info 0. Note that no activation from the terminal side is possible starting from this state. A DC-command has to be issued to enter the state deactivated.

Deactivated

The U_{PN}-interface is deactivated and the IOM-interface is or will be deactivated. Activation is possible from the U_{PN}-interface and from the IOM-interface.

Power-Up

The U_{PN}-interface is deactivated and the IOM-interface is activated, i.e. the clocks are running.

Pending Activation

Upon the command Activation Request (AR) the PSB 2196 ISAC-P TE transmits the 2-kHz info 1 w towards the network, waiting for info 2.

Level Detect, Resynchronization

During the first period of receiving info 2 or under severe disturbances on the line the U_{PN}-receiver recognizes the receipt of a signal but is not (yet) synchronized.

Synchronized

The U_{PN}-receiver is synchronized and detects info 2. It continues the activation procedure by transmission of info 1.

Activated

The U_{PN}-receiver is synchronized and detects info 4. It concludes the activation procedure by transmission of info 3. All user channels are now conveyed transparently.

Analog Loop 3 Pending

Upon the command Activation Request Loop (ARL) the PSB 2196 ISAC-P TE loops back the transmitter to the receiver and activates by transmission of info 1. The receiver is not yet synchronized.

Analog Loop 3 Synchronized

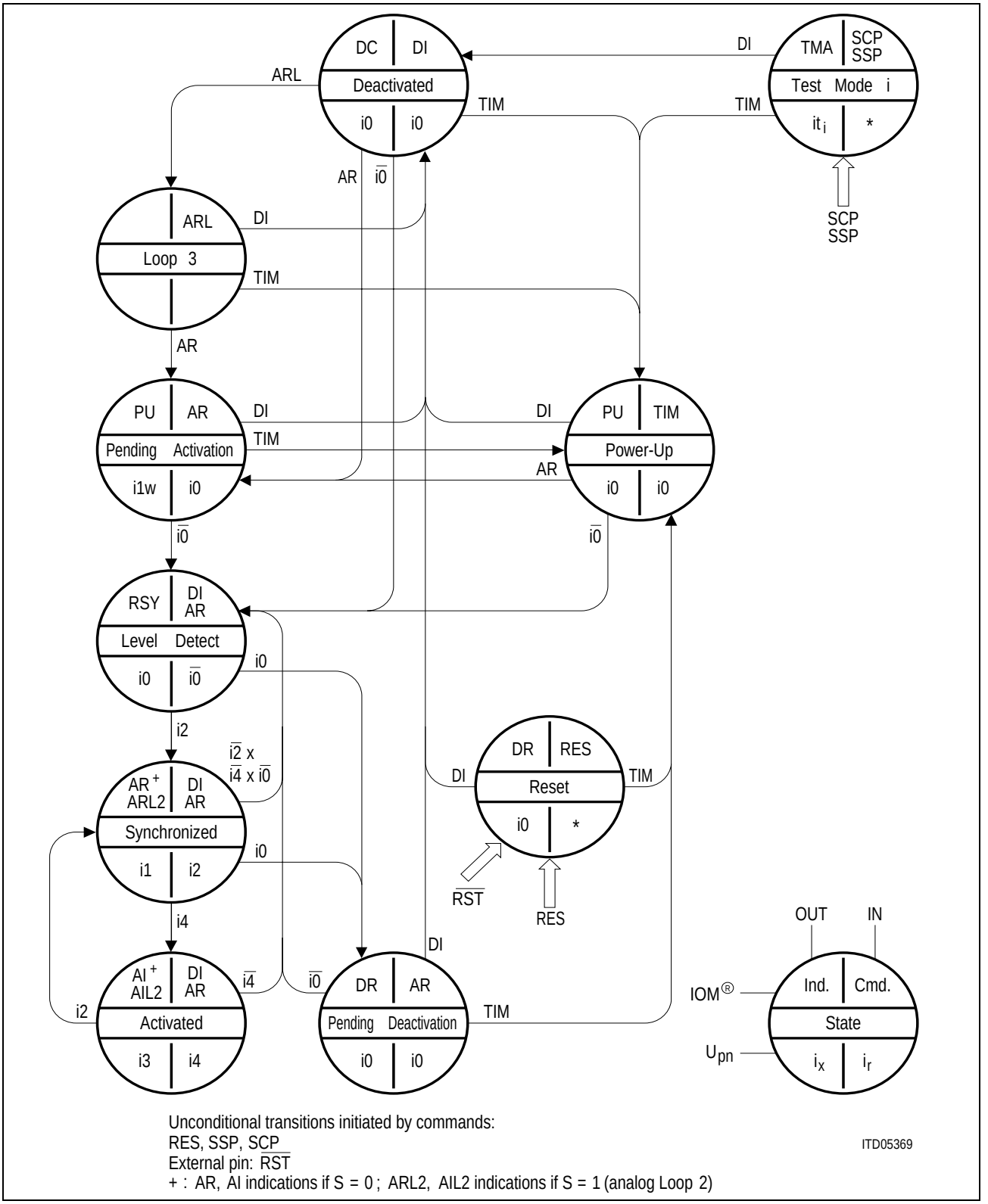
After synchronization the transmitter continues by transmitting info 3.

Analog Loop 3 Activated

After recognition of the looped back info 3 the channels are looped back transparently.

Test Mode Acknowledge

After entering test mode initiated by SCP-, SSP-commands.



Unconditional Transitions Initiated by Commands: RES, SSP, SCP
External Pin: RES*

Figure 44
State Diagram in TE-Mode

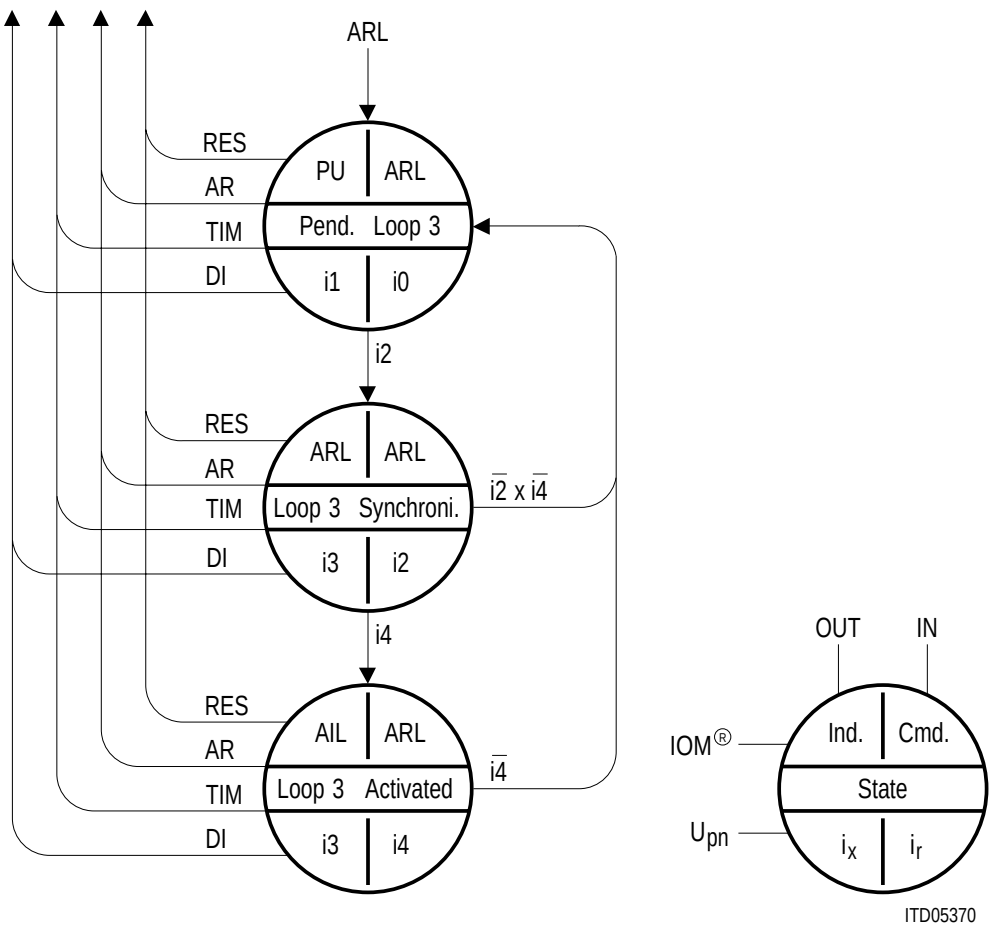


Figure 45
State Diagram TE-Mode (Test loop 3)

3.1.2.6 Example of the Activation / Deactivation

Figure 46 shows the activation / deactivation procedure between the line-card (Octat-P) and the terminal (ISAC-P TE).

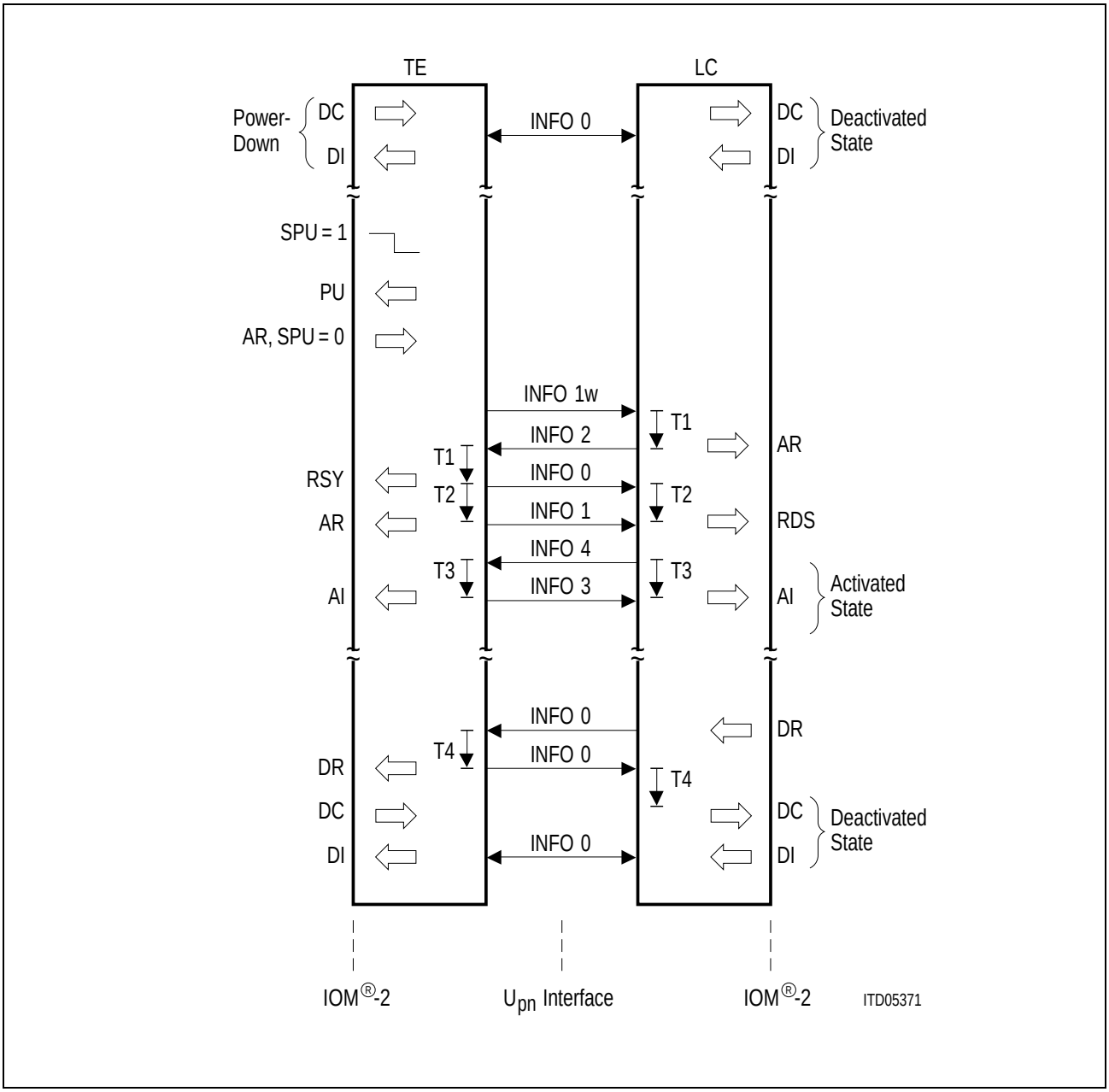


Figure 46
Activation/Deactivation (LC, TE)

Note: T1: 1.5 ms; time for error free level detection
T2: < 80 ms; time for synchronization
T3: 1 ms; four subsequent burst with no CV in F-bit
T4: 2 ms; time for error free detection of INFO 0

3.1.3 Reset

Reset Logic

Address data pins are configured as inputs. The U_{PN}-awake detector is active after reset.

A subset of the registers are set to their reset values in order to achieve a defined state of the ISAC-P TE. These registers and their meaning is listed in **table 6**.

Table 6
Reset State of the ISAC®-P TE Registers

Register	Value after Reset	Meaning
ISTA (20)	00_H	No interrupts
MASK (20)	00_H	All interrupts enabled
EXIR (24)	00_H	No interrupts
STAR (21)	48_H or $4A_H$	XFIFO is ready to be written to RFIFO is ready to receive at least 16 octets of a new message
CMDR (21)	00_H	No command
MODE (22)	00_H	Receiver inactive
RBCL (25)	00000000_B	Receiver byte counter is reset
SPCR (30)	00_H	IDP1-pin = “high”
CIR0 (31)	$7C_H$	Another device occupies the D- and C/I-channel Received CI-code is “1111” No CI-code change
CIX0 (31)	$3C_H$	TIC-bus is not requested for transmitting a C/I-code Transmitted CI-code is “1111”
STCR (37)	00_H	Terminal specific functions disabled TIC-bus address is “000”
ADF1 (38)	00_H	Interframe timefill is continuous “1”
ADF2 (39)	00_H	Non-IOM-2 interface mode selection
GCR (2C)	00_H	Pull-up on AD active, MCLK = 3.84 MHz
LCD (2D)	00_H	LCD contrast off
LED (3C-3E)	00_H	LED’s off

3.1.4 Initialization

During initialization a subset of registers have to be programmed to set the configuration parameters according to the application and desired features. They are listed in **table 7**.

In order to keep the compatibility of the ICC (PEB 2070) the ISAC-P TE enters IOM-1 mode after reset. The microprocessor has to select the IOM-2 interface mode by setting the IMS-bit to “1”.

Table 7
Initialization of the ISAC®-P TE Registers

Register	Bit	Effect	Application	Restricted to
ADF2 (39)	IMS	Program IOM-2 interface mode		
SPCR (30)	SPU	Set the ISAC-P TE in standby by requesting clocks		
ADF1 (38)	IDC	IOM-data port direction		
CIX0 (31)	RSS	Hardware reset generation		
STCR (37)	TSF	Terminal Specific function		
MODE (22)	RAC	HDLC-receiver control		

3.2 TR-Mode

3.2.1 Control of the U_{PN}-Transceiver

3.2.1.1 Activation / Deactivation of the IOM®-2 Interface

The U_{PN}-transceiver functions are controlled by commands issued by the ISAC-P TE depending on the current state. In downstream direction, only the commands “DR”, “AR” and “DC” trigger the state machine. In upstream direction, the four indications “TIM”, “AR”, “AI” or “DC” are generated.

If the IOM-2 interface is turned off, an asynchronous awake procedure is initiated if the ISAC-P TE in TR-mode request an activation procedure.

3.2.1.2 Layer-1 Command/Indication Codes in TR-Mode

Command (downstream)	Abbr.	Code	Remarks
Deactivate request	DR	0000	
Activate request	AR, AI, ARL2, AIL2	1xx0	Transmission of Info 2 and Info 4 according to the U_{PN}-procedure
Deactivation confirmation	DC	1111	Info 0 or DC received after deactivation request or no TIC-bus request

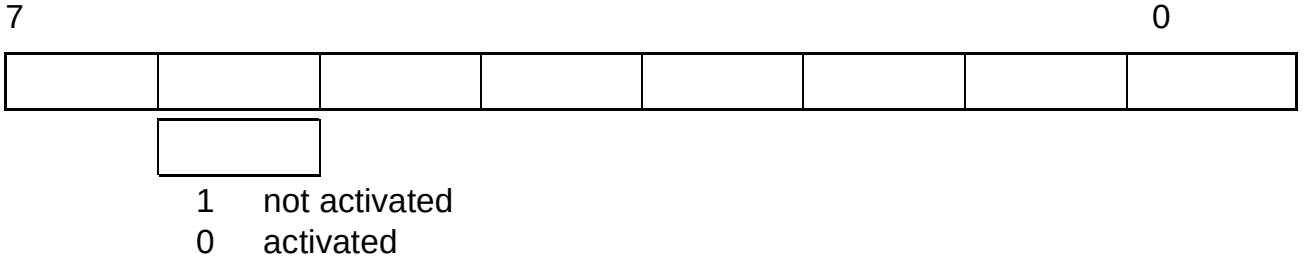
Indication (upstream)	Abbr.	Code	Remarks
Timing	TIM	0000	Deactivation state, activation from the line not possible
Activate request	AR	1000	Info 1 received
Activation indicaton	AI	1100	Info 3 received
Deactivation indication	DI	1111	Deactivation acknowledgement, quiescent state

In TR-mode, the U_{PN}-interface is activated if the C/I-code Activate Request (AR, ARL2) or Activate Indication (AI, AIL2) has been detected in downstream direction. It stays activated until the C/I-code Deactivate Request (DR) is received in downstream direction.

3.2.1.3 State Diagrams

In TR-mode the layer-1 (U_{PN}) part of the PSB 2196 ISAC-P TE is an IOM-interface slave in any aspect. Therefore it is also able to activate the IOM-interface by pulling the data upstream line to zero asynchronously.

Since the PSB 2196 ISAC-P TE in TR-mode is a stand alone function without microprocessor aid, the PSB 2196 ISAC-P TE in TR-mode will indicate the activated state of the slave U_{PN}-interface by pulling bit 6 of the C/I1-channel on the data upstream line to “0”.



1 not activated
0 activated

3.2.1.4 TR-Mode State Description

Pending Deactivation

State after reset or deactivation from the IOM-interface by command DR. Note that no activation from the network side is possible starting from this state.

Wait for $\overline{\text{DR}}$

This state is entered from the pending deactivation state once info 0 has been identified or after the command DI.

Deactivated

The U_{PN}-interface is deactivated and the IOM-interface is or will be deactivated. Activation is possible from the U_{PN}-interface and from the IOM-interface. If activation is initiated by the terminal side it first leads to the activation of the IOM-interface by the indication “TIM” (Awake: DU pulled to V_{SS} asynchronously, later on synchronously).

Pending Activation 1

After activation from the line has been started the indication Activation Request (AR) is issued to get synchronization from the upstream network side.

Pending Activation 2

Upon the command Activation Request (AR) the PSB 2196 ISAC-P TE transmits the 4-kHz info 2 towards the terminal, waiting for info 1.

Synchronized

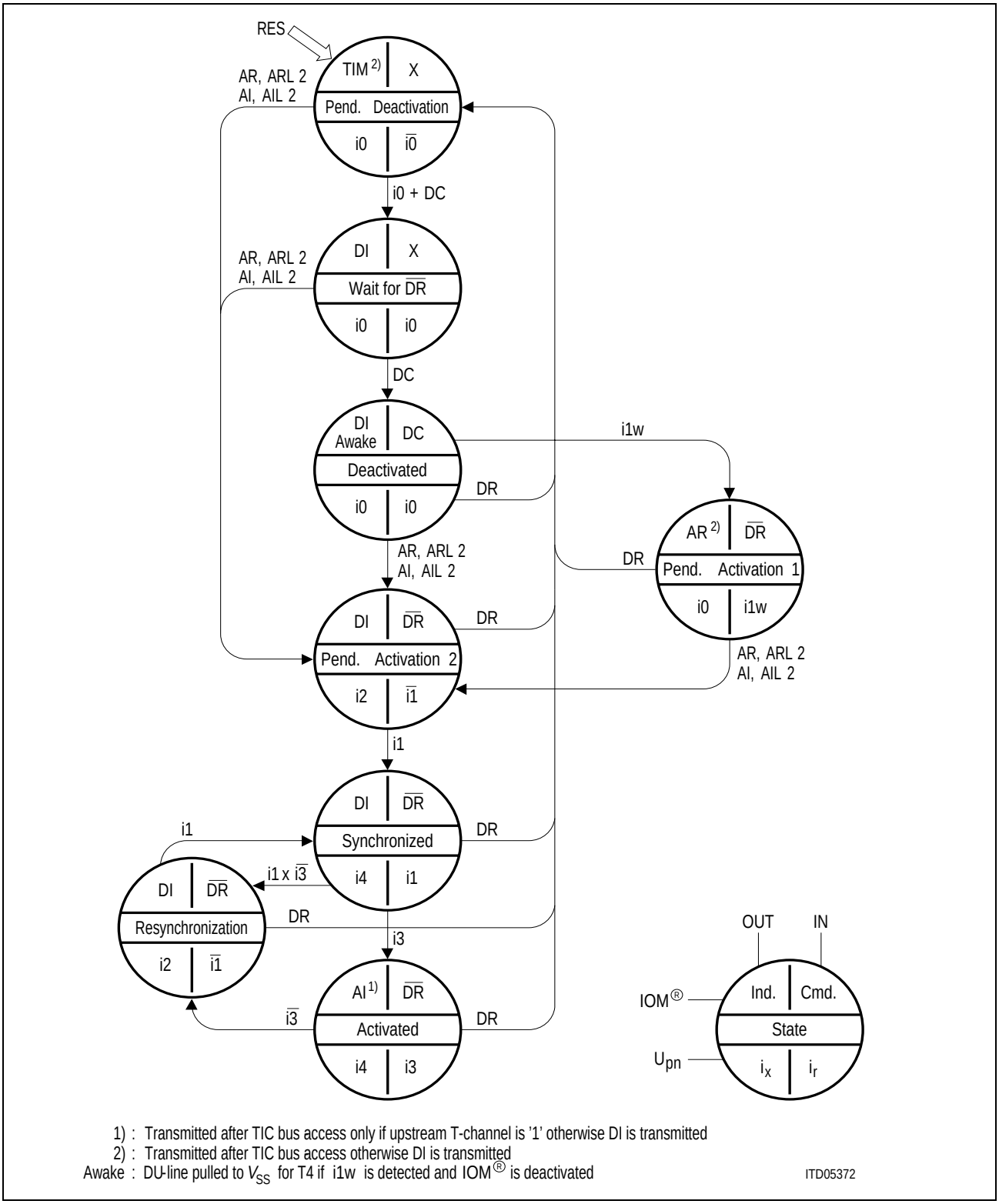
The U_{PN}-receiver is synchronized and detects info 1. It continues the activation procedure by transmission of info 4.

Activated

The U_{PN}-receiver is synchronized and detects info 3. The activation procedure is now completed and B1, B2, and downstream D-channels are conveyed transparently. For transmission of the upstream D-channel the TIC-bus function applies.

Resynchronization

Under severe disturbances on the line the U_{PN}-receiver still recognizes the receipt of a signal but is no more synchronized.



*: Transmitted after TIC-bus access only if upstream T-channel is "1" otherwise DC is transmitted
+: Transmitted after TIC-bus access otherwise DC is transmitted
Awake: DU-line pulled to V_{SS} for T4 if i1w is detected and IOM is deactivated

Figure 47
State Diagram TR-Mode

3.2.1.5 Example of the Activation / Deactivation

Figure 48 shows the activation / deactivation procedure between the ISAC-P TE operating in TR-mode and a ISAC-P TE on the secondary terminal.

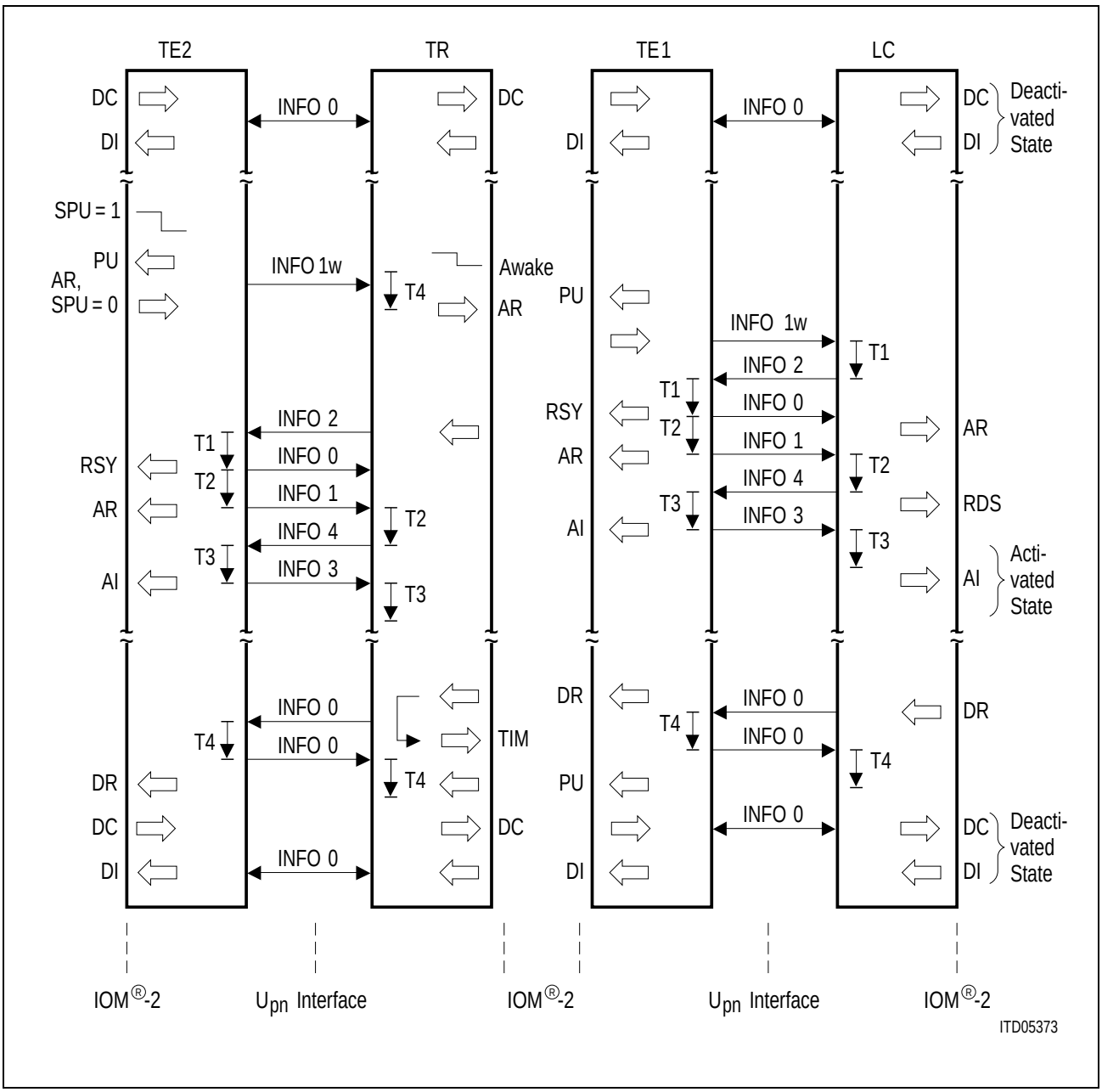


Figure 48
Activation/Deactivation (TR, TE)

Note: T1: 1.5 ms; time for error free level detection
T2: > 80 ms; time for synchronization
T3: 1 ms; four subsequent bursts with no CV in F-bit
T4: 2 ms; time for error free detection of INFO 0

3.2.2 D-Channel Access Procedure

The TR-mode uses the TIC-bus access procedure to access the upstream D-channel if requested by the terminal connected to the U_{PN}-interface.

Idle

The idle state is specified by the TIC-bus address as “111” and the BAC-bit set to “1”. During this state, the upstream D-channel is transparent and the downstream T-bit transmits the inverse value of the stop/go bit.

TIC-Bus Access by other D-Channel Sources

If the TIC-bus is occupied by another source which is indicated by the TIC-bus address different from “111” or the BAC-bit set to “0”, the downstream T-bit changes to the block value (T = 0).

TIC-Bus Request by U_{PN}-Receiver

Upon a received T-bit = 0 from the U_{PN}-interface which is interpreted as a D-channel access request the PSB 2196 ISAC-P TE tries to access the TIC-bus according to the specified procedure using TIC-bus address “011”.
After the TIC-bus has been occupied the inverse status of the S/G-bit position is transmitted via the U_{PN} T-bit.

If the received T-bit changes to “1”, the ISAC-P TE in TR-mode releases the TIC-bus immediately.

Blocked Condition during a Frame Transmission

If a blocked condition occurs during the transmission of a frame, the S/G-bit changes to stop and no further D-bits are output to the IOM-2 interface. The stop condition changes the downstream T-bit to a blocked state and the HDLC-transmitter in the terminal aborts the frame. If the upstream “T”-bit remains “0” (BAC-bit of the terminal), the TR ISAC-P TE retains its TIC-bus access to make sure that the slave terminal can transmit a frame if the stop/go bit becomes “go” again.

3.2.3 Reset State

The reset state is entered after applying an active signal to the reset input.

In reset state, the transceiver state machine is reset and info 0 is output on the U_{PN}-interface. The TIC-bus access state machine is also reset so that the TIC-bus becomes idle.

3.2.4 Software Restriction for TR Operation

To ensure a correct operation of a terminal repeater configuration it is necessary to implement software restrictions in the terminal software.

Activation of the U_{PN} Line

To activate the U_{PN} Interface it is necessary to output the C/I0 command “AR”. If this is output permanently, there is a chance that the TR ISAC-P TE enters a blocking state. This state may be entered by a transition form the deactivate state to Pending Activation 1 and to Pending Deactivation. For the transition to wait for $\overline{DR}$ it is necessary to receive Info 0 or to receive “DC”. Info 0 will not be received since the terminal connected to the TR ISAC-P TE remains outputting info 1 w. “DC” is also not received since the TR ISAC-P TE outputs TIM which results in a “PU” indication.
This transition may occur if the line between linecard and terminal is connected while the second terminal already requests activation. To avoid the blocking situation it is recommended to toggle between “AR” and “TIM” on the terminal software. Each C/I command should be valid for 20 ms.

Early Release of TIC Bus

The TR ISAC-P TE releases the TIC bus before the D-bits of that U_{PN} frame have been transmitted on IOM-2. As a result the HDLC frame from the second terminal may be corrupted and indicated as aborted frame by the linecard HDLC receiver.

To avoid problems the terminal software has to set the BAC-bit to “1” before the last part of an HDLC frame is entered into the XFIFO and keeps it active for at least 500 µs after the XPR interrupt has been generated.

Continuous TIC Bus Access by the Second Terminal

Since the T-bit is only transferred every 500 µs there is the chance that the second terminal may transmit continuous HDLC messages and the first terminal has no chance to interface.
To assure that the first terminal is able to enter HDLC messages in between, the terminal software has to wait for at least 250 µs before another HDLC frame is started.

4 Register Description

The parameterization of the ISAC-P TE and the transfer of data and control information between the microprocessor and the ISAC-P TE is performed through a set of registers.

The register set in the address range 00 – $2B_H$ pertains to the HDLC-transceiver. It includes the two FIFOs having an identical address range from 00 – $1F_H$.

The register set ranging from 30 – $3B_H$ pertains to the control of layer-1 functions and of the IOM-2 interface.

In order to access the LCD-contrast control, the prescaler and the LED-matrix new registers have been added (2C, 2D, 3C, 3D, 3E).

Address 2F accesses a test register for factory tested. It should not be modified during operation. The reset value is 00_H.

Table 8
ISAC-P TE Address Map Serial Interface Mode

Adr.	Bit 7							Bit 0	Reg.	R/W
00 – 1F									RFIFO	R
00 – 1F									XFIFO	W
20	RME	RPF	RSC	XPR	TIN	CIC	SIN	EXI	ISTA	R
20	RME	RPF	RSC	XPR	TIN	CIC	SIN	EXI	MASK	W
21	XDOV	XFW	XRNR	RRNR	MBR	MAC1	X	MAC0	STAR	R
21	RMC	RRES	RNR	STI	XTF	XIF	XME	XRES	CMDR	W
22	MDS2	MDS1	MDS0	TMD	RAC	DIM2	DIM1	DIM0	MODE	R/W
23	CNT			VALUE					TIMR	R/W
24	XMR	XDU	PCE	RFO	SOV	MOS	0	WOV	EXIR	R
24									XAD1	W
25	RBC7	RBC6	RBC5	RBC4	RBC3	RBC2	RBC1	RBC0	RBCL	R
25									XAD2	W
26									SAPR	R
26	SAPI1						CRI	0	SAP1	W
27	RDA	RDO	CRC	RAB	SA1	SA0	CR	TA	RSTA	R
27	SAPI2						MCS	0	SAP2	W
28				TEI1				EA	TEI1	W
29									RHCR	R
29				TEI2				EA	TEI2	W
2A	XAC	VN1	VN0	OV	RBC11	RBC10	RBC9	RBC8	RBCH	R
2B	0	0	0	0	WFA	0	TREC	SDET	STAR2	R
30	SPU	0	0	TLP	C1C1	C1C0	C2C1	C2C0	SPCR	R/W
31	0	BAC	C	O	D	R0	CIC0	CIC1	CIR0	R
31	RSS	BAC	C	O	D	X0	1	1	CIX0	W
32									MOR0	R
32									MOX0	W
33	C	O	D	R	1		MR1	MX1	CIR1	R
33	C	O	D	X	1		1	1	CIX1	W
34									MOR1	R
34									MOX1	W
35									C1R	R/W
36									C2R	R/W

ISAC-P TE Address Map Serial Interface Mode (cont'd)

Adr.	Bit 7							Bit 0	Reg.	R/W
37									B1CR	R
37	TSF	TBA2	TBA1	TBA0	ST10	ST0	SC1	SC0	STCR	W
38									B2CR	R
38	WTC1	WTC2	CI1E	IDC	IOF	0	0	ITF	ADF1	W
39	IMS	D2C2	D2C1	D2C0	ODS	D1C2	D1C1	D1C0	ADF2	R/W
3A	MDR1	MER1	MDA1	MAB1	MDR0	MER0	MDA0	MAB0	MOSR	R
3A	MRE1	MRC1	MXE1	MXC1	MRE0	MRC0	MIE0	MXC0	MOCR	W
2C	BCS	LLC	PUR	SDO	TCM	LEM	PR1	PR0	GCR	W
2C			SCLK	SDI					GCR	R
2D					LCON3	LCON2	LCON1	LCON0	LCCR	R/W
3C	L2C4	L2C3	L2C2	L2C1	L1C4	L1C3	L1C2	L1C1	LER0	R/W
3D	L4C4	L4C3	L4C2	L4C1	L3C4	L3C3	L3C2	L3C1	LER1	R/W
3E	L6C4	L6C3	L6C2	L6C1	L5C4	L5C3	L5C2	L5C1	LER2	R/W
2F									TEST	

4.1 ISAC®-P TE Register Summary: HDLC-Operation and Status Registers

RFIFO HDLC-Receive FIFO

Value after reset: xx

Adr.	Bit 7							Bit 0	Reg.	R/W
00 – 1F									RFIFO	R

A read access to any address within the range 00 – $1F_H$ gives access to the "current" FIFO location selected by an internal pointer which is automatically incremented after each read access. This allows for the use of efficient "moving string" type commands by the processor.

The RFIFO contains up to 32 bytes of received frame.

After an ISTA:RPF-interrupt, exactly 32 bytes are available.

After an ISTA:RME-interrupt, the number of bytes available can be obtained by reading the RBCL-register.

XFIFO HDLC-Transmit FIFO

Value after reset: xx

Adr.	Bit 7							Bit 0	Reg.	R/W
00 – 1F									XFIFO	W

A write access to any address within the range 00 – $1F_H$ gives access to the “current” FIFO-location selected by an internal pointer which is automatically incremented after each write access. This allows for the use of efficient “move string” type commands by the processor.

Up to 32 bytes of transmit data can be written into the XFIFO following an ISTA:XPR-interrupt.

Interrupt Status Register

Value after reset: 00_H

Adr.	Bit 7							Bit 0	Reg.	R/W
20	RME	RPF	RSC	XPR	TIN	CIC	SIN	EXI	ISTA	R

Bits 7 to 3 and 1 of the ISTA-register are cleared with the read access. CIC and EXI remain active until their associated status register has been read.

RME **Receive Message End**
One complete frame of length less than or equal to 32 bytes, or the last part of a frame of length greater than 32 bytes has been received. The contents are available in the RFIFO. The message length and additional information may be obtained from RBCH + RBCL and the RSTA-register.

RPF **Receive Poll Full**
A 32-byte block of a frame longer than 32 bytes has been received and is available in the RFIFO. The frame is not yet complete.

RSC **Receive Status Change**. Used in auto-mode only.
A status change in the receiver of the remote station – Receiver Ready/ Receiver Not Ready – has been detected (RR or RNR S-frame). The actual status of the remote station can be read from the STAR register (RRNR-bit).

XPR **Transmit Pool Ready**
A data block of up to 32 bytes can be written to the XFIFO.

An XPR-interrupt will be generated in the following cases:

– after an XTF or XIF command, when one transmit pool is emptied and the frame is not yet complete

– after an XTF together with an XME-command is issued, when the whole transparent frame has been transmitted

– after an XIF together with an XME-command is issued, when the whole I-frame has been transmitted and a positive acknowledgement from the remote station has been received (auto-mode).

TIN **Timer Interrupt**
The internal timer and repeat counter has expired (see TIMR-register).

CIC **Channel Change**
A change in C/I-channel 0 or C/I-channel 1 (only in IOM-2 TE-mode) has been recognized. The actual value can be read from CIR0 or CIR1.

SIN **Synchronous Transfer Interrupt**
When programmed (STCR-register), this interrupt is generated to enable the processor to lock on to the IOM-timing, for synchronous transfers.

EXI **Extended Interrupt**
This bit indicates that one of six non-critical interrupts has been generated. The exact interrupt cause can be read from EXIR.

Mask Register
Value after reset: 00_H

Adr.	Bit 7							Bit 0	Reg.	R/W
20	RME	RPF	RSC	XPR	TIN	CIC	SIN	EXI	MASK	W

Each interrupt source in the ISTA-register can be selectively masked by setting the corresponding bit in MASK to “1”. Masked interrupt status bits are not indicated when ISTA is read. Instead, they remain internally stored and pending, until the mask bit is reset to zero.

Note: In the event of an extended interrupt and of a C/I-channel change, EXI and CIC are set in ISTA even if the corresponding mask bit in MASK are active, but no interrupt ($\overline{\text{INT}}$-pin) is generated.

Status Register
Value after reset: 48_H or $4A_H$

Adr.	Bit 7							Bit 0	Reg.	R/W
21	XDOV	XFW	XRNR	RRNR	MBR	MAC1	X	MAC0	STAR	R

XDOV **Transmit Data Overflow**
More than 32 bytes have been written into one pool of the XFIFO, i.e. data has been overwritten.

XFW **Transmit FIFO-Write Enable**
Data may be written into the XFIFO.

XRNR **Transmit RNR**. Used in auto-mode only.
In auto-mode, this bit indicates whether the ISAC-P TE receiver is in the “ready” (0) or “not ready” (1) state. When “not ready”, the ISAC-P TE sends an S-frame autonomously to the remote station when an I-frame or an S-frame is received.

RRNR **Receive RNR**. Used in auto-mode only.
In the auto-mode, this bit indicates whether the ISAC-P TE has received an RR or an RNR-frame, this being an indication of the current state of the remote station: receiver ready (0) or receiver not ready (1).

MBR **Message Buffer Ready**
This bit signifies that temporary storage is available in the RFIFO to receive at least the first 16 byte of a new message.

MAC1 **MONITOR Transmit Channel 1 Active**
Data transmission is in progress in monitor channel 1.

MAC0 **MONITOR Transmit Channel 0 Active**
Data transmission is in progress in monitor channel 0.

Command Register
Value after reset: 00_H

Adr.	Bit 7							Bit 0	Reg.	R/W
21	RMC	RRES	RNR	STI	XTF	XIF	XME	XRES	CMDR	W

Note: The maximum time between writing to the CMDR-register and the execution of the command is 2.5 DCL clock cycles. During this time no further commands should be written to the CMDR-register to avoid any loss of commands.

RMC **Receive Message Complete**
Reaction to RPF (Receive Pool Full) or RME (Receive Message End) interrupt. By setting this bit, the processor confirms that it has fetched the data, and indicates that the corresponding space in the RFIFO may be released.

RRES **Receiver Reset**
HDLC-receiver is reset, the RFIFO is cleared of any data.
In addition, in auto-mode, the transmit and receive counters (V(S), V(R)) are reset.

RNR **Receiver Not Ready**. Used in auto-mode only.
Determines the state of the ISAC-P TE HDLC-receiver.
When RNR = “0”, a received I- or S-frame is acknowledged by an RR-supervisory frame, otherwise by an RNR-supervisory frame.

STI **Start Timer**
The ISAC-P TE hardware timer is started when STI is set to one. In the internal timer mode (TMD-bit, MODE register) an S-command (RR, RNR) with poll bit set is transmitted in addition. The timer may be stopped by a write of the TIMR-register.

XTF **Transmit Transparent Frame**
After having written up to 32 bytes in the XFIFO, the processor initiates the transmission of a transparent frame by setting this bit to “1”. The opening flag is automatically added to the message by the ISAC-P TE.

XIF **Transmit I-Frame**. Used in auto-mode only.
After having written up to 32 bytes in the XFIFO, the processor initiates the transmission of an I-frame by setting this bit to “1”. The opening flag, the address and the control field are automatically added by the ISAC-P TE.

XME **Transmit Message End**
By setting this bit to “1” the processor indicates that the data block written last in the XFIFO complete the corresponding frame. The ISAC-P TE terminates the transmission by appending the CRC and the closing flag sequence to the data.

XRES **Transmitter Reset**
HDLC-transmitter is reset and the XFIFO is cleared of any data.
This command can be used by the processor to abort a frame currently in transmission.

Notes:
- After an XPR-interrupt further data has been written in the XFIFO and the appropriate Transmit Command (XTF or XIF) has to be written in the CMDR-register again to continue transmission, when the current frame is not yet complete (see also XPR in ISTA).
- During frame transmission, the 0-bit insertion according to the HDLC bit-stuffing mechanism is done automatically.

Mode Register
Value after reset: 00_H

Adr.	Bit 7							Bit 0	Reg.	R/W
22	MDS2	MDS1	MDS0	TMD	RAC	DIM2	DIM1	DIM0	MODE	R/W

MDS2 – 0 Mode Select
Determines the message transfer mode of the HDLC-controller, as follows:

MDS2 MDS1 MDS0	Mode	Number of Address Bytes	Address Comparison 1. Byte	2. Byte	Remark
000	Auto-mode	1	TEI1, TEI2	–	One-byte address compare. HDLC-protocol handling for frames with address TEI1.
001	Auto-mode	2	SAP1, SAP2, SAPG	TEI1, TEI2, TEIG	Two-byte address compare. LAPD-protocol handling for frames with address SAP1 + TEI1.
010	Non-Auto mode	1	TEI1, TEI2	–	One-byte address compare.
011	Non-Auto mode	2	SAP1, SAP2, SAPG	TEI1, TEI2, TEIG	Two-byte address compare.
100	Reserved				
101	Transparent mode 1	> 1	–	TEI1, TEI2, TEIG	Low-byte address compare.
110	Transparent mode 2	–	–	–	No address compare. All frames accepted.
111	Transparent mode 3	> 1	SAP1, SAP2, SAPG	–	High-byte address compare.

Note: SAP1, SAP2: two programmable address values for the first received address byte (in the case of an address field longer than 1 byte);
SAPG = fixed value FC/FE_H.

TEI1, TEI2: two programmable address values for the second (or the only, in the case of a one-byte address) received address byte;
TEIG = fixed value FF_H.

TMD **Timer Mode**
Sets the operating mode of the ISAC-P TE timer. In the external mode (0) the timer is controlled by the processor. It is started by setting the STI-bit in CMDR and it is stopped by a write of the TIMR-register.
In the internal mode (1) the timer is used internally by the ISAC-P TE for timeout and retry conditions (handling of LAPD/HDLC-protocol in auto-mode).

RAC **Receiver Active**
The HDLC-receiver is activated when this bit is set to “1”.

DIM2 – 0 **Digital Interface Mode**
These bits define the characteristics of the IOM-Data Ports (IDP0, IDP1) according to following tables:

IOM®-2 Modes (ADF2:IMS = 1)

	DIM2-0				
Characteristics	**000**	**001**	**010**	**011**	**100-111**
IOM-2 terminal mode SPCR: SPM = 0	x	x	x	x	
Last octet of IOM channel 2 used for TIC-bus access	x	x			
Stop/go bit evaluated for D-channel access handling		x		x	
Reserved					x
Applications					
TE mode		x		x	

Timer Register
Value after reset: xx

Adr.	Bit 7		Bit 0	Reg.	R/W
23	CNT	VALUE		TIMR	R/W

CNT The meaning depends on the selected timer mode (TMD bit, MODE register).

*** Internal Timer Mode (TMD = 1)**

CNT indicates the maximum number of S-commands “N1” which are transmitted autonomously by the ISAC-P TE after expiration of time period T1 (retry, according to HDLC).

The internal timer procedure will be **started** in auto-mode:

– after start of an I-frame transmission

or

– after an “RNR” S-frame has been received.

After the last retry, a timer interrupt (TIN-bit in ISTA) is generated.

The timer procedure will be **stopped** when

– a TIN-interrupt is generated. The time between the start of an I-frame transmission or reception of an “RNR” S-frame and the generation of a TIN-interrupt is equal to: (CNT + 1) $\times$ T1.

– or the TIMR is written.

– or a positive or negative acknowledgement has been received.

Note: The maximum value of CNT can be 6. If CNT is set to 7, the number of retries is unlimited.

*** External Timer Mode (TMD = 0)**

CNT together with VALUE determine the time period T2 after which a TIN-interrupt will be generated:

CNT $\times$ 2.048 s + T1

with T1 = (VALUE + 1) $\times$ 0.064 s,

in the normal case, and

T2 = 16348 $\times$ CNT $\times$ DCL + T1

with T1 = 512 × (VALUE + 1) × DCL

when TLP = 1 (test loop activated, SPCR-register).

DCL denotes the period of the DCL-clock.

The timer can be started by setting the STI-bit in CMDR and will be stopped when a TIN-interrupt is generated or the TIMR-register is written.

Note: If CNT is set to 7, a TIN-interrupt is indefinitely generated after every expiration of T1.f.

VALUE Determines the time period T1:

T1 = (VALUE +1) × 0.064 s (SPCR:TLP = 0, normal mode)

T1 = 512 × (VALUE +1) × DCL (SPCR:TLP = 1, test mode).

Extended Interrupt Register
Value after reset: 00_H

Adr.	Bit 7							Bit 0	Reg.	R/W
24	XMR	XDU	PCE	RFO	SOV	MOS	0	WOV	EXIR	R

XMR **Transmit Message Repeat**
The transmission of the last frame has to be repeated because:

– the ISAC-P TE has received a negative acknowledgement to an I-frame in auto-mode (according to HDLC/LAPD)
– or a collision on the S-bus has been detected after the contents of the first XFIFO of a transmit frame.

XDU **Transmit Data Underrun**
The current transmission of a frame is aborted by transmitting seven “1’s” because the XFIFO holds no further data. This interrupt occurs whenever the processor has failed to respond to an XPR-interrupt (ISTA-register) quickly enough, after having initiated a transmission and the message to be transmitted is not yet complete.

Note: When a XMR- or an XDU-interrupt is generated, it is not possible to send transparent frames or I-frames until the interrupt has been acknowledged by reading EXIR.

PCE **Protocol Error**. Used in auto-mode only.
A protocol error has been detected in auto-mode due to a received

– S- or I-frame with an incorrect sequence number N (R) or
– S-frame containing an I-field.

RFO **Receive Frame Overflow**
The received data of a frame could not be stored, because the RFIFO is occupied. The whole message is lost.

This interrupt can be used for statistical purposes and indicates that the processor does not respond quickly enough to an RPF- or RME-interrupt (ISTA).

SOV **Synchronous Transfer Overflow**
The synchronous transfer programmed in STCR has not been acknowledged in time via the SC0/SC1-bit.

MOS **MONITOR Status**
A change in the MONITOR Status Register (MOSR) has occurred (IOM-2). A new MONITOR channel byte is stored in MOR0 (IOM-1).

WOV **Watchdog Timer Overflow**. Used only if terminal specific functions are enabled (STCR:TSF = 1).

Signals the expiration of the watchdog timer, which means that the processor has failed to set the watchdog timer control bits WTC1 and WTC2 (ADF1-register) in the correct manner. A reset pulse has been generated by the ISAC-P TE.

Transmit Address 1
Value after reset: xx

Adr.	Bit 7							Bit 0	Reg.	R/W
24									XAD1	W

Used in auto-mode only.

XAD1 contains a programmable address byte which is appended automatically to the frame by the ISAC-P TE in auto-mode. Depending on the selected address mode XAD1 is interpreted as follows:

*** 2-Byte Address Field**

XAD1 is the high byte (SAPI in the ISDN) of the 2-byte address field. Bit 1 is interpreted as the command/response bit “C/R”. It is automatically generated by the ISAC-P TE following the rules of ISDN LAPD-protocol and the CRI-bit value in SAP1-register. Bit 1 has to be set to “0”.

C/R-Bit			
Command	**Response**	**Transmitting End**	**CRI-Bit**
0	1	subscriber	0
1	0	network	0

In the ISDN LAPD the address field extension bit “EA”, i.e. bit 0 of XAD1 has to be set to “0”.

*** 1-Byte Address Field**

According to the X.25 LAPB-protocol, XAD1 is the address of a command frame.

Note: In standard ISDN-applications only 2-byte address fields are used.

Receive Frame Byte Count Low Register
Value after reset: 00_H

Adr.	Bit 7							Bit 0	Reg.	R/W
25	RBC7	RBC6	RBC5	RBC4	RBC3	RBC2	RBC1	RBC0	RBCL	R

RBC7 – 0 **Receive Byte Count**
Eight least significant bits ot the total number of bytes in a received message. Bits RBC4 – 0 indicate the length of a data block currently available in the RFIFO, the other bits (together with RBCH) indicate the number of whole 32-byte blocks received.

If exactly 32 bytes are received RBCL holds the value 20_H.

Transmit Address 2

Adr.	Bit 7							Bit 0	Reg.	R/W
25									XAD2	W

Used in auto-mode only.

XAD2 contains the second programmable address byte, whose function depends on the selected address mode:

*** 2-Byte Address Field**

XAD2 is the low byte (TEI in the ISDN) of the 2-byte address field.

*** 1-Byte Address Field**

According to the X.25 LAPB-protocol, XAD2 is the address of a response frame.

Note: See note to XAD1-register description.

Received SAPI-Register

Adr.	Bit 7							Bit 0	Reg.	R/W
26									SAPR	R

When a transparent mode 1 is selected SAPR contains the value of the first address byte of a receive frame.

SAPI1-Register

Value after reset: xx

Adr.	Bit 7			Bit 0	Reg.	R/W
26	SAPI1	CRI	0		SAP1	W

SAPI1 **SAPI1-value**
Value of the first programmable Service Access Point Identifier (SAPI) according to the ISDN LAPD-protocol.

CRI **Command/Response Interpretation**
CRI defines the end of the ISDN-user-network interface the ISAC-P TE is used on, for the correct identification of “Command” and “Response” frames. Depending on the value of CRI the C/R-bit will be interpreted by the ISAC-P TE, when receiving frames in auto-mode, as follows:

		C/R-Bit	
CRI-Bit	**Receiving End**	**Command**	**Response**
0	subscriber	1	0
1	network	0	1

For transmitting frames in auto-mode, the C/R-bit manipulation will also be done automatically, depending on the value of the CRI-bit (refer to XAD1-register description).

In message transfer modes with SAPI-address recognition the first received address byte is compared with the programmable values in SAP1, SAP2 and the fixed group SAPI.

In 1-byte address mode, the CRI-bit is to be set to “0”.

Receive Status Register
Value after reset: xx

Adr.	Bit 7							Bit 0	Reg.	R/W
27	RDA	RDO	CRC	RAB	SA1	SA0	C/R	TA	RSTA	R

RDA **Receive Data**
A “1” indicates that data is available in the RFIFO. After an RME-interrupt, a “0” in this bit means that data is available in the internal registers RHCR or SAPR only (e.g. S-frame). See also RHCR-register description table.

RDO **Receive Data Overflow**
At least one byte of the frame has been lost, because it could not be stored in RFIFO (1).

CRC **CRC-Check**
The CRC is correct (1) or incorrect (0).

RAB **Receive Message Aborted**
The receive message was aborted by the remote station (1), i.e. a sequence of 7 1’s was detected before a closing flag.

SA1 – 0 **SAPI-Address Identification**

C/R **Command/Response**
The C/R-bit identifies a receive frame as either a command or a response, according to the LAPD-rules:

Command	Response	Direction
0	1	Subscriber to network
1	0	Network to subscriber

TA **TEI-Address Identification**
SA1 – 0 are significant in auto-mode and non-auto mode with a two-byte address field, as well as in transparent mode 3. TA is significant in all modes except in transparent modes 2 and 3.

Two programmable SAPI-values (SAP1, SAP2) plus a fixed group SAPI (SAPG of value FC/FE_H), and two programmable TEI-values (TEI1, TEI2) plus a fixed group TEI (TEIG of value FF_H), are available for address comparison.

The result of the address comparison is given by SA1-0 and TA, as follows:

				Address Match with	
	SA1	**SA0**	**TA**	**1st Byte**	**2nd Byte**
Number of Address Bytes = 1	x x	x x	0 1	TEI2 TEI1	– –
Number of address bytes = 2	0 0 0 0 1 1 1	0 0 1 1 0 0 1	0 1 0 1 0 1 x	SAP2 SAP2 SAPG SAPG SAP1 SAP1 reserved	TEIG TEI2 TEIG TEI1 or TEI2 TEIG TEI1

Notes:
- If the SAPI-values programmed to SAP1 and SAP2 are identical the reception of a frame with SAP2/TEI2 results in the indication SA1 = 1, SA0-0, TA = 1.
- Normally RSTA should be read by the processor after an RME-interrupt in order to determine the status of the received frame. The contents of RSTA are valid only after an RME-interrupt, and remain so until the frame is acknowledged via the RMC-bit.

SAPI2-Register
Value after reset: xx

Adr.	Bit 7			Bit 0	Reg.	R/W
27	SAPI2		MCS	0	SAP2	W

SAPI2 **SAPI2-value**
Value of the second programmable Service Access Point Identifier (SAPI) according to the ISDN LAPD-protocol.

MCS **Modulo Count Select**. Used in auto-mode only.
This bit determines the HDLC-control field format as follows:
0: One-byte control field (modulo 8)
1: Two-byte control field (modulo 128)

TEI1-Register
Value after reset: xx

Adr.	Bit 7							Bit 0	Reg.	R/W
28	TEI1							EA	TEI1	W

EA **Address Field Extension bit**
This bit is set to “1” according to HDLC/LAPD.

In all message transfer modes except in transparent modes 2 and 3, TEI1 is used by the ISAC-P TE for address recognition. In the case of a two-byte address field, it contains the value of the first programmable Terminal Endpoint Identifier according to the ISDN LAPD-protocol.

In the auto-mode with a two-byte address field, numbered frames with the address SAPI1 – TEI1 are handled autonomously by the ISAC-P TE according to the LAPD-protocol.

Note: If the value FF_H is programmed in TEI1, received numbered frames with address SAPI1 – TEI1 (SAPI1 – TEIG) are not handled autonomously by the ISAC-P TE.

In auto- and non-auto modes with one-byte address field, TEI1 is a command address, according to X.25 LAPB.

Receive HDLC-Control Register
Value after reset: xx

Adr.	Bit 7							Bit 0	Reg.	R/W
29									RHCR	R

In all modes except transparent modes 2 and 3, this register contains the control field of a received HDLC-frame. In transparent modes 2 and 3, the register is not used.

Mode	Contents of RHCR		Contents of RFIFO
	Modulo 8 (MCS = 0)	**Modulo 128 (MCS = 1)**	**Contents of RFIFO**
Auto-mode, 1-byte address (U/I-frames) (Note 1)	Control field	U-frames only: Control field (Note 2)	From 3rd byte after flag (Note 4)
Auto-mode, 2-byte address (U/I-frames) (Note 1)	Control field	U-frames only: Control field (Note 2)	From 4th byte after flag (Note 4)
Auto-mode, 1-byte address (I-frames)		Control field in compressed form (Note 3)	From 4th byte after flag (Note 4)
Auto-mode, 2-byte address (I-frames)		Control field in compressed form (Note 3)	From 5th byte after flag (Note 4)
Non-auto mode, 1-byte address	2nd byte after flag		From 3rd byte after flag
Non-auto mode, 2-byte address	3rd byte after flag		From 4th byte after flag
Transparent mode 1	3rd byte after flag		From 4th byte after flag
Transparent mode 2	–		From 1st byte after flag
Transparent mode 3	–		From 2nd byte after flag

Note 1 S-frames are handled automatically and are not transferred to the microprocessor.

Note 2 For U-frames (bit 0 of RHCR = 1) the control field is as in the modulo 8 case.

Note 3 For I-frames (bit 0 of RHCR = 0) the compressed control field has the same format as in the modulo 8 case, but only the three LSB's of the receive and transmit counters are visible:

Bit	7	6	5	4	3	2	1	0
	N (R)		2 – 0	P	N (S)		2 – 0	0

Note 4 I-field.

TEI2-Register
Value after reset: xx

Adr.	Bit 7							Bit 0	Reg.	R/W
28	TEI2							EA	TEI2	W

EA **Address field Extension bit**
This bit is to be set to “1” according to HDLC/LAPD.

In all message transfer modes except in transparent modes 2 and 3, TEI2 is used by the ISAC-P TE for address recognition. In the case of a two-byte address field, it contains the value of the second programmable Terminal Endpoint Identifier according of the ISDN LAPD-protocol.

In auto- and non-auto modes with one-byte address field, TEI2 is a response address, according to X.25 LAPD.

Receive Frame Byte Count High
Value after reset: 0xxx00002

Adr.	Bit 7							Bit 0	Reg.	R/W
2A	XAC	VN1	VN0	OV	RBC11	RBC10	RBC9	RBC8	RBCH	R

XAC **Transmitter Active**
The HDLC-transmitter is active when XAC = 1. This bit may be polled.
The XAC-bit is active when

– either an XTF/XIF-command is issued and the frame has not been completely transmitted

– or the transmission of an S-frame is internally initiated and not yet completed.

VN1 – 0 **Version Number of Chip**
00 Version V1.4

OV **Overflow**
A “1” in this bit position indicates a message longer than 4095 bytes.

RBC8 – 11 **Receive Byte Count**
Four most significant bits of the total number of bytes in a received message.

Note: Normally RBCH and RBCL should be read by the processor after an RME-interrupt in order to determine the number of bytes to be read from the RFIFO, and the total message length. The contents of the registers are valid only after an RME-interrupt, and remain so until the frame is acknowledged via the RMC-bit.

Status Register 2
Value after reset: 0x

Adr.	Bit 7							Bit 0	Reg.	R/W
2B	0	0	0	0	WFA	0	TREC	SDET	STAR2	R

SDET **S-frame Detected:** This bit is set to “1” by the first received correct I-frame or S-command with p = 1.
It is reset by reading the STAR2-register.

TREC **Timer Recovery status:**
0: The device is not the Timer Recovery state.
1: The device is in the Timer Recovery state.

WFA **Waiting for Acknowledge:** This bit shows, if the last transmitted I-frame was acknowledged, i.e. V(A) = V(S) (≥ WFA = 0) or was not yet acknowledged, i.e. V(A) < V(S) (≥ WFA = 1).

4.2 ISAC®-P TE Register Summary: Special Purpose Registers

Special Configuration Register
Value after reset: 00_H

Adr.	Bit 7							Bit 0	Reg.	R/W
30	SPU	0	0	TLP	C1C1	C1C0	C2C1	C2C0	SPCR	R/W

Important Note: After a hardware reset the pins SDAX/SDS1 and SCA/FSD/SDS2 are both “low” and have the functions of SDS1 and SDS2 in terminal timing mode (since SPM = 0), respectively, until the SPCR is written to for the first time. From that moment, the function taken on by these pins depends on the state of the IOM-Mode Select bit IMS (ADF2-register).

SPU **Software Power-UP.** Used in TE-mode only.
Setting this bit to “1” and ADF:IDC to “1” will pull the DU-line to low. This will enforce connected layer-1 devices to deliver IOM-clocking.

After power down in TE-mode the SPU-bit and the ADF1:IDC-bit have to be set to “1” and then cleared again.

After a subsequent CIC-interrupt (C/I-code change; ISTA) and reception of the C/I-code “PU” (Power-Up indication in TE-mode) the reaction of the processor would be:

– to write an Activate Request command as C/I-code in the CIX0-register.

– to reset the SPU and ADF1:IDC-bits and wait for the following CIC-interrupt.

TLP **Test Loop**

When set to “1” the DU- and DD-lines are internally connected together, and the times T1 and T2 are reduced (cf. TIMR).

C1C1, C1C0 **Channel 1 Connect**

Determines which of the two channels B1 or IC1 is connected to register C1R and/or B1CR, for monitoring, test-looping and switching data to/ from the processor.

		C1R		B1CR	
C1C1	**C1C0**	**Read**	**Write**	**Read**	**Application(s)**
0	0	IC1	–	B1	B1-monitoring + IC1-monitoring
0	1	IC1	IC1	B1	B1-monitoring + IC1-looping from/to IOM
1	0	–	B1	B1	B1-access from/to S_0; transmission of a constant value in B1-channel to S_0.
1	1	B1	B1	–	B1-looping from S_0; transmission of a variable pattern in B1-channel to S_0.

C2C1, C2C0 **Channel 2 Connect**

Determines which of the two channels B2 or IC2 is connected to register C2R and/or B2CR, for monitoring, test-looping and switching data to/from the processor.

		C2R		B2CR	
C2C1	**C2C0**	**Read**	**Write**	**Read**	**Application(s)**
0	0	IC2	–	B2	B2-monitoring + IC2-monitoring
0	1	IC2	IC2	B2	B2-monitoring + IC2-looping from/to IOM
1	0	–	B2	B2	B2-access from/to S_0; transmission of a constant value in B2-channel to S_0.
1	1	B2	B2	–	B2-looping from S_0; transmission of a variable pattern in B2-channel to S_0.

Note: B-channel access is only possible in TE-mode.

Command/Indicate 0 Status Register

Adr.	Bit 7						Bit 0	Reg.	R/W
31	0	BAS	C	O	D	R0	CIC0	CIC1	CIR0	R

BAS **Bus Access Status**
Indicates the state of the TIC-bus:

0: the ISAC-P TE itself occupies the D- and C/I-channel
1: another device occupies the D- and C/I-channel

CODR0 **C/I-Code 0 Receive**
Value of the received Command/Indication code. A C/I-code is loaded in CODR0 only after being the same in two consecutive IOM-frames and the previous code has been read from CIR0.

CIC0 **C/I-Code 0 Change**
A change in the received Command/Indication code has been recognized. This bit is set only when a new code is detected in two consecutive IOM-frames. It is reset by a read of CIR0.

CIC1 **C/I-Code 1 Change**
A change in the received Command/Indication code in IOM-channel 1 has been recognized. This bit is set when a new code is detected in one IOM-frame. It is reset by a read of CIR0.

CIC1 is only used if Terminal Mode is selected.

Note: The BAS- and CODR0-bits are update every time a new C/I-code is detected in two consecutive IOM-frames.
If several consecutive valid new codes are detected and CIR0 is not read, only the first and the last C/I-code (and BAS-bit) is made available in CIR0 at the first and second read of that register, respectively.

RSS **Reset Source Select**
Only valid if the terminal specific functions are activated (STCR:TSF).

0 → **Subscriber or Exchange Awake**
As reset source serves:
– a C/I-code change (Exchange Awake).

1 → **Watchdog Timer**
The expiration of the watchdog timer generates a reset pulse.

The watchdog timer will be reset and restarted, when two specific bit

Monitor Receive Channel 0

Adr.	Bit 7							Bit 0	Reg.	R/W
32									MOR0	R

Contains the MONITOR data received in IOM-MONITOR Channel/MONITOR channel 0 according to the MONITOR channel protocol.

Monitor Transmit Channel 0

Adr.	Bit 7							Bit 0	Reg.	R/W
32									MOX0	W

Contains the MONITOR data transmitted in IOM-MONITOR Channel/MONITOR channel 0 according to the MONITOR channel protocol.

Command/Indicate 1 Status Register

Adr.	Bit 7							Bit 0	Reg.	R/W
33	C	O	D	R	1		MR1	MX1	CIR1	R

CODR1 **C/I-Code 1 Receive**
Bits 7 – 2 of C/I-channel 1

MR1 **MR-Bit**
Bit 1 of C/I-channel 1

MX1 **MX-Bit**
Bit 0 of C/I-channel 1

Command/Indicate 1 Control Register

Adr.	Bit 7							Bit 0	Reg.	R/W
33	C	O	D	X	1		1	1	CIX1	W

CODX1 C/I Code 1 Transmit

Bit 7 – 2 which are transmitted on C/I-channel 1.

Monitor Receive Channel 1

Adr.	Bit 7							Bit 0	Reg.	R/W
34									MOR1	R

Contains the MONITOR data received in IOM-channel 1 according to the MONITOR channel protocol.

Monitor Transmit Channel 1

Adr.	Bit 7							Bit 0	Reg.	R/W
34									MOX1	W

Contains the MONITOR data transmitted in IOM-channel 1 according to the MONITOR channel protocol.

Channel Register 1

Adr.	Bit 7							Bit 0	Reg.	R/W
35									C1R	R/W

Contains the value received/transmitted in IOM-channel B1 or IC1, as the case may be (cf. C1C1, C1C0, SPCR-register).

Channel Register 2

Adr.	Bit 7							Bit 0	Reg.	R/W
36									C2R	R/W

Contains the value received/transmitted in IOM-channel B2 or IC2, as the case may be (cf. C2C1, C2C0, SPCR-register).

B1 Channel Register

Adr.	Bit 7							Bit 0	Reg.	R/W
37									B1CR	R

Contains the value received in IOM-channel B1, if programmed (cf. C1C1, C1C0, SPCR-register).

Synchronous Transfer Control Register
Value after reset: 00_H

Adr.	Bit 7							Bit 0	Reg.	R/W
37	TSF	TBA2	TBA1	TBA0	ST1	ST0	SC1	SC0	STCR	W

TSF **Terminal Specific Functions**
Enables the feature of the RSS-bit.

Note: TSF-bit will be cleared only by a hardware reset.

TBA2 – 0 **TIC-Bus Address**
Defines the individual TIC-bus address for the ISAC-P TE on the IOM-2 interface. This address is used to access the C/I- and D-channel on the IOM-2 interface.

ST1 **Synchronous Transfer 1**
When set, causes the ISAC-P TE to generate an SIN-interrupt status (ISTA-register) at the beginning of an IOM-2 frame.

ST0 **Synchronous Transfer 0**
When set, causes the ISAC-P TE to generate an SIN-interrupt status (ISTA-register) at the middle of the IOM-2 frame.

SC1 **Synchronous Transfer 1 Completed**
After an SIN-interrupt the processor has to acknowledge the interrupt by setting the SC1-bit before the middle of the IOM-2 frame, if the interrupt was originated from the Synchronous Transfer 1 (ST1).
Otherwise an SOV-interrupt (EXIR-register) will be generated.

SC0 **Synchronous Transfer 0 Completed**
After an SIN-interrupt the processor has to acknowledge the interrupt by setting the SC0-bit before the start of the next IOM-2 frame, if the interrupt was originated from the Synchronous Transfer 0 (ST0).
Otherwise an SOV-interrupt (EXIR-register) will be generated.

Note: ST0/1 and SC0/1 are useful for synchronizing µP-accesses and receive/transmit operations.

B2 Channel Register

Adr.	Bit 7							Bit 0	Reg.	R/W
38									B2CR	R

Contains the value received in the IOM-channel B2, if programmed (cf. C2C1, C2C0, SPCR-register).

Additional Feature 1 Register
Value after reset: 00_H

Adr.	Bit 7							Bit 0	Reg.	R/W
38	WTC1	WTC2	CI1E	IDC	IOF	0	0	ITF	ADF1	W

WTC1 – 2 **Watchdog Timer Control 1, 2**
After the watchdog timer mode has been selected (STCR:TSF = 1, CIX0:RSS = 1) the watchdog timer is started.

During every time period of 128 ms the processor has to program the WTC1- and WTC2-bit in the following sequence to reset and restart the watchdog timer:

	WTC1	WTC2
1.	1	0
2.	0	1

If the watchdog timer expires, a reset pulse of 125 µs is generated. In the EXIR-register, the WOV-bit is set to distinguish between V_{DD} reset and watchdog reset. Registers are not affected by the watchdog reset.

CI1E **C/I1-Interrupt Enable**
0: C/I1 changes will not generate a CIC-status
1: C/I1 changes generate a CIC-status

IDC **IOM-Direction Control**
0: IOM-master mode
1: IOM-slave mode (IDP0, IDP1 crossed during IOM-channel 1)

IOF **IOM OFF**
Controls the IOM-2 interface signals
0: IOM-2 operating
1: IOM-2 interface turned off. FSC, DCL, DU, DD, BCL are high impedance

ITF **Interface Time Fill**
Selects the interframe time fill signal which is transmitted between HDLC-frames.
0: Idle (continuous “1”)
1: Flags (sequence of pattern: “01111110”)

Note: In applications together with the ELIC or other TIC-bus devices it is necessary to set the ITF-bit to “0”.

Additional Feature 2 Register
Value after reset: 00_H

Adr.	Bit 7							Bit 0	Reg.	R/W
39	IMS	D2C2	D2C1	D2C0	ODS	D1C2	D1C1	D1C0	ADF2	R/W

IMS **IOM-Mode Select**
Must be set to “1” after reset for IOM-2 interface configuration.

D2C2 – 0 **Data Strobe Control**

D1C2 – 0 These bits determine the polarity of the two independent strobe signals SDS1 and SDS2 as follows:

DxC2	DxC1	DxC0	SDSx
0	0	0	always low
0	0	1	high during B1
0	1	0	high during B2
0	1	1	high during B1 + B2
1	0	0	always low
1	0	1	high during IC1
1	1	0	high during IC2
1	1	1	high during IC1 + IC2

The strobe signals allow standard combos or data devices to access a programmable channel.

ODS **Output Driver Select**
0: IOM-output drivers are open drain
1: IOM-output drivers are push-pull

Monitor Channel Status Register
Value after reset: 00_H

Adr.	Bit 7							Bit 0	Reg.	R/W
3A	MDR1	MER1	MDA1	MAB1	MDR0	MER0	MDA0	MAB0	MOSR	R

MDR1 **MONITOR Channel 1 Data Received**
The MONITOR channel handler has received a valid byte.

MER1 **MONITOR Channel 1 End of Reception**
The MONITOR channel handler has detected the end of reception condition (MR = 011).

MDA1 **MONITOR Channel 1 Data Acknowledged**
The MONITOR channel handler has detected the acknowledgement of the opposite station (MR = 110 or 010).

MAB1 **MONITOR Channel 1 Data Abort**
The MONITOR channel handler has detected an abort condition (MR = 011).

MDR0 **MONITOR Channel 0 Data Received**
The MONITOR channel handler has received a valid byte.

MER0 **MONITOR Channel 0 End of Reception**
The MONITOR channel handler has detected the end of reception condition (MR = 011).

MDA0 **MONITOR Channel 0 Data Acknowledged**
The MONITOR channel handler has detected the acknowledgement of the opposite station (MR = 110 or 010).

MAB0 **MONITOR Channel 0 Data Abort**
The MONITOR channel handler has detected an abort condition (MR = 011).

Monitor Channel Configuration Register
Value after reset: 00_H

Adr.	Bit 7							Bit 0	Reg.	R/W
3A	MRE1	MRC1	MIE1	MXC1	MRE0	MRC0	MIE0	MXC0	MOCR	W

MRE1 **Monitor Receive Interrupt Enable 1**
Monitor interrupt status MDR1-generation is enabled (1) or masked (0).

MRC1 **MR-Control Bit**

Determines the value of the MR-bit:

0: MR always “1”. In addition, the MDR1-interrupt is blocked except for the first byte of a packet if MRE1 is “1”.

1: MR internally controlled by the ISAC-P TE according to the Monitor channel protocol. In addition, the MDR1-interrupt is enabled for all received bytes according to the Monitor channel protocol (if MRE1 = 1).

MIE1 **Monitor Channel Interrupt Enable**

Monitor interrupt status MER1, MDA1 and MAB1 generation is enabled (1) or masked (0).

MXC1 **Monitor Channel Transmit Control**

Determines the value of the MX-bit:

0: MX always “1”.

1: MX internally controlled by the ISAC-P TE according to the monitor channel protocol.

MRE0 **Monitor Receive Interrupt Enable 0**

Monitor interrupt status MDR0 generation is enabled (1) or masked (0).

MRC0 **MR-Control Bit**

Determines the value of the MR-bit:

0: MR always “1”. In addition, the MDR0-interrupt is blocked except for the first byte of a packet if MRE0 is “1”.

1: MR internally controlled by the ISAC-P TE according to the monitor channel protocol. In addition, the MDR0-interrupt is enabled for all received bytes according to the monitor channel protocol (if MRE0 = 1).

MXC0 **Monitor Channel Transmit Control**

Determines the value of the MX-bit:

0: MX always “1”.

1: MX internally controlled by the ISAC-P TE according to the monitor channel protocol.

MIE0 **Monitor Channel Interrupt Enable**

Monitor interrupt status MER0, MDA0 and MAB0 generation is enabled (1) or masked (0).

General Configuration Register

Value after reset: 00_H

Adr.	Bit 7							Bit 0	Reg.	R/W
2C	BCS	LLC	PUR	SDO	TCM	LEM	PR1	PR0	GCR	W

BCS **B-Channel Switching during remote test loop**

Controls the switching of the received B-channel information onto the IOM-2 interface during remote test loop condition.

0: B1, B2 switched transparent

1: B1, B2 transmit “1” on DD during remote test loop

LLC **LED- and LCD-Control**

This bit selects the operation of the SDS1/LEDC1, SDS2/LEDC2 and BCL/LEDC3/L6 pin and the LED-matrix and LCD-contrast control function.

0: SDS1, SDS2, BCL selected. LED and LCD off (reset value)

1: LEDC1, LEDC2, LEDC3/L6 selected, LED and LCD active

PUR **Pull-Up Resistors**

Controls the pull-up resistors on the address data bus.

0: pull-up’s are active (reset value)

1: pull-up’s are inactive

SDO **SDO-Control**

Controls the SDO-output in parallel microprocessor mode.

0: SDO is “0”

1: SDO is “1”

TCM **T-Channel Mapping**

0: T-channel data is mapped onto the S/G-bit (S/G = inverse T-channel)

1: T-channel data is mapped onto the A/B-bit (A/B = T-channel)

LEM **LED-Interface Mode**

0: 4×4 LED-matrix selected

1: 6×4 LED-matrix selected

PR1 – 0 **Prescaler**

Determine the clock frequency of the MCLK-output.

0 0 3.84 MHz

0 1 7.68 MHz

1 0 0.48 MHz

1 1 0.96 MHz

Adr.	Bit 7							Bit 0	Reg.	R/W
2C			SCLK	SDI					GCR	R

SCLK **SCLK-Status**
Represents the status of the SCLK-input in parallel microprocessor mode
0: SCLK is “0”
1: SCLK is “1”

SDI **SDI-Status**
Represents the status of the SDI-input in parallel microprocessor mode
0: SDI is “0”
1: SDI is “1”

Note: Status change on SCLK and SDI do not generate an interrupt.

LCD-Contrast Control Register
Value after reset: 00_H

Adr.	Bit 7							Bit 0	Reg.	R/W
2D					LCON3	LCON2	LCON1	LCON0	LCCR	R/W

LCON3 – 0 **LCD-Contrast Control**
Determine the pulse width of the PMW-output for contrast control.

0000 OFF
0001 Pulse of 1/15 period
…
1110 Pulse of 14/15 period
1111 ON

LED-Registers
Value after reset: 00_H

Adr.	Bit 7							Bit 0	Reg.	R/W
3C	L2C4	L2C3	L2C2	L2C1	L1C4	L1C3	L1C2	L1C1	LER0	R/W
3D	L4C4	L4C3	L4C2	L4C1	L3C4	L3C3	L3C2	L3C1	LER1	R/W
3E	L6C4	L6C3	L6C2	L6C1	L5C4	L5C3	L5C2	L5C1	LER2	R/W

LxCy **LED-Control**
Each bit represents the on/off state of the corresponding LED.
0: LED OFF
1: LED ON

x indicates the line number (LEDL1 … LEDL6)
y indicates the column number (LEDC1 … LEDC4)

5 Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Maximum voltage on V_{DD}	V_{DD}	6	V
Voltage on any pin with respect to ground	V_S	– 0.4 to V_{DD} + 0.4	V
Ambient temperature under bias	T_A	0 to 70	°C
Storage temperature	T_{stg}	– 65 to 125	°C

Line Overload Protection

The maximum input current (under voltage conditions) is given as a function to the width of a rectangular input current pulse.

For the destruction current limits refer to **figure 49**.

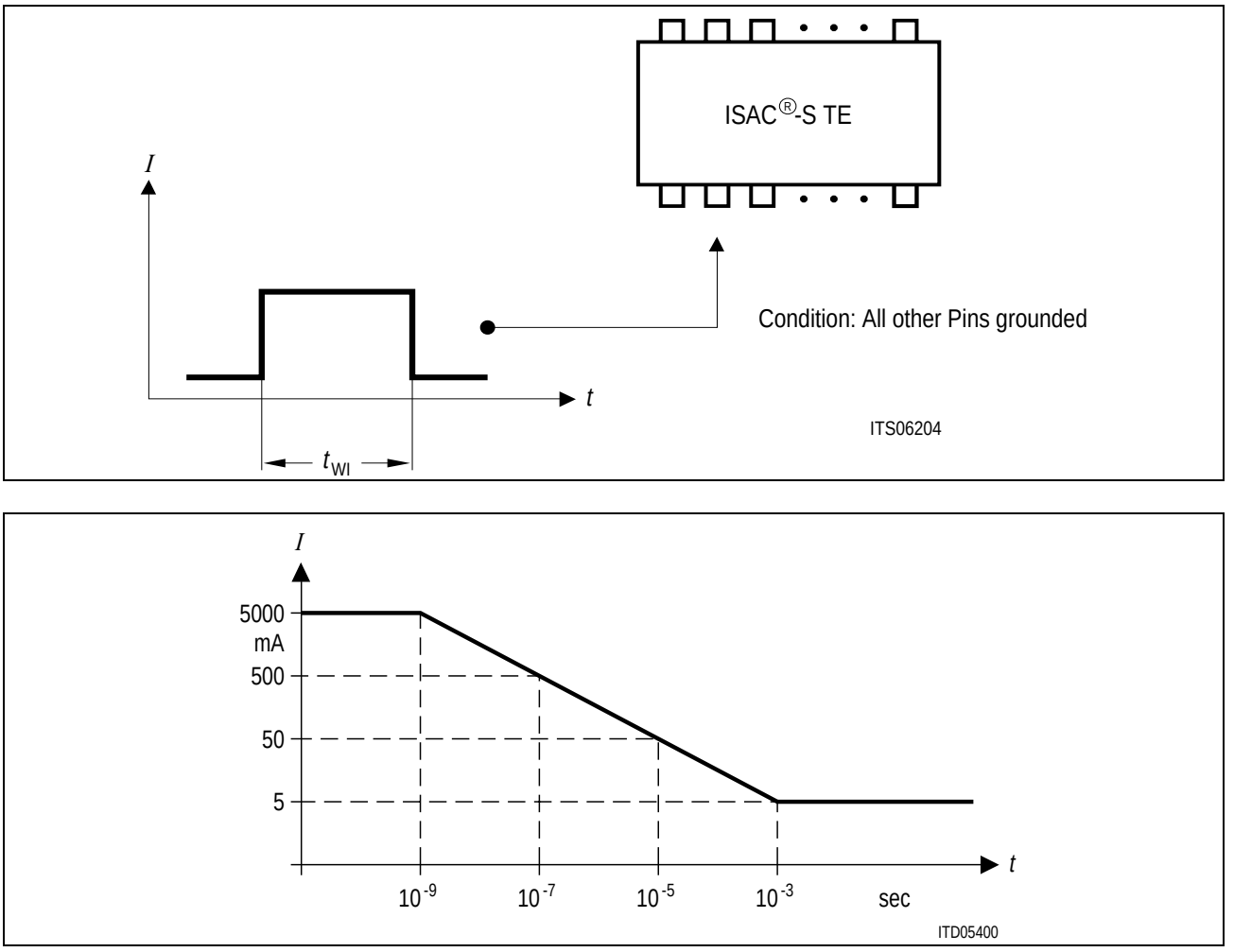


Figure 49
Maximum Line Input Current

DC-Characteristics

T_A = 0 to 70 °C; V_{DD} = 5 V ± 5 %, V_{SS} = 0 V

Parameter	Symbol	Limit Values		Unit	Test Condition	Remarks
		min.	max.			
L-input voltage	V_{IL}	– 0.4	0.8	V		All pins except Lla, Llb, XTAL1
H-input voltage	V_{IH}	2.0	V_{DD} + 0.4	V		All pins except Lla, Llb, XTAL2
L-output voltage L-output voltage 1	V_{OL} V_{OL1}		0.45 0.45	V V	I_{OL} = 2 mA I_{OL} = 7 mA (DD, DU only)	All pins except Lla, Llb, XTAL2
H-output voltage	V_{OH} V_{OH1}	2.4 V_{DD} – 0.5		V V	I_{OH} = – 400 µA I_{OH} = – 100 µA	All pins except Lla, Llb, XTAL2, INT[1], RES –[1], SDO[1], DU[2], DD[2], LEDL1-4
H-output voltage	V_{OH}	V_{DD} – 1.0		V	I_{OH} = – 12 mA	LEDL1-4

Note 1: Not applicable because of open drain output driver.
Note 2: Applicable for push-pull operation only.

DC-Characteristics (cont'd)

Parameter	Symbol	Limit Values		Unit	Test Condition	Remarks
		min.	max.			
Power supply current	I_{CC}		20	mA	DCL = 1.536 MHz	V_{DD} = 5 V, inputs at V_{SS}/V_{DD}, no output loads except Lla, Llb; Lla, Llb load ± 15 mA
Input leakage current Output leakage current	I_{LI} I_{LO}		1[1)] 1[1)]	µA µA	0 V < V_{IN} < V_{DD} 0 V < V_{OUT} < V_{DD}	All pins except Lla, Llb
Transmitter output impedance		10	30	Ω	I_{OUT} = 20 mA	Lla, Llb
Receiver input impedance		20		kΩ	V_{DD} = 5 V, transmitter inactive	Lla, Llb
H-input voltage L-input voltage	V_{IH} V_{IL}	3.5 – 0.4	V_{DD} + 0.4 1.5	V V		XTAL1
H-output voltage L-output voltage	V_{OH} V_{OL}	V_{DD} – 0.5	 0.45	V V	I_{OH} = 100 µA, C_L ≤ 60 pF I_{OL} = 100 µA, C_L ≤ 60 pF	XTAL2

Note 1: Values are valid after disconnecting the internal pull-up resistors.

Capacitances

T_A = 0 to 70 °C; V_{DD} = 5 V ± 5 %, V_{SS} = 0 V

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Input capacitance I/O-capacitance	C_{IN} $C_{I/O}$		7 7	pF pF	All pins except Lla, Llb
Output capacitance	C_{OUT}		10	pF	Lla, Llb
Load capacitance	C_{LD}		60	pF	XTAL1, XTAL2

Oscillator Circuits

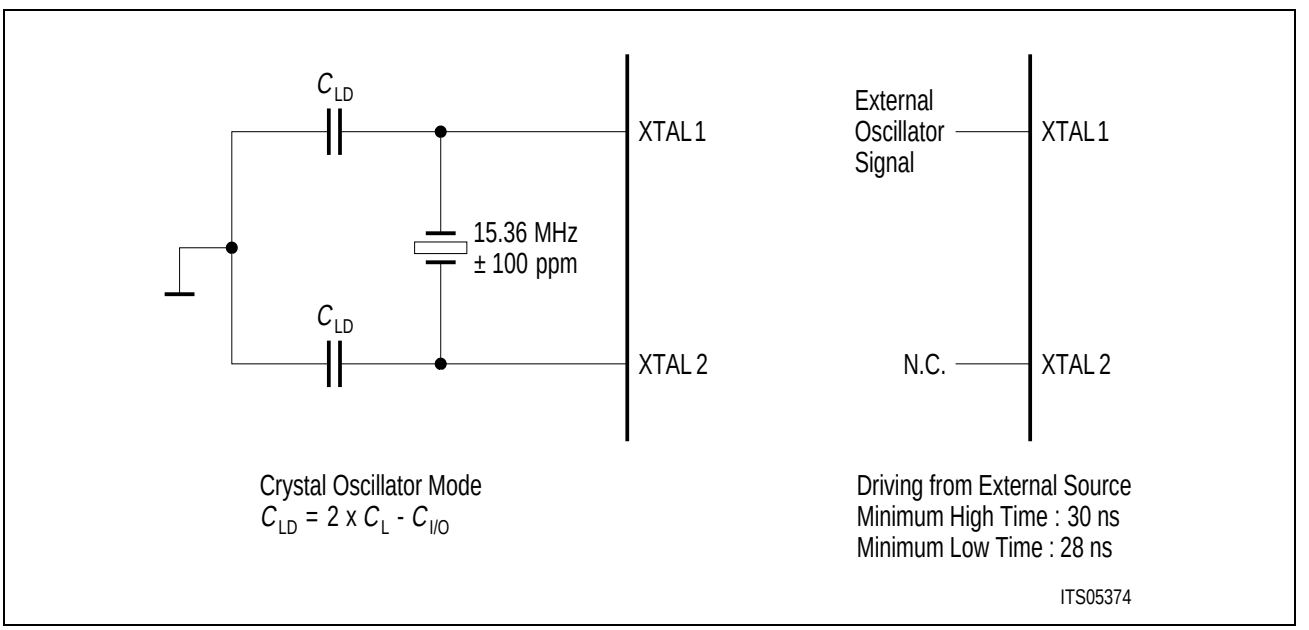


Figure 50
Oscillator Circuits

XTAL1,2 Recommended **typical** crystal parameters.

Parameter	Symbol	Limit Values	Unit
Motional capacitance	C_1	20	fF
Shunt	C_0	7	pF
Load	C_L	≤ 30	pF
Resonance resistor	R_r	≤ 65	Ω

AC-Characteristics

T_A = 0 to 70 °C; V_{DD} = 5 V ± 5 %, V_{SS} = 0 V

Inputs are driven to 2.4 V for a logical “1” and to 0.45 V for a logical “0”. Timing measurements are made at 2.0 V for a logical “1” and 0.8 V for a logical “0”. The AC testing input/output waveforms are shown below.

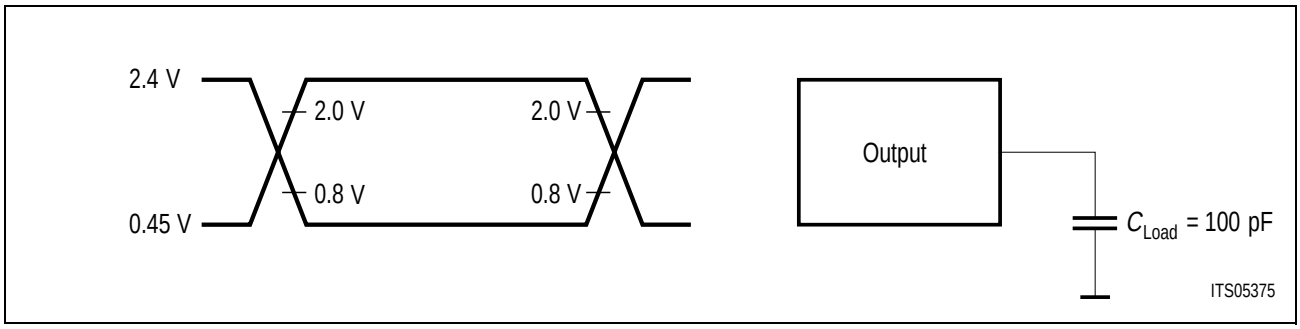


Figure 51
Input/Output Waveforms for AC-Tests

Multiplexed Address Timing

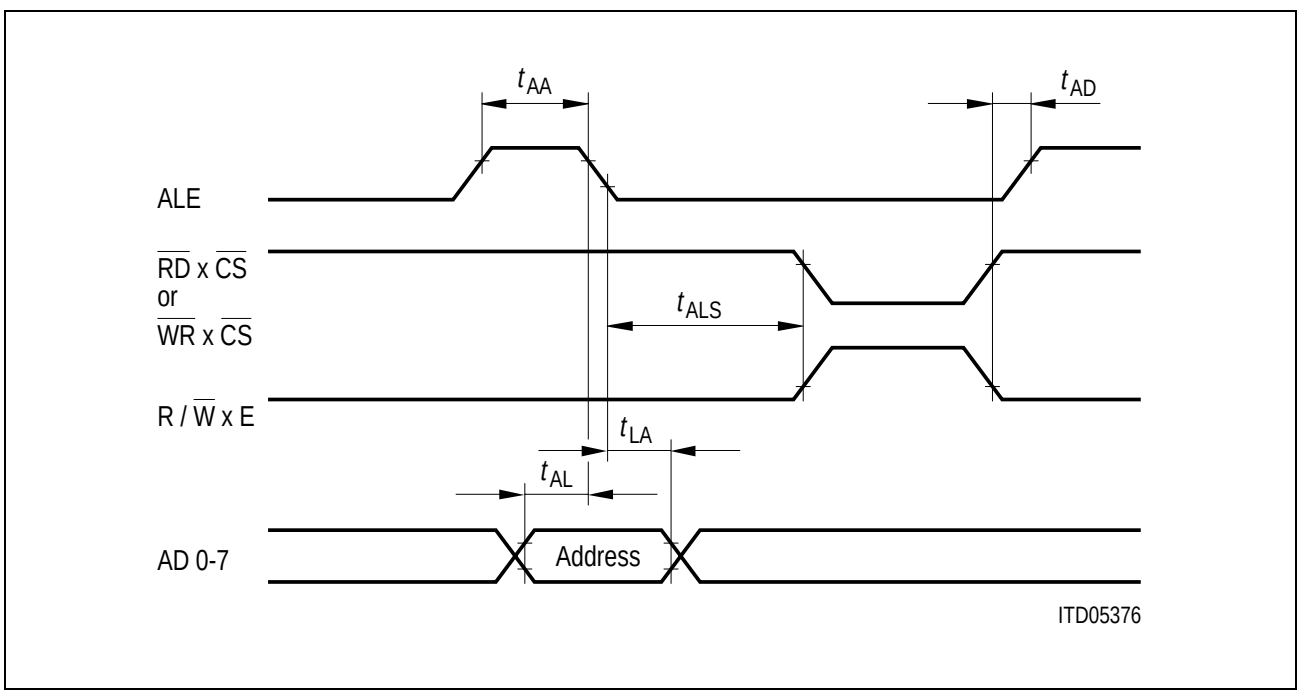


Figure 52
Multiplexed Address Timing

Note: $\overline{RD} \times \overline{CS}$, $\overline{WR} \times \overline{CS}$ applies to Siemens/Intel mode, R/$\overline{W} \times$ E applies to Motorola mode

Siemens/Intel Bus Mode

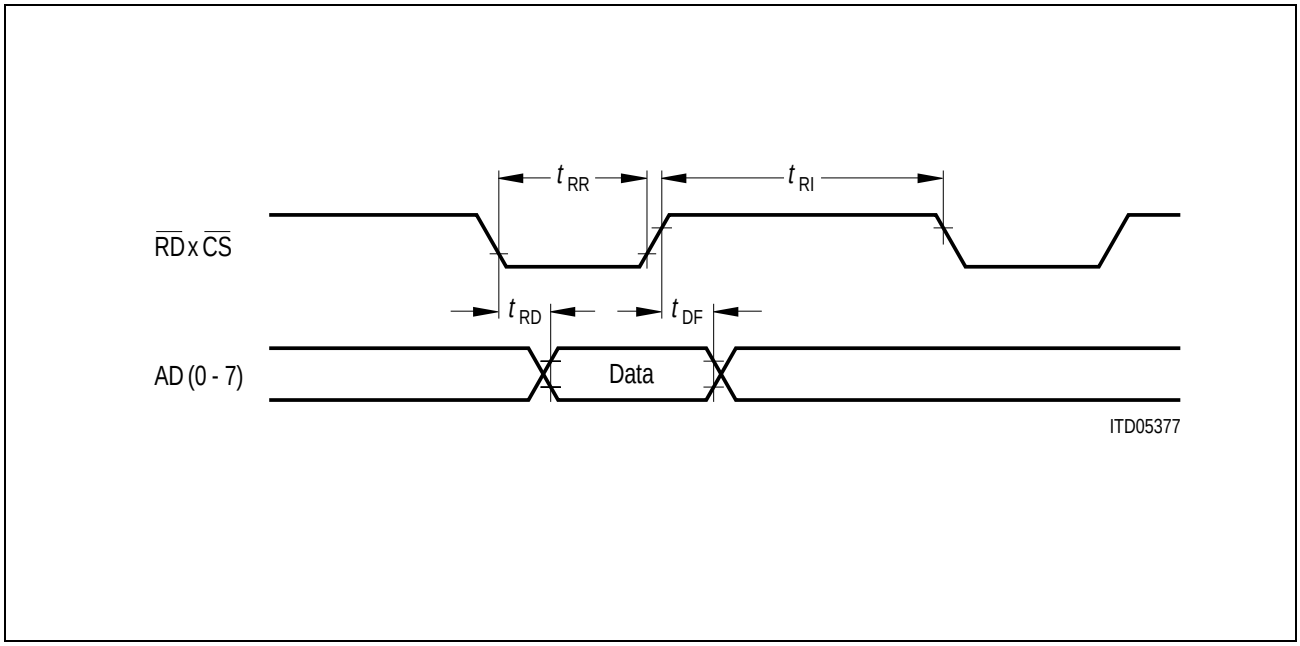


Figure 53
Microcontroller Read Cycle

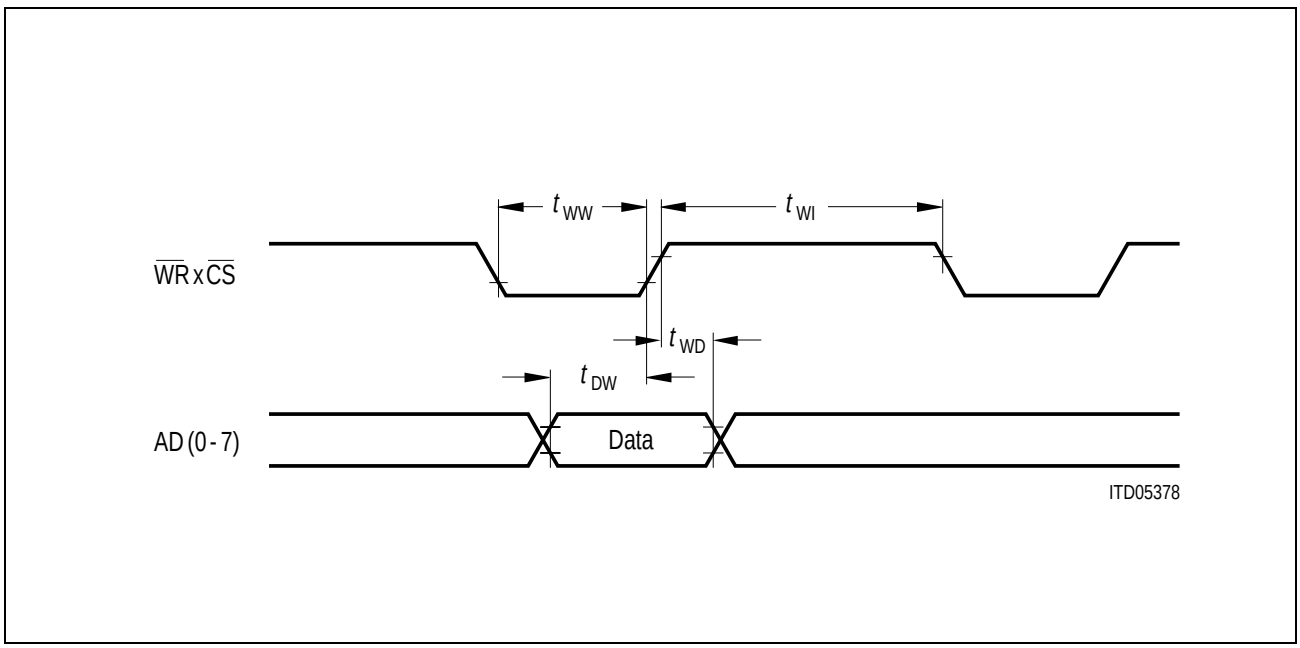


Figure 54
Microcontroller Write Cycle

Motorola Bus Mode

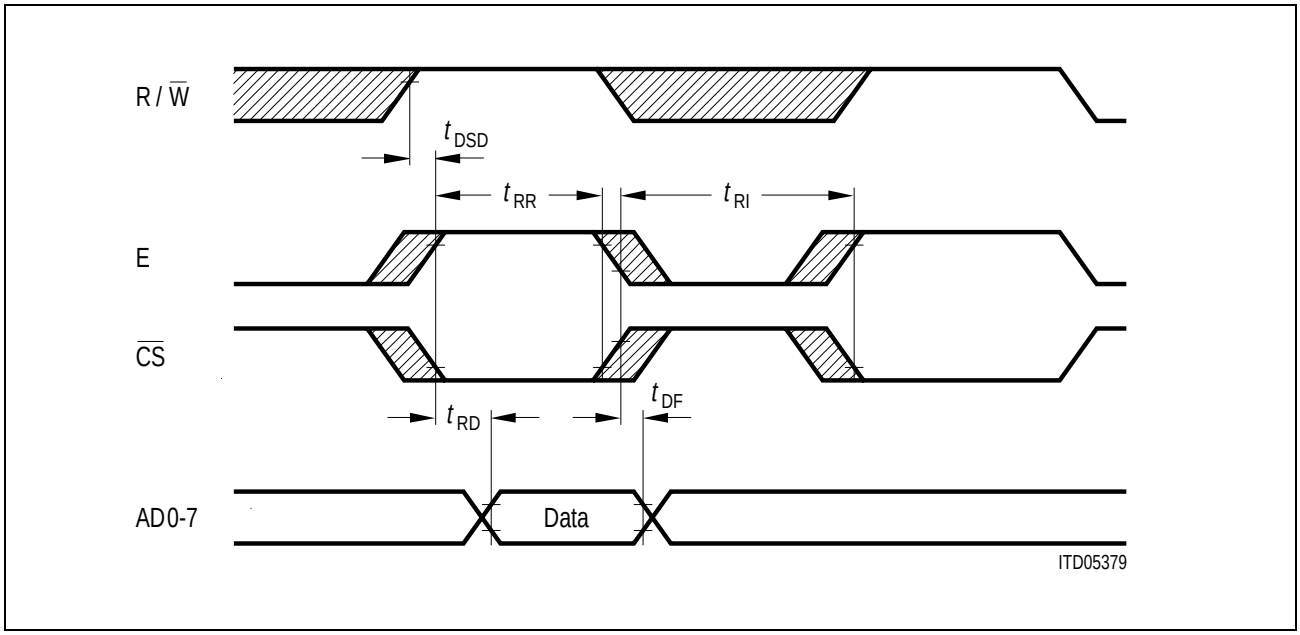


Figure 55
Microcontroller Read Cycle

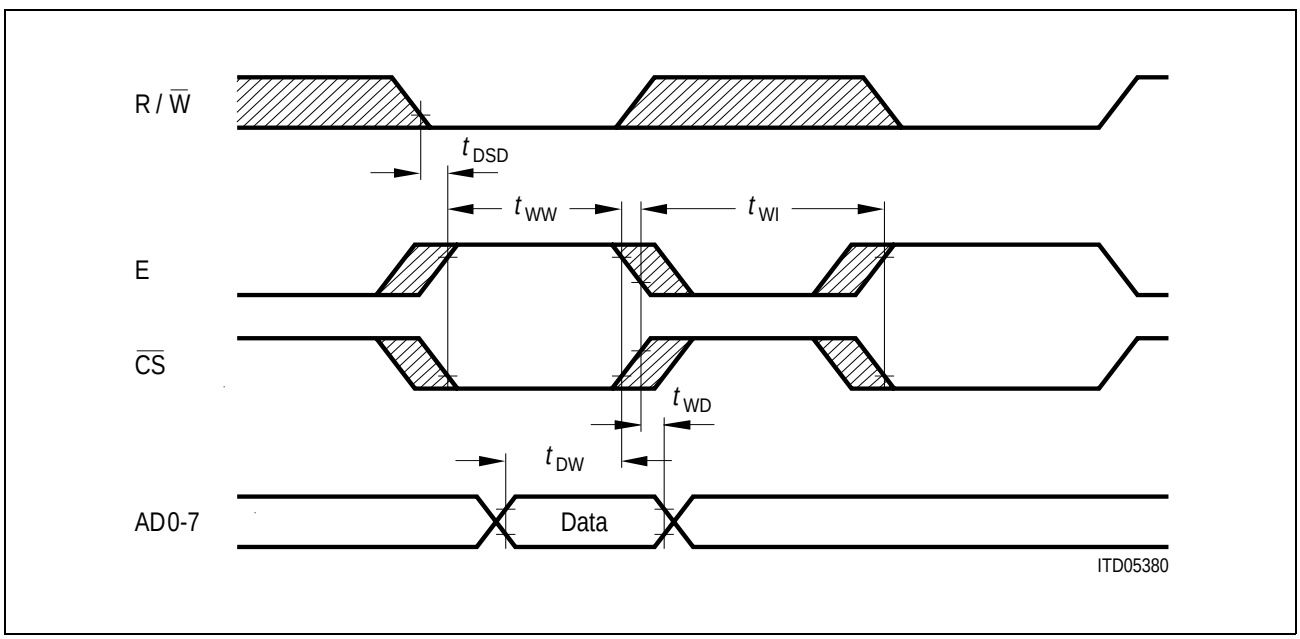


Figure 56
Microcontroller Write Cycle

Microcontroller Interface Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
ALE-pulse width	t_{AA}	50		ns
Address setup time to ALE	t_{AL}	15		ns
Address hold time from ALE	t_{LA}	10		ns
Address latch setup time to $\overline{WR}$, $\overline{RD}$	t_{ALS}	0		ns
ALE-guard time	t_{AD}	15		ns
E delay after R/$\overline{W}$-setup	t_{DSD}	0		ns
$\overline{RD}$-pulse width	t_{RR}	110		ns
Data output delay from $\overline{RD}$	t_{RD}		110	ns
Data float from $\overline{RD}$	t_{DF}		25	ns
$\overline{RD}$-control interval	t_{RI}	70		ns
$\overline{WR}$-pulse width	t_{WW}	60		ns
Data setup time to $\overline{WR} \times \overline{CS}$, E $\times$ $\overline{CS}$	t_{DW}	35		ns
Data hold time from $\overline{WR} \times \overline{CS}$, E $\times$ $\overline{CS}$	t_{WD}	10		ns
$\overline{WR}$-control interval	t_{WI}	70		ns

Serial Control Port Timing

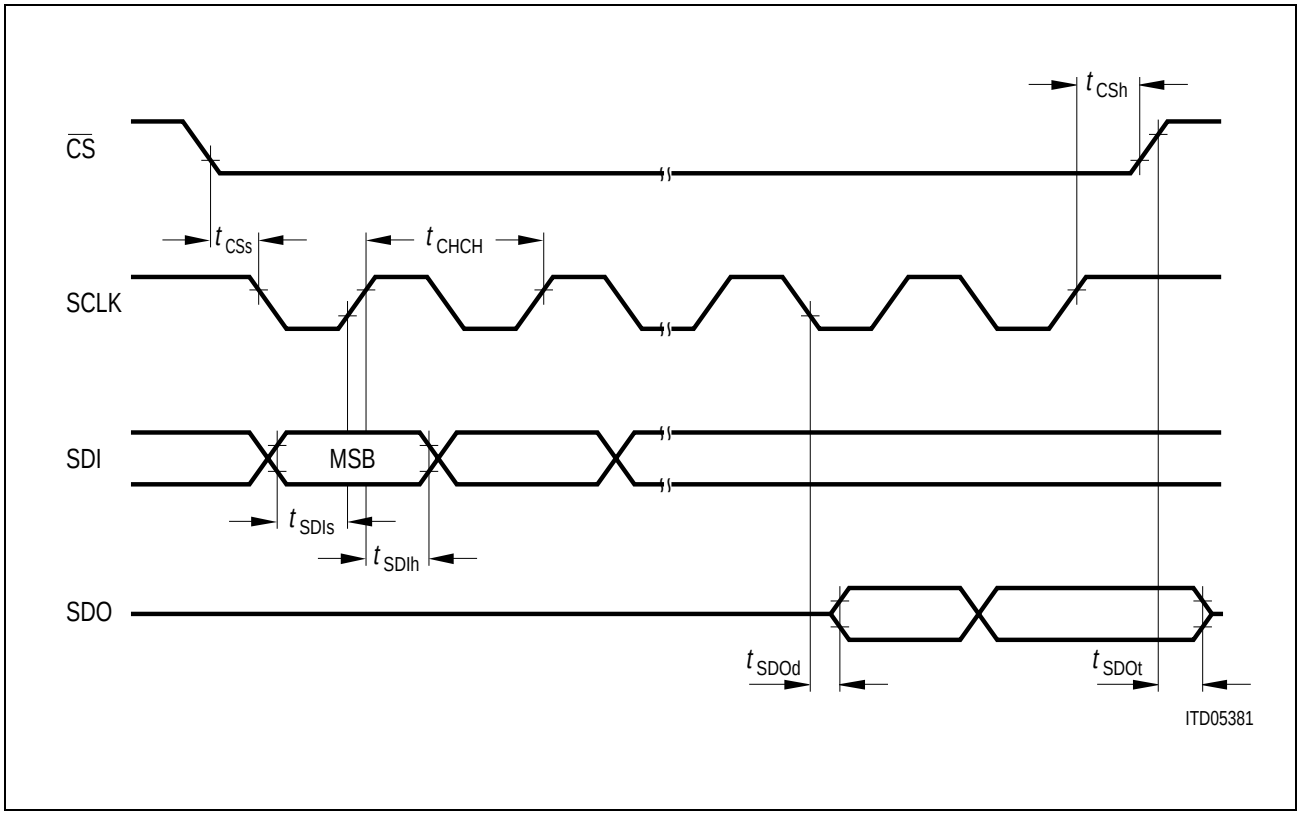


Figure 57
SCP-Switching Characteristics

Parameter	Symbol	Limit Values		Unit
		min.	max.	
SCLK-frequency	t_{CHCH}	1000		ns
Chip select setup time	t_{CSs}	20		ns
Chip select hold time	t_{CSh}	500		ns
SDI-setup time	t_{SDIs}	50		ns
SDI-hold time	t_{SDIh}	50		ns
SDO-data-out delay	t_{SDOd}		150	ns
SDO/$\overline{CS}$ high to tristate	t_{SDOt}		50	ns

IOM®-2 Bus Switching Characteristics

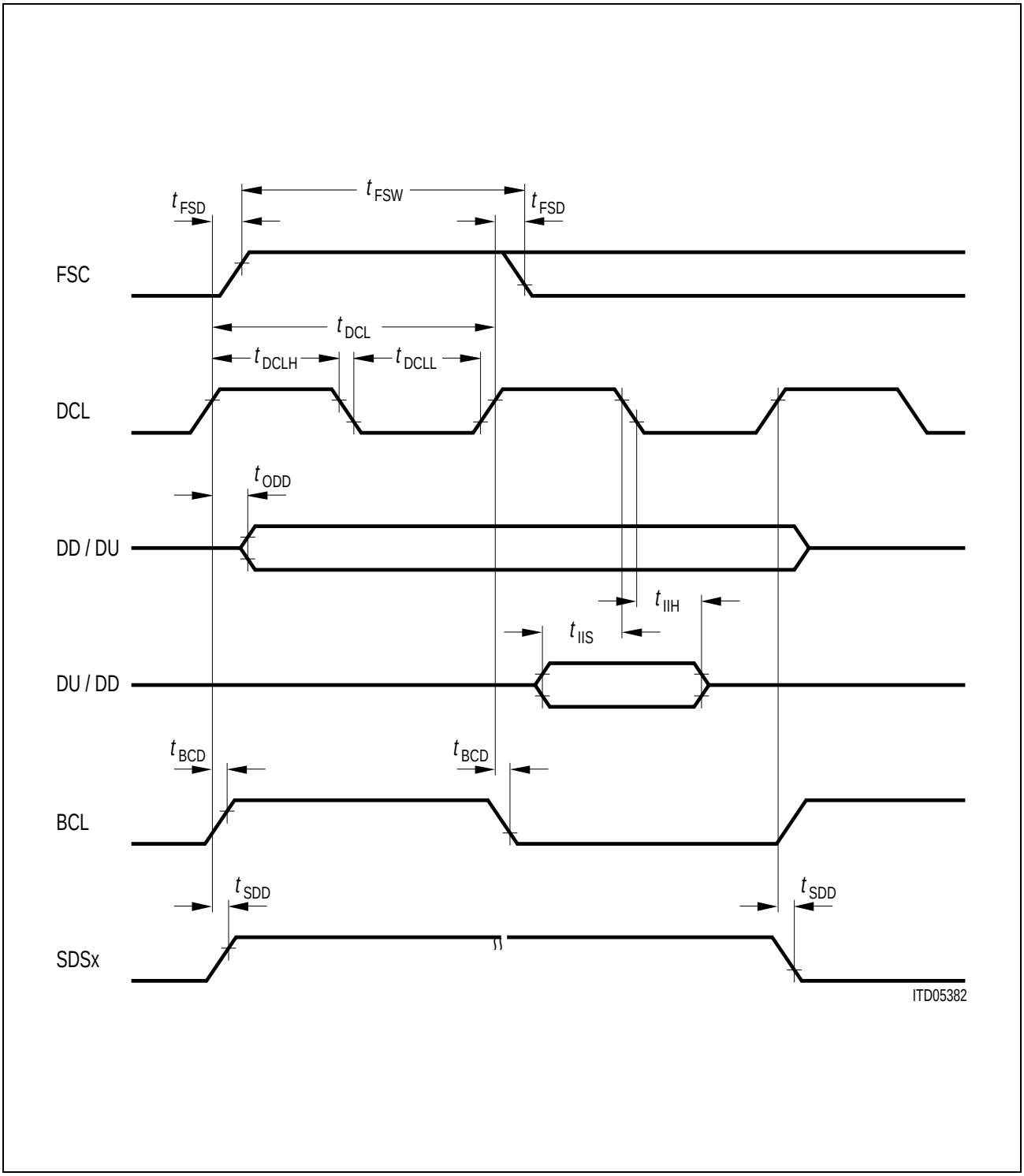


Figure 58
TE-Mode (DCL, FSC output)

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
DCL-clock period (1.536 MHz)	t_{DCL}	585	651	717	ns
DCL-duty cycle		40	50	60	%
DCL-width high	t_{DCLH}	260	326	391	ns
DCL-width low	t_{DCLL}	260	326	391	ns
FSC-period	t_{FSC}		125		µs
FSC-setup delay	t_{FSD}	– 20		20	ns
FSC-width reduced FSC-length (1 DCL) nominal FSC-length (64 DCL)	t_{FSW}	585	651 41.6	717	ns µs
DU/DD-data-in setup time	t_{IIS}	50			ns
DU/DD-data-in hold time	t_{IIH}	50			ns
DU/DD-data-out delay	t_{ODD}			150	ns
Bit clock delay	t_{BCD}	– 20		20	ns
Strobe delay from DCL	t_{SDD}			120	ns

Note: Reduced FSC-length is output every eighth frame triggered by a CV in the received M-bit.

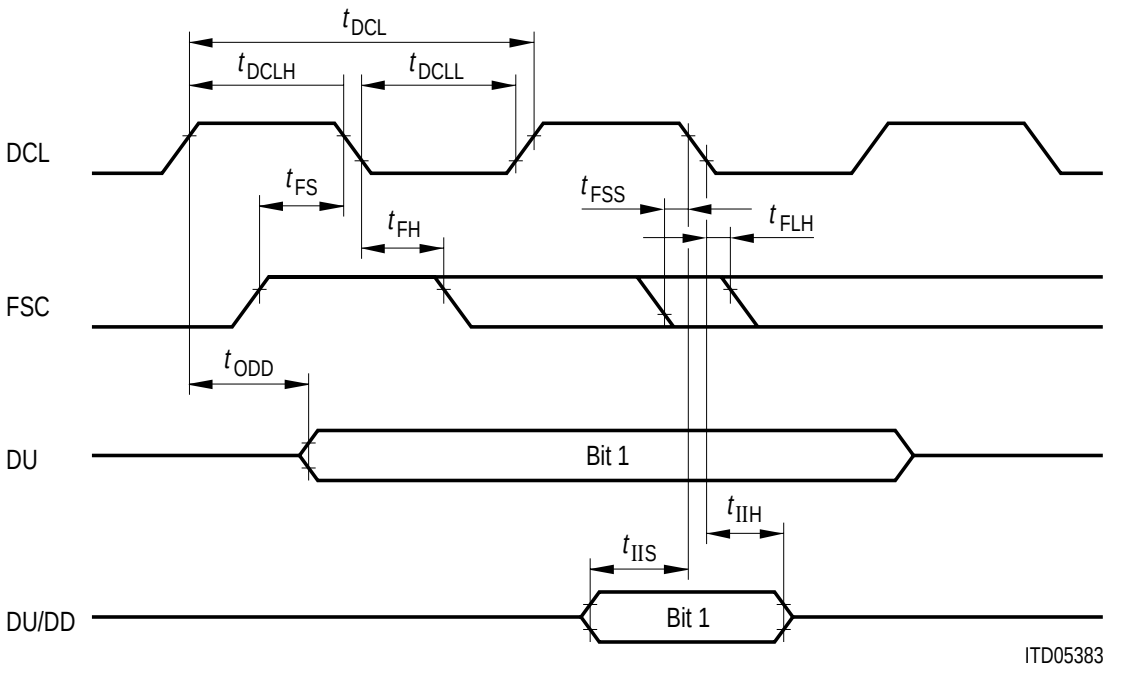


Figure 59
TR-Mode (DCL, FSC input)

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
DCL-clock period (1.536 MHz)	t_{DCL}	488	651	814	ns
DCL-duty cycle		30	50	70	%
DCL-width high	t_{DCLH}	163	326	489	ns
DCL-width low	t_{DCLL}	163	326	489	ns
FSC-period	t_{FSC}		125		µs
FSC-setup time	t_{Fs}	70			ns
FSC-hold time	t_{Fh}	40			ns
FSC-setup short[1)]	t_{FSS}	70			ns
FSC-hold long[2)]	t_{FLH}	40			ns
DU/DD-data-in setup time	t_{IIs}	50			ns
DU/DD-data-in hold time	t_{IIh}	50			ns
DU-data-out delay from DCL	t_{ODD}			150	ns

Notes: 1) Nominal FSC-length = 1 DCL-period (Trigger for M = CV-generation)
2) No trigger for M = CV-generation

MCLK-Timing

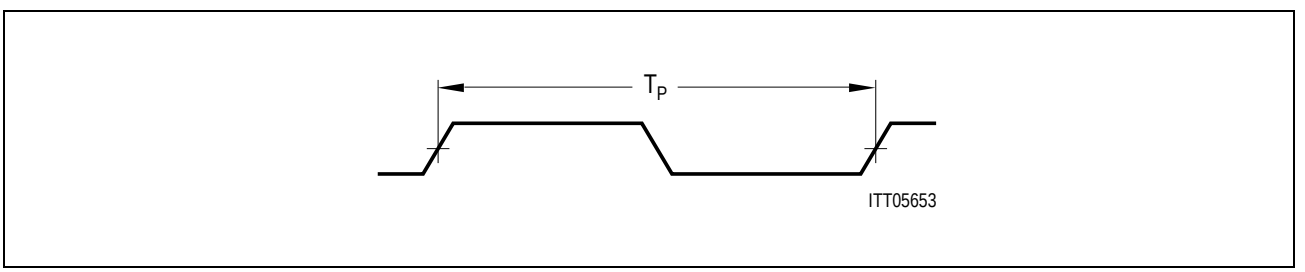


Figure 60
MCLK-Timing

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Clock period 0.48 MHz	T_p		2083		ns
0.96 MHz	T_p		1042		ns
3.84 MHz	T_p		260		ns
7.68 MHz	T_p		130		ns
Duty cycle			50		%

LED-Timing

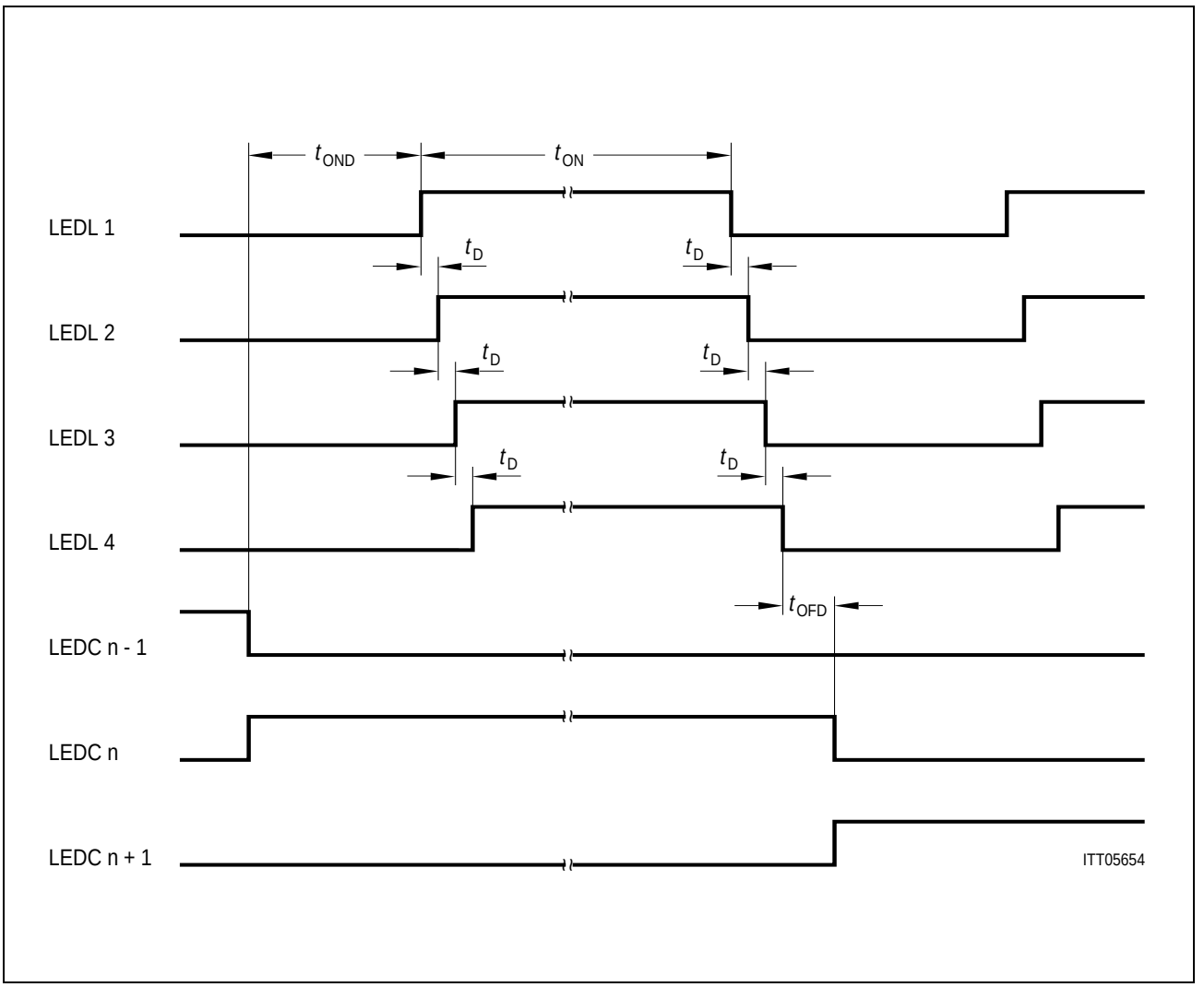


Figure 61
LED-Timing

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Column to line delay	T_{OND}		$10 \times T_D$		
Line to column delay	T_{OFD}		$3 \times T_D$		
ON-period	T_{ON}		2.13		ms
Delay to next line	T_D		130		ns

LCD-Contrast Timing

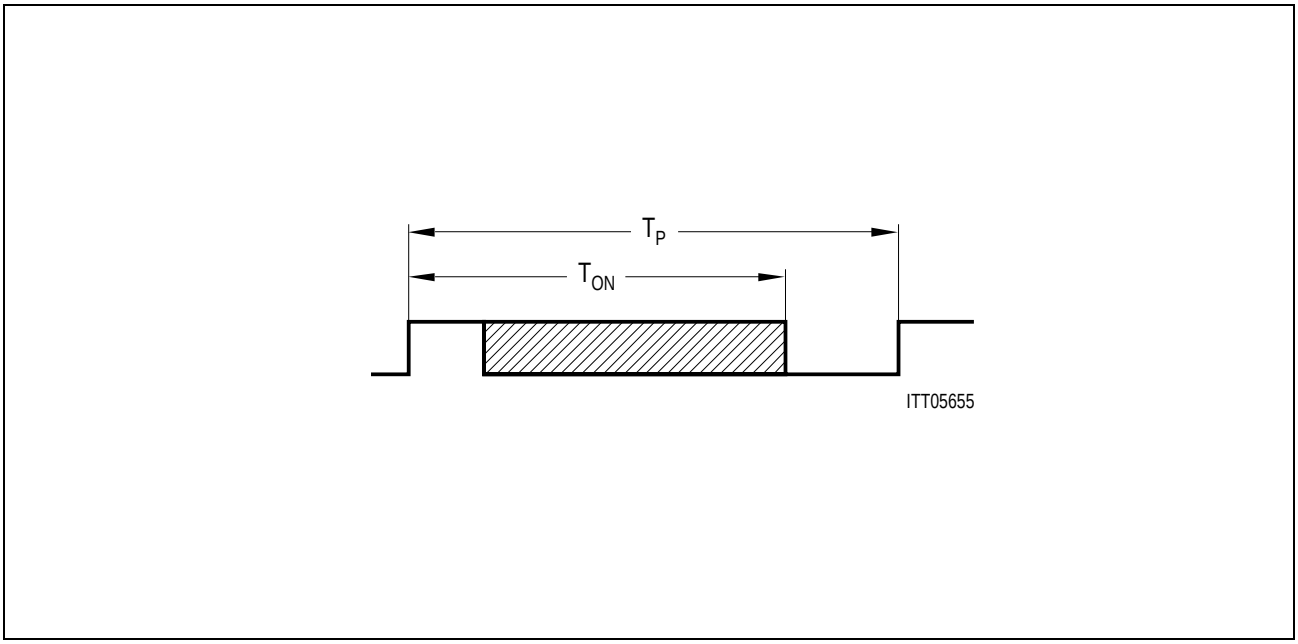
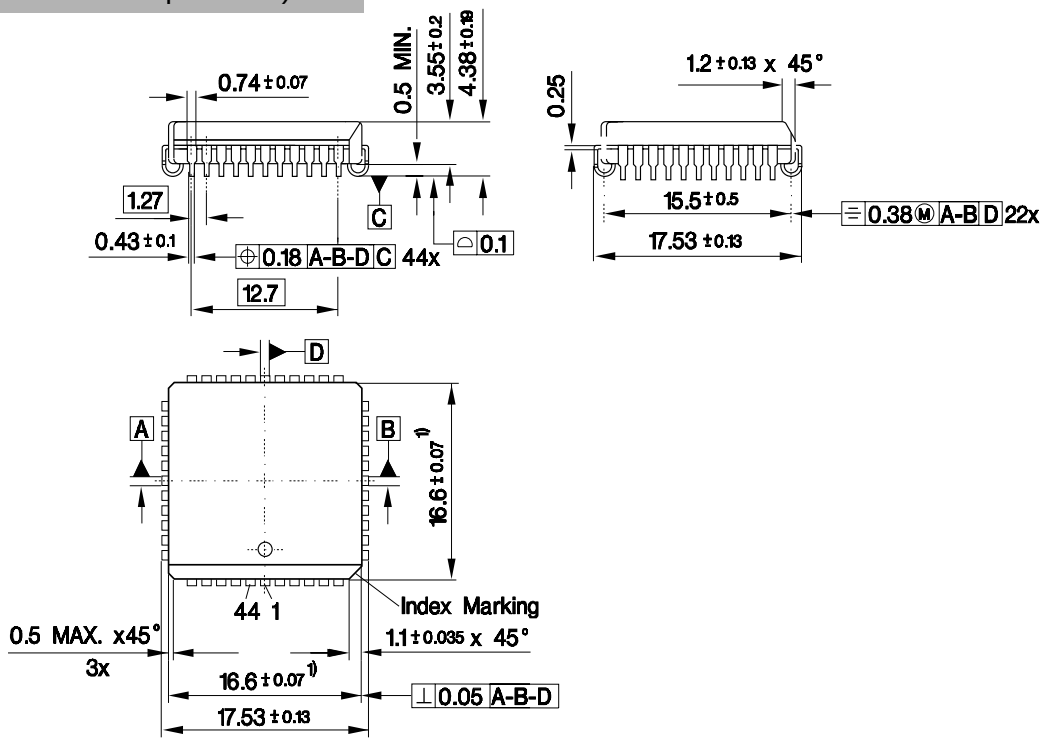


Figure 62
LCD-Contrast Timing

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Repition period	T_p		111.36		µs
ON-period n = 0 … 15	T_{ON}		n × 7.42		µs

6 Package Outlines

Plastic Package, P-LCC-44-1
(Plastic Leaded Chip Carrier)



1) Does not include plastic or metal protrusion of 0.15 max. per side

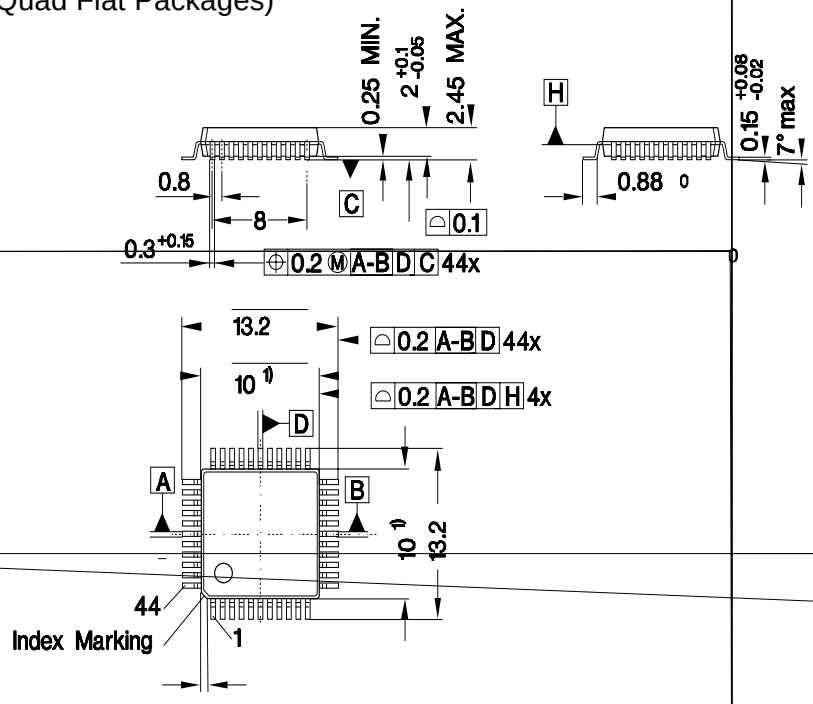
Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”

SMD = Surface Mounted Device

Dimensions in mm

Plastic Package, P-MQFP-44-2

(Plastic Metric Quad Flat Packages)



1) Does not include plastic or metal protrusion of 0.25 max. per side

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our

SMD = Surface Mounted Device„

Data Book "Package Information"

Dimensions in mm