DATA SHEET

SN11121ASF

USB AUDIO Controller

Revision 0.3

I. Description

SONiX SN11121ASF is an USB audio controller. It supports total 3 sampling rates including 32KHz, 44.1KHz and 48KHz in digital/analog playback.

In digital playback mode, it receives audio stream from PC via USB interface and transmits audio data according to the AES/EBU, IEC60958, S/PDIF consumer interface standards. In analog playback mode, it supports 2 channels Codec for analog playback.

Totally one control pipe, one isochronous pipe, and one interrupt pipe are supported by SN11121ASF.

II. Features

- Supports AES/EBU, IEC60958, S/PDIF consumer formats for stereo PCM audio
- 32KHz, 44.1KHz and 48KHz sampling rates for 2 channels playback in digital/analog mode
- Conveys AC-3 data stream by S/PDIF output
- Compatible with Win98 SE/ WinME/ Win2000/ WinXP and MacOS 9.2.1/MacOS10.2 without additional driver
- Plug-and-Play operation with Microsoft OS or MacOS default drivers
- Compliant with USB specification v1.1
- Compliant with USB audio device class specification v1.0
- Supports USB full speed 12Mbits/s serial data transmission
- USB bus power or self power option
- Supports suspend/resume and remote wake-up
- 6MHz crystal input with on-chip PLL and embedded transceiver for USB
- On-chip PLL for synchronized with USB host for CODEC interface
- USB audio function topology has one input terminal, two output terminals, and one feature unit
- Alternate setting0 is a zero-bandwidth setting; used to release the claimed bandwidth on the bus when this device is inactive

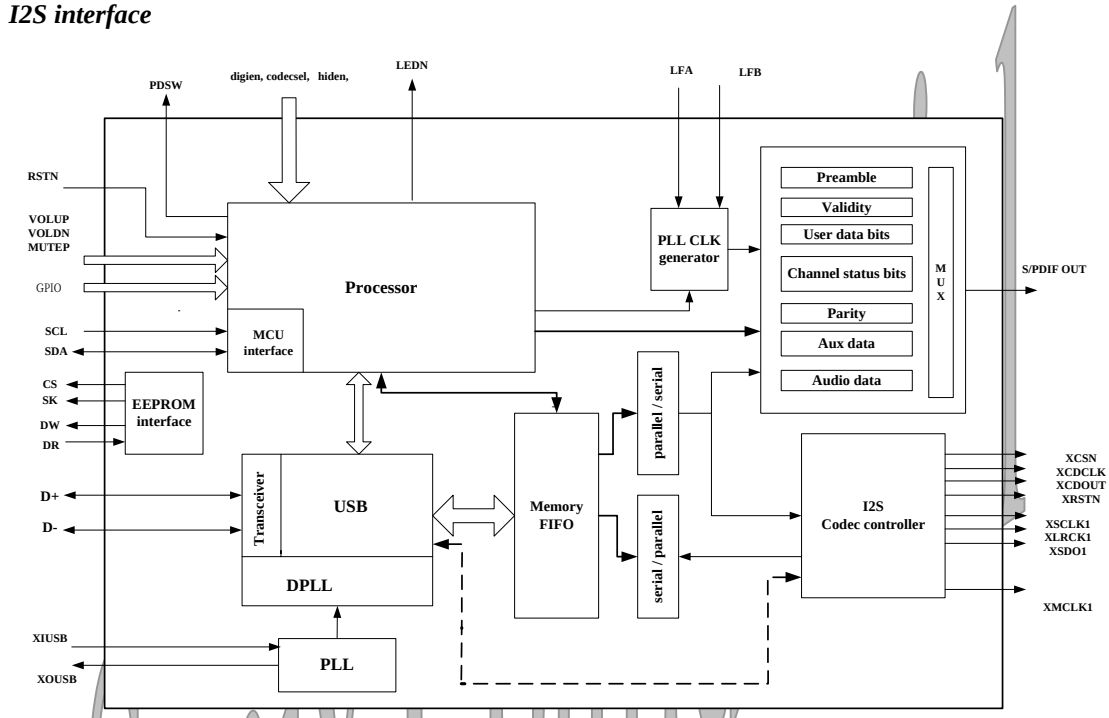
- Isochronous transfer uses adaptive, synchronous and asynchronous synchronization
- Supports AC'97 component specification v2.1 and v2.2; AC link interface for external AC97 audio Codec
- Supports 2ch Codec with I2S, Left-justified serial interface format
- Embedded Digital Volume Control of Line out for I2S interface mode
- Compliant with USB HID class specification v1.1; pin control for volume up / down, play mute
- Supports two wire series bus interface; slave only interface with transfer speed up to 400Kbps(Fast-mode)
- EEPROM interface for customized USB IDs and strings; Codec registers programming
- 3.3 V core operation and 5 V tolerant I/O
- Available in 48-pin LQFP(7x7 mm)
- System on chip solution: low cost and easy implementation without external memory
- LED indicator pins for playback and recording mute
- 4 GPIO pins controlled via USB HID
- Features programmable by jumper pins and EEPROM values

III. Ordering information

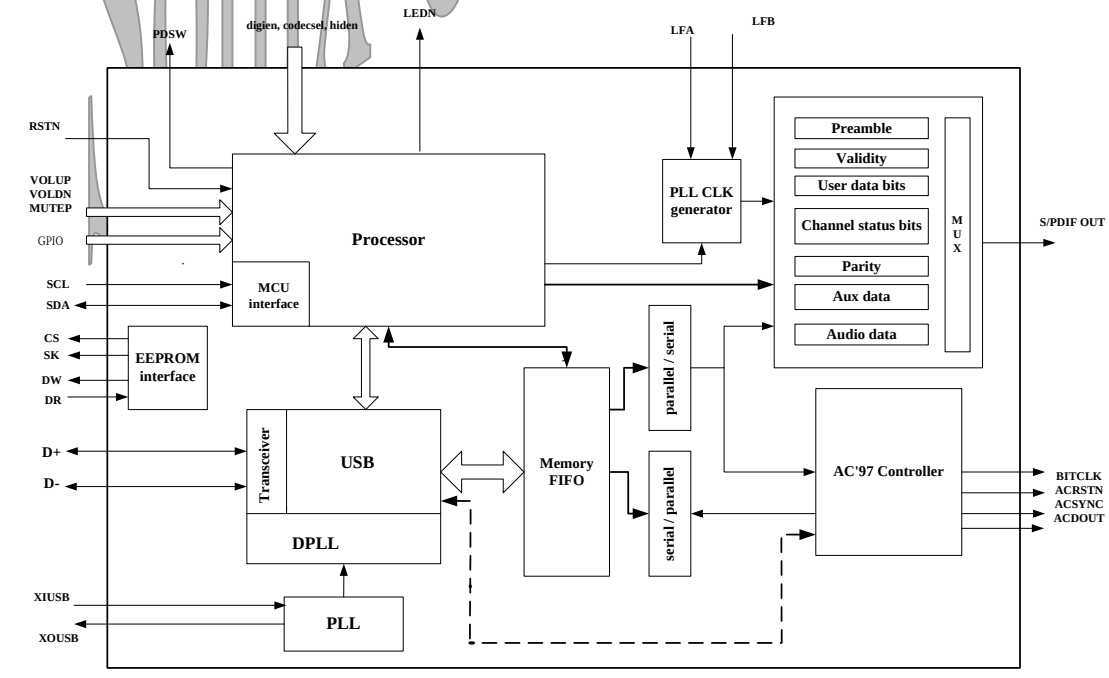
SN11121ASF : 48-pin LQFP (7x7x1.4 mm)

IV. Block diagram

I2S interface

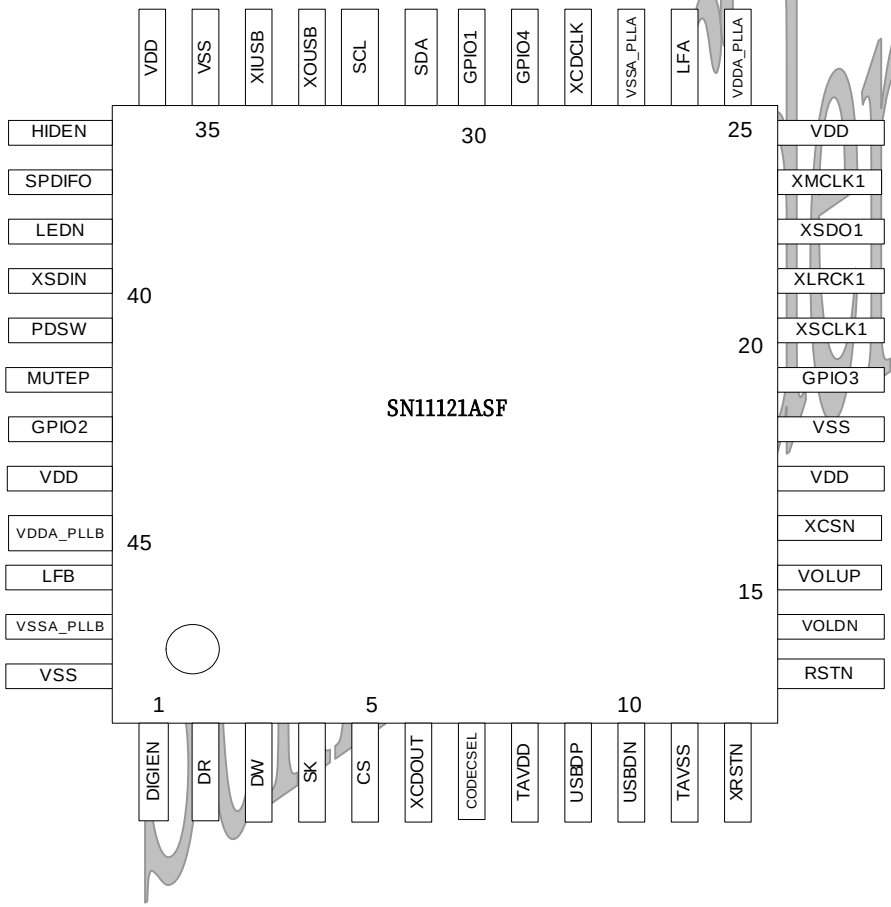


AC'97 interface



V. Pin description

5.1 SN11121ASF pin chart (48-pin LQFP)



5.2 pin assignment and description (48-pin LQFP)

Pin No.	Pad Name	Pin Type	Description
1	DIGIEN	I, ST	Enable SPDIF In/Out 1: enable ; 0: disable (analog only)
2	DR(EEPROM_ DO)	I, ST	EEPROM data input (Fixing this pin to H or L sets USB vendor ID to SONiX USB vendor ID (hex 0C45); PU or PD is used for different product ID

3	DW(EEPROM_ DI)	O, 4mA, SR	EEPROM data output
4	SK(EEPROM_ SK)	O, 4mA, SR	EEPROM clock pin
5	CS(EEPROM_ CS)	O, 4mA, SR	EEPROM chip select
6	XCDOUT(SPI_DIN)	O, 4mA, SR	SPI Codec control data
7	CODECSEL	I, ST	Codec interface selection, 0: AC-link; 1: I2S
8	TAVDD/ AVDD	P	Power pin for USB transceiver
9	USBDP	I/O	USB data plus
10	USBDN	I/O	USB data minus
11	TAVSS /AVSS	P	GND pin for USB transceiver
12	XRSTN	O, 4mA, SR	Codec reset
13	RSTN	I, ST, PU	System reset pin, pull high to reset
14	VOLDN	I, ST	Volume down control, edge trigger with 64ms de-bouncing circuit
15	VOLUP	I, ST	Volume up control, edge trigger with 64ms de-bouncing circuit
16	XCSN(SPI_CS)	O, 4mA, SR	SPI Codec chip select
17	VDD	P	3.3 V power pin
18	VSS	P	GND pin
19	GPIO3	I/O	General Purpose I/O 3
20	XSCLK1	O, 4mA, SR	I2S SCLK for play
21	XLRCK1/AC_ SYNC	O, 4mA, SR	I2S L/R frame for play / AC-link SYNC
22	XSDO1(XSD OUT/AC_DO UT)	O, 4mA, SR	I2S dout / AC-link dout
23	XMCLK1/AC _Bit_CLK	O, 8mA, SR	I2S Codec master clock for play / AC-link bit clock
24	VDD	P	3.3V power pin

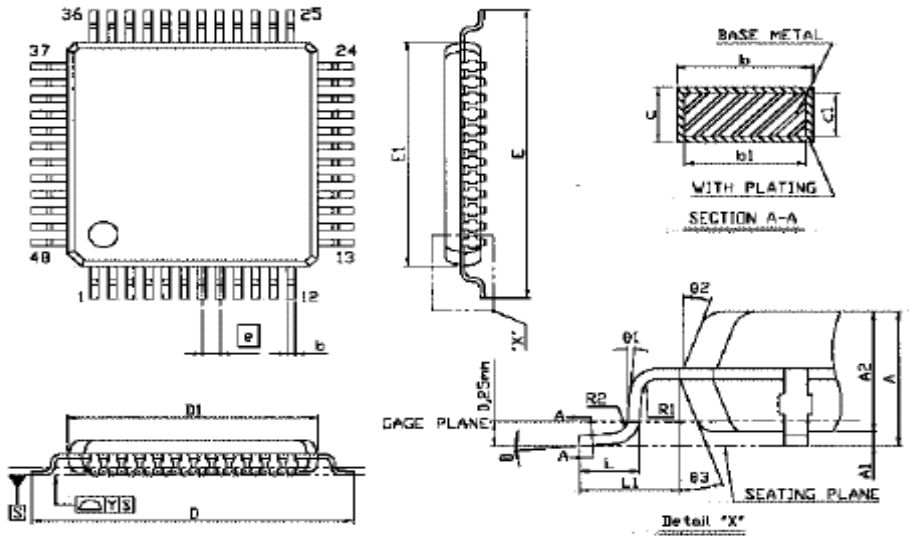
25	VDDA_PLLA	P	Power pin for internal PLL
26	LFA	I/O	Filter for internal PLL
27	VSSA_PLLA	P	GND pin for internal PLL
27	VSS	P	GND pin
28	XCDCLK(SPI_CLK)	O, 4mA, SR	SPI Codec control clock
29	GPIO4	I/O	General Purpose I/O 4
30	GPIO1	I/O	General Purpose I/O 1
31	SDA	I/O, 4mA, SR	IIC data pin
32	SCL	I, ST	IIC clock pin for external MCU control
33	XOUSB	O	6 MHz clock osc pin for USB PLL
34	XIUSB	I	6 MHz clock osc pin for USB PLL
35	VSS	P	GND pin
36	VDD	P	3.3V power pin
37	HIDEN	I, ST	USB HID enable, 1: enable, 0: disable
38	SPDIFO	O, 8mA, SR	SPDIF data output
39	LEDN	O, 8mA, SR	LED indicator pin, output low after power on reset, toggle during operation
40	XSDIN/AC_DIN	I, ST	I2D Din / AC-link Din
41	PDSW	O, 4mA, SR	Power down switch control -- 0: normal mode, 1: power down mode
42	MUTEP	I, ST	Playback mute control pin, edge trigger with 64ms de-bouncing circuit
43	GPIO2	I/O	General Purpose I/O 2
44	VDD	P	3.3V Power pin
45	VDDA_PLLB	P	Power pin for internal PLL
46	LFB	I/O	Filter for internal PLL
47	VSSA_PLLB	P	GND pin for internal PLL
48	VSS	P	GND pin

** All input pin are 5 volt tolerance, TTL level and Schmitt trigger

All output pins are slew rate control

I – input pin , O – output pin, P – power pin, ST – Schmitt trigger, SR – slew rate control, PU/PD – pull up or pull down

VI. Package dimension



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.60			63
A1	0.05		0.15	2		6
A2	1.35	1.40	1.45	53	55	57
b	0.17	0.22	0.27	7	9	11
b1	0.17	0.20	0.23	7	8	12
c	0.09		0.20	4		8
c1	0.09		0.16	4		6
D	9.00 BSC			354 BSC		
D1	7.00 BSC			276 BSC		
E	9.00 BSC			354 BSC		
E1	7.00 BSC			276 BSC		
e	0.50 BSC			20 BSC		
L	0.45	0.60	0.75	18	24	30
L1	1.00 REF			39 REF		
R1	0.08			3		
R2	0.08		0.20	3		8
Y			0.075			3
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°

NOTE:
1.REFER TO JEDEC MS-026/BBC
2.DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
ALLOWABLE PROTRUSION IS 0.25mm PER SIDE D1 AND E1 ARE
MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE
DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED
THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
4.ALL DIMENSIONS IN MILLIMETERS.

Revision History

Revision	*Revision Date*	*Description of changes*
Revision V0.2	Jan 2, 2004	Initial release.
Revision V0.3	Jan 13, 2004	Add package dimension

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