1. General Description

This OTP-Based 8-bit micro-controller uses a fully static CMOS technology process to achieve higher speed and smaller size with the low power consumption and high noise immunity. On chip memory includes 4K words of EPROM, and 192 bytes of static RAM.

2. Features

- RISC CPU
- Fully static design
- 37 single word instructions
- 4K x 14 program memory.
- 192 bytes RAM for data
- 35 bi-directional I/O
- Eight level hardware stacks
- Watchdog timer with on-chip RC oscillator.
- Interrupt capability
- Timer0 : 8-bit timer with 8-bit prescaler
- Timer1 : 8-bit timer with 8-bit compare register. This timer can be used as carrier generator.
- Sleep mode for power saving.
- PB and PD with port change wake-up interrupt.

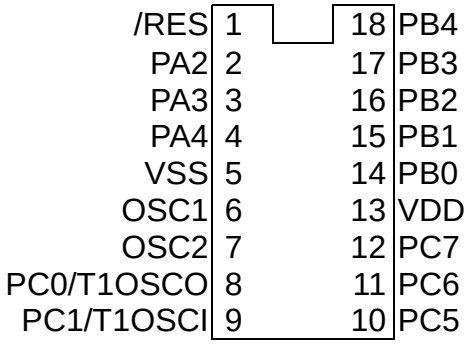
3. Applications

The application areas of this MDT10P65 range from appliance motor control and high speed automotive to low power remote transmitters/receivers and telecommunications processors, such as Remote controller, small instruments, toy, automobile and keyboard … etc.

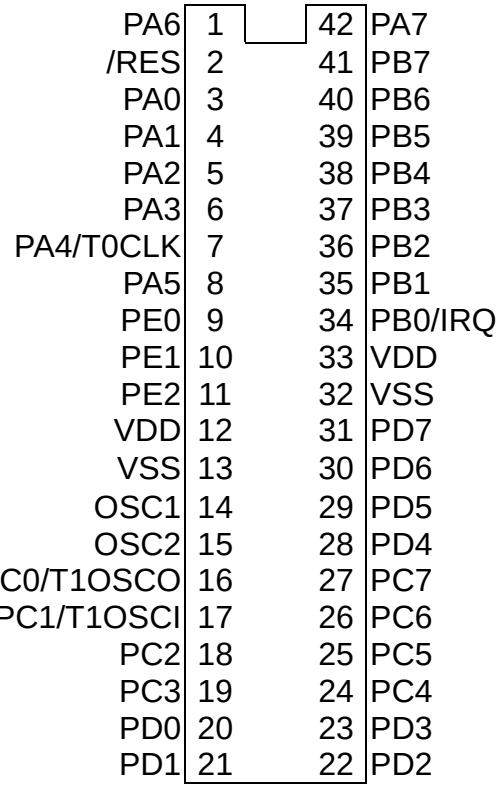
PS : timer1 counter PC0 clock in low to high the counter data increase

4. Pin Diagram

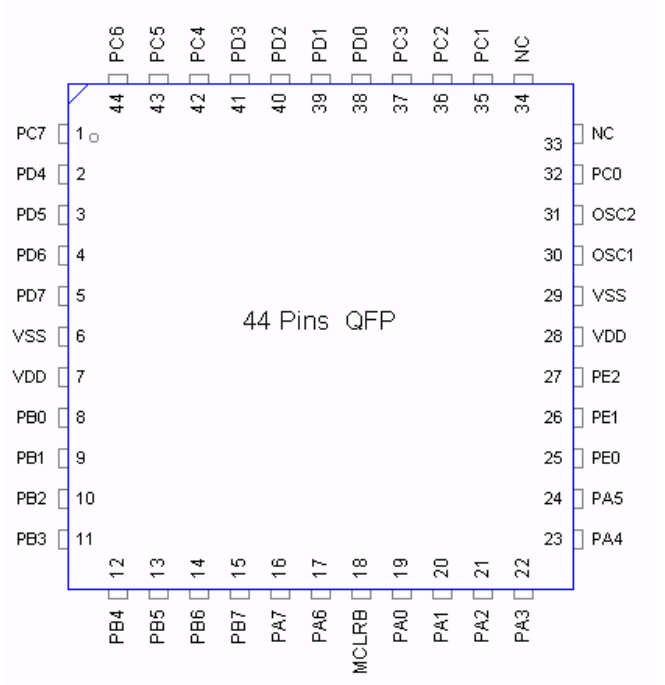
MDT10P65A3P/S 18 pin DIP/SOP



MDT10P65SD42 pin Shrink PDIP



MDT10P65A1Q



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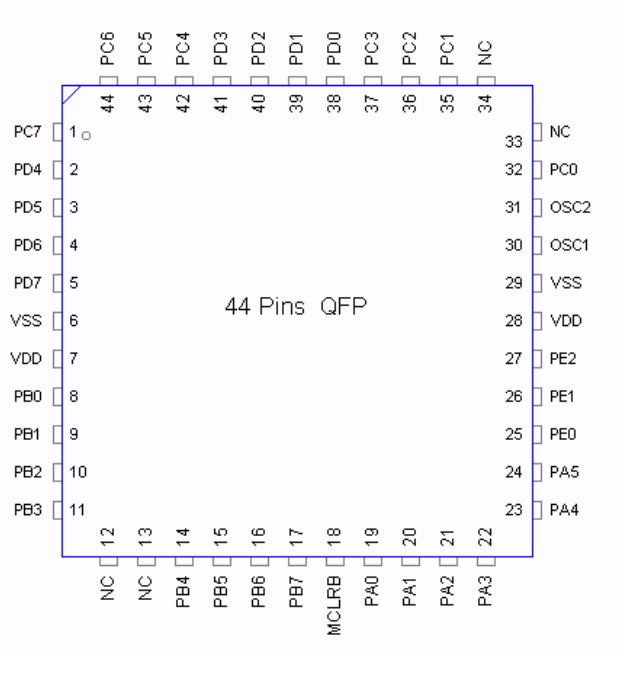
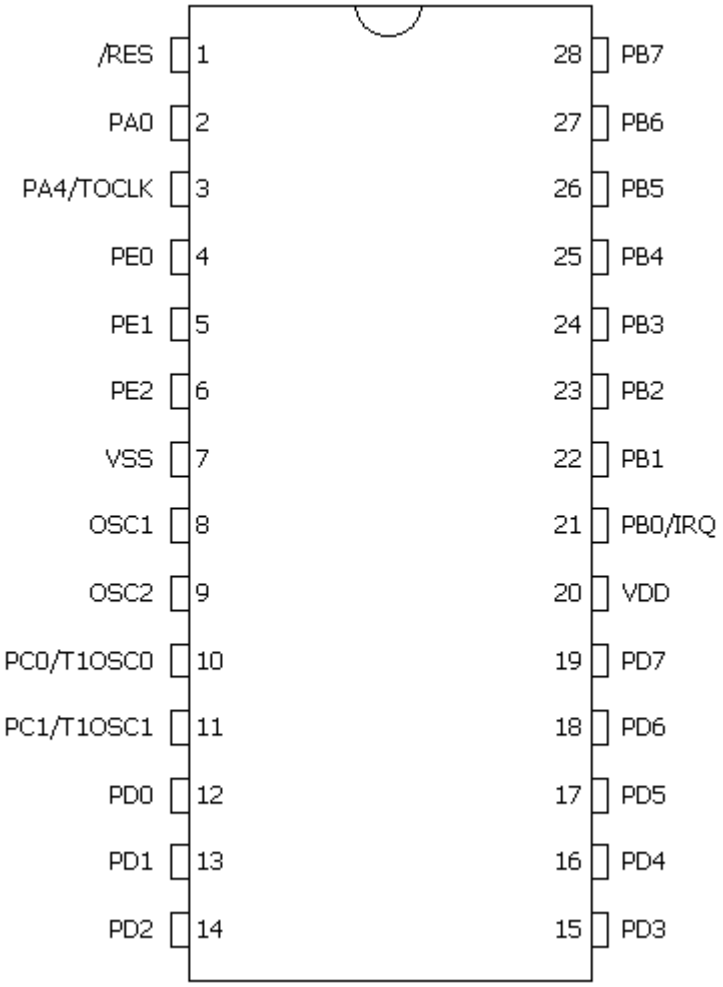


MDT10P65 pin 28 PDIP/SOP



5. Pin function description

Pin name	Type	Buffer type	Description
OSC1	I		Oscillator input
OSC2	O		Oscillator out
/RES(MCLRB)	I	ST	Reset input with 130K ohm pull-up
			Bi-directional I/O port A. Port A can be software programmed for internal 45K ohm pull-up on all pins except PA5. The pull-up resistance on PA5 is 100K ohm.
PA0	I/O	TTL	
PA1	I/O	TTL	
PA2	I/O	TTL	
PA3	I/O	TTL	
PA4	I/O	ST	Can be clock input to Timer0.
PA5	I/O	TTL	
PA6	I/O	TTL	
PA7	I/O	TTL	

Pin name	Type	Buffer type	Description
PB0/IQR PB1 PB2 PB3 PB4 PB5 PB6 PB7	I/O I/O I/O I/O I/O I/O I/O I/O	ST/TTL TTL TTL TTL TTL TTL TTL TTL	Bi-directional I/O port B. Port B can be software programmed for internal 25K ohm pull-up on all pins. PB0-PB7 can generate interrupt on pin state change. Can be the external interrupt pin.
PC0 PC1 PC2 PC3 PC4 PC5 PC6 PC7	I/O I/O I/O I/O I/O I/O I/O I/O	ST ST ST ST ST ST ST ST	Bi-directional I/O port C. Port C can be software programmed for internal 100K pull-up on all pins. Can be Timer1 oscillator output or Timer1 clock input. Can be Timer1 oscillator input.
PD0-PD7	I/O	ST	Bi-directional port. All pins can generate interrupt on pin state change. Port D can be software programmed for internal 100K pull-up on all pins.
PE0 PE1 PE2	I/O I/O I/O	ST ST ST	Bi-directional port E. Port E can be software programmed for internal 100K pull-up on all pins.
Vdd			Power input
Vss			Ground pin

6. Memory Mapping

6.1Program memory :

0000h	Reset Vector
0001h	
0002h	
0003h	
0004h	Peripheral interrupt Vector
0005h	Program memory (Page 0)
07FFh	
0800h	Program memory (Page 1)
0FFFh	

6.2Register file map :

	BANK 0	BANK 1	
00h	IAR	IAR	80h
01h	RTCC	TMR	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	MSR	MSR	84h
05h	PORT A	CPIO A	85h
06h	PORT B	CPIO B	86h
07h	PORT C	CPIO C	87h
08h	PORT D	CPIO D	88h
09h	PORT E	CPIO E	89h
0Ah	PCH	PCH	8Ah
0Bh	INTS	INTS	8Bh
0Ch	PIFB1	PIEB1	8Ch
0Dh	PIFB2	PIEB2	8Dh
0Eh	TMR1L	PSTA	8Eh
0Fh			8Fh
10h	T1STA	PPHE	90h
11h			91h
12h			92h
13h			93h
14h			94h
15h	CCP1L		95h
16h			96h
17h	CCP1CTL		97h
18h			98h
1Fh			9Fh
20h	General Purpose Register	General Purpose Register	A0h
7Fh			FFh

Unimplemented memory location.

00 Indirect addressing register
01 Timer0 register
02 Program counter low byte
03 Status register
Bit 0 : Carry
1 : Digit carry
2 : Zero flag
3 : Power-down
4 : WDT time-out
5 : Register bank select (For direct addressing)
=0 Bank 0 (00h-7Fh)
=1 Bank 1 (80h-FFh)
7-6 : Always read as zero.
04 Memory select register
05 Port A data register
06 Port B data register
07 Port C data register
08 Port D data register
09 Port E data register
Bit 2-0 – Port E data register.
7-3 – Unimplemented. Always set as 0.
0A Program memory segment register
0B Interrupt control register
Bit 0 – PB port change interrupt flag bit.
1 – PB0/IRQ external interrupt flag bit.
2 – Timer0 overflow interrupt flag bit.
3 – PB port change interrupt enable bit.
4 – PB0/IRQ external interrupt enable bit.
5 – Timer0 overflow interrupt enable bit.
6 – Peripheral interrupt enable bit.
7 – Global interrupt enable bit.
0C Peripheral interrupt flag register 1.
Bit 0 – Timer1 overflow interrupt flag bit
7-1 – Unimplemented. Always read as 0.
0D Peripheral interrupt flag register 2.
Bit 6-0 – Unimplemented. Read as zero.
7 – PD port change interrupt flag bit
0E Timer1 data register low byte.

0F Unimplemented..

10 Timer1 control register

Bit 0 – Timer1 enable bit

1 – Timer1 clock source select

2 – Timer 1 external clock synchronization control bit

3 – Timer 1 oscillator enable control bit

5-4 – Timer 1 prescaler select bits

7-6 – Unimplemented. Always read as 0.

11-14 Unimplemented.

15 Timer1 compare register

16 Unimplemented.

17 Timer1 compare control register

Bit 7-1 –Unimplemented. Always set as 0.

0 – compare enable bit

18-1F Unimplemented.

20-7F General purpose register

80 Same as register 00.

81 TMR register

Bit 2-0 – Prescaler rate select bits

3 – Prescaler assign bit

4 – Timer 0 edge select bit

5 – Timer 0 clock source select bit

6 – PB0/IRQ interrupt edge select bit

7 – Port B pull-up enable bit.

82-84 Same as 02H-04H.

85 Port A data direction register.

86 Port B data direction register.

87 Port C data direction register.

88 Port D data direction register.

89 Port E data direction register.

Bit 2-0 – Port E data direction register.

7-3 – Unimplemented. Always set as 0.

8A -8B Same as 0AH-0BH.

8C Peripheral interrupt control register 1.

Bit 0 – Timer1 overflow interrupt enable bit.

7-1 – Unimplemented. Always set these bits to 0.

8D Peripheral interrupt control register 2

Bit 6-0 – Unimplemented.

7 – PD port change interrupt enable bit.

8E Power control register.

Bit 0 –Unimplemented. Always read as 0.

1 – Power-on reset status bit.

7-2 – Unimplemented. Always read as 0.

8F Unimplemented.

90 PPHE register . (“ 0 ” Enable ; “ 1 ” Disable)

Bit 0-3 – Unimplemented.

4 – PA port pull-up enable bit.

5 – PC port pull-up enable bit.

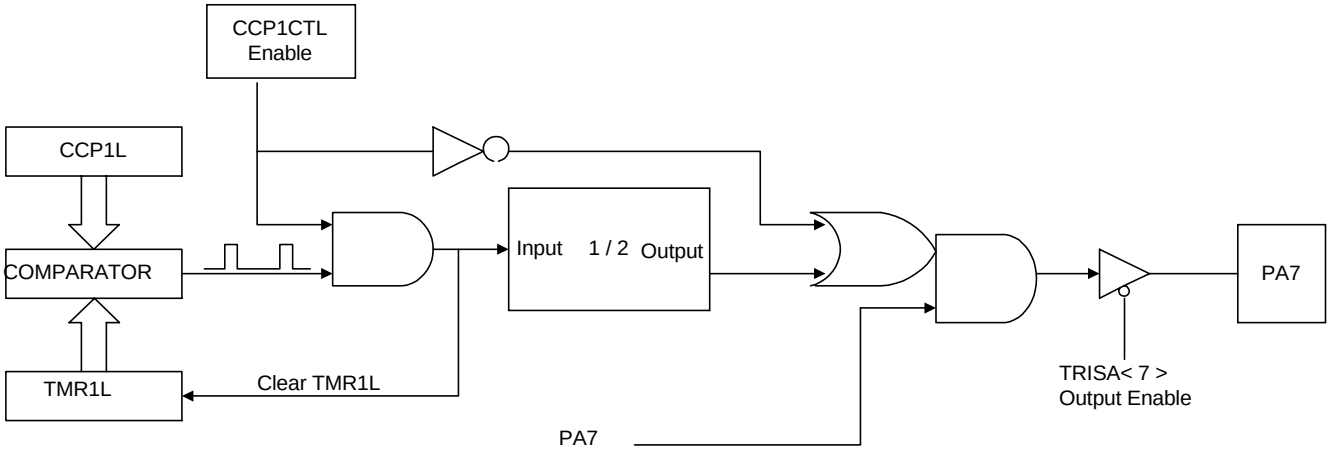
6 – PD port pull-up enable bit.

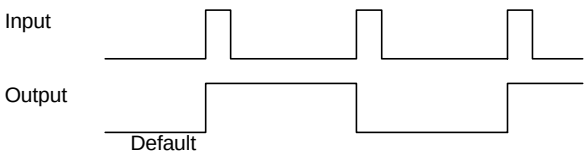
7 – PE port pull-up enable bit.

91-9F Unimplemented.

A0-FF General purpose register.

7. Timer1 CCP Mode





8. Reset Condition for all Registers

Register	Address	Power-On Reset, Power range detector Reset	/MCLR or WDT Reset	Wake-up from SLEEP
IAR	00h(80h)	0000 0000	0000 0000	uuuu uuuu
RTCC	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h(82h)	0000 0000	0000 0000	0000 0100
STATUS	03h(83h)	0001 1xxx	000# #uuu	000# #uuu
MSR	04h(84h)	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORT A	05h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORT B	06h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORT C	07h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORT D	08h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORT E	09h	---- -xxx	---- -uuu	---- -uuu
PCH	0Ah(8Ah)	---- 0000	---- 0000	---- uuuu
INTS	0Bh(8Bh)	0000 0001	0000 0001	uuuu uuuu
PIFB1	0Ch	---- ---x	---- ---u	---- ---u
PIFB2	0Dh	1--- ----	1--- ----	u--- ----
TMR1L	0Eh	xxxx xxxx	Uuuu uuuu	Uuuu uuuu
T1STA	10h	--00 0000	--00 0000	--uu uuuu
CCP1L	15h	Xxxx xxxx	uuuu uuuu	--uu uuuu
CCP1CTL	17h	---- ---0	---- ---0	---- ---u
TMR	81h	1111 1111	1111 1111	uuuu uuuu
CPIO A	85h	1111 1111	1111 1111	uuuu uuuu
CPIO B	86h	1111 1111	1111 1111	uuuu uuuu
CPIO C	87h	1111 1111	1111 1111	uuuu uuuu
CPIO D	88h	1111 1111	1111 1111	uuuu uuuu
CPIO E	89h	---- -111	---- -111	---- -uuu
PIEB1	8Ch	---- ---0	---- ---0	---- ---u
PIEB2	8Dh	0--- ----	0--- ----	u--- ----
PSTA	8Eh	---- --#-	---- --u-	---- --u-
PPHE	90h	1111 ----	1111 ----	uuuu ----

Note ： u = unchanged, x = unknown, - = unimplemented, read as “0”

= value depends on the condition of the following table

Condition	Status bit 4	Status bit 3	PSTA bit 1
POWR ON RESET	1	1	0
/MCLR reset (not during SLEEP)	u	u	u
/MCLR reset during SLEEP	1	0	u
WDT reset (not during SLEEP)	0	1	u
WDT reset during SLEEP	0	0	u
Interrupt Wake-up during SLEEP	1	0	u

9. Electrical Characteristics

(Operating temperature at 25℃).

Sym	Description	Condition	Min	Typ	Max	Unit
Vdd	Operating voltage		2.3		5.5	V
V_{IL}	Input Low Voltage					
	PA, PB, PC, PD, PE	Vdd=5V	-0.6		1.0	V
	/RES	Vdd=5V	-0.6		1.0	V
V_{IH}	Input high Voltage					
	PA, PB, PC, PD, PE	Vdd=5V	2.0		Vdd+0.6	V
	/RES	Vdd=5V	3.0		Vdd+0.6	V
I_{IL}	Input leakage current	Vdd=5V			+/-1	μA
V_{OL}	Output Low Voltage					
	PA0-PA3	Vdd=5V, I_{OL}=16mA		4		V
	PA4-PA7, PB, PC, PD, PE	Vdd=5V, I_{OL}=20mA		0.5		V
		Vdd=5V, I_{OL}=5mA		0.2		V
V_{OH}	Output High Voltage					
	PA, PB, PC, PD, PE	Vdd=5V, I_{OH}= -20mA		3.5		V
		Vdd=5V, I_{OH}= -5mA		4.5		V
R_{Hi}	Pull-up resistance					
	PA0-PA4, PA6-PA7	Vdd=5V		45K		Ohm
	PB	Vdd=5V		25K		Ohm
	PA5, PC, PD, PE	Vdd=5V		100K		Ohm

10. Instruction Set

Instruction Code	Mnemonic Operands	Function	Operation	Status
010000 00000000	NOP	No operation	None	
010000 00000001	CLRWT	Clear Watchdog timer	0→WT	TF, PF
010000 00000010	SLEEP	Sleep mode	0→WT, stop OSC	TF, PF
010000 00000011	TMODE	Load W to TMODE register	W→TMODE	None
010000 00000rrr	CPIO R	Control I/O port register	W→CPIO r	None
010001 1rrrrrrr	STWR R	Store W to register	W→R	None
011000 trrrrrrr	LDR R, t	Load register	R→t	Z
111010 iiiiiiii	LDWI I	Load immediate to W	I→W	None
010111 trrrrrrr	SWAPR R, t	Swap halves register	[R(0~3) ↔ R(4~7)]→t	None
011001 trrrrrrr	INCR R, t	Increment register	R + 1→t	Z
011010 trrrrrrr	INCRSZ R, t	Increment register, skip if zero	R + 1→t	None
011011 trrrrrrr	ADDWR R, t	Add W and register	W + R→t	C, HC, Z
011100 trrrrrrr	SUBWR R, t	Subtract W from register	R – W→t (R+/W+1→t)	C, HC, Z
011101 trrrrrrr	DECR R, t	Decrement register	R – 1→t	Z
011110 trrrrrrr	DECRSZ R, t	Decrement register, skip if zero	R – 1→t	None
010010 trrrrrrr	ANDWR R, t	AND W and register	R ∩ W→t	Z
110100 iiiiiiii	ANDWI i	AND W and immediate	i ∩ W→W	Z
010011 trrrrrrr	IORWR R, t	Inclu. OR W and register	R ∪ W→t	Z
110101 iiiiiiii	IORWI i	Inclu. OR W and immediate	i ∪ W→W	Z
010100 trrrrrrr	XORWR R, t	Exclu. OR W and register	R ⊕ W→t	Z
110110 iiiiiiii	XORWI i	Exclu. OR W and immediate	i ⊕ W→W	Z
011111 trrrrrrr	COMR R, t	Complement register	/R→t	Z
010110 trrrrrrr	RRR R, t	Rotate right register	R(n) → R(n-1), C→ R(7), R(0)→C	C
010101 trrrrrrr	RLR R, t	Rotate left register	R(n)→r(n+1), C→R(0), R(7)→C	C
010000 1xxxxxxx	CLRW	Clear working register	0→W	Z

Instruction Code	Mnemonic Operands	Function	Operation	Status
010001 0rrrrrrr	CLRR R	Clear register	0→R	Z
0000bb brrrrrrr	BCR R, b	Bit clear	0→R(b)	None
0010bb brrrrrrr	BSR R, b	Bit set	1→R(b)	None
0001bb brrrrrrr	BTSC R, b	Bit Test, skip if clear	Skip if R(b)=0	None
0011bb brrrrrrr	BTSS R, b	Bit Test, skip if set	Skip if R(b)=1	None
100nnn nnnnnnnn	LCALL n	Long CALL subroutine	n→PC, PC+1→Stack	None
101nnn nnnnnnnn	LJUMP n	Long JUMP to address	n→PC	None
110001 iiiiiiii	RTWI i	Return, place immediate to W	Stack→PC, i→W	None
110111 iiiiiiii	ADDWI	Add immediate to W	PC+1→PC, W+i→W	C,HC,Z
111000 iiiiiiii	SUBWI	Subtract W from immediate	i-W→W	C,HC,Z
010000 00001001	RTFI	Return from interrupt	Stack→PC, 1→GIS	None
010000 00000100	RET	Return from subroutine	Stack→PC	None

Note :

W	:	Working register	b	:	Bit position
WT	:	Watchdog timer	t	:	Target
TMODE	:	TMODE mode register	0	:	Working register
CPIO	:	Control I/O port register	1	:	General register
TF	:	Timer overflow flag	R	:	General register address
PF	:	Power loss flag	C	:	Carry flag
PC	:	Program Counter	HC	:	Half carry
OSC	:	Oscillator	Z	:	Zero flag
Inclu.	:	Inclusive ‘∪’	/	:	Complement
Exclu.	:	Exclusive ‘⊕’	x	:	Don’t care
AND	:	Logic AND ‘∩’	i	:	Immediate data (8 bits)
			n	:	Immediate address