OVERVIEW

The SM6155P/S is a successive-approximation 8-bit A/D converter, fabricated using the Molybdenum-gate CMOS process. It's low-voltage operation makes it ideal for battery-powered portable equipment.

The output comprises 8-bit 3-state output pins for easy interface with a microprocessor. The 8-bit converted data can be output in either MSB first or LSB first order. Also, it features an 8-channel analog multiplexer built-in.

FEATURES

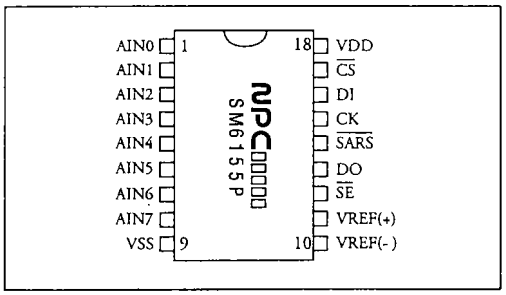
- Charge-redistribution method, successive-approximation A/D converter
- 8-bit resolution
- 18 µs conversion time (f_{CK} = 1 MHz)
- 4.5 to 5.5 V operating supply voltage range
- Low current consumption
  - ≤ 2 mA during conversion
  - Standby current
    - ≤ 100 µA (f_{CK} = 1 MHz)
    - ≤ 1 µA (with no input clock)
- High precision
  - ≤ ±0.75 LSB non-linearity error
- Serial input/output type
- 8-channel analog multiplexer built-in
- Molybdenum-gate CMOS process
- 18-pin plastic SOP and DIP

APPLICATIONS

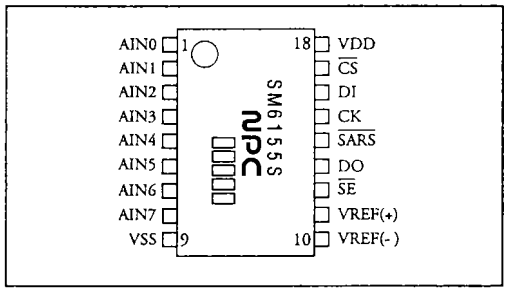
- Data acquisition systems
- Measurement equipment

PINOUTS

18-pin DIP



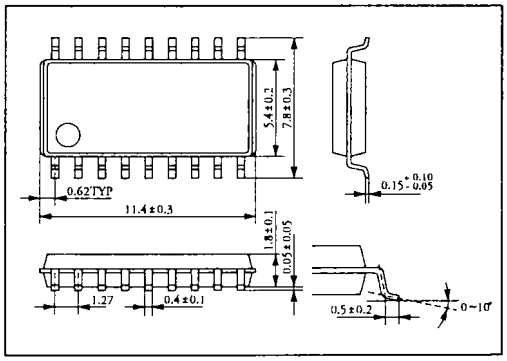
18-pin SOP



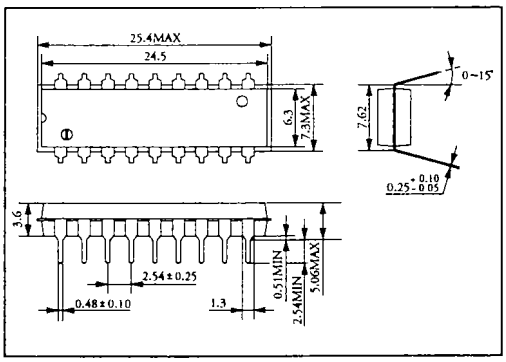
PACKAGE DIMENSIONS

Unit: mm

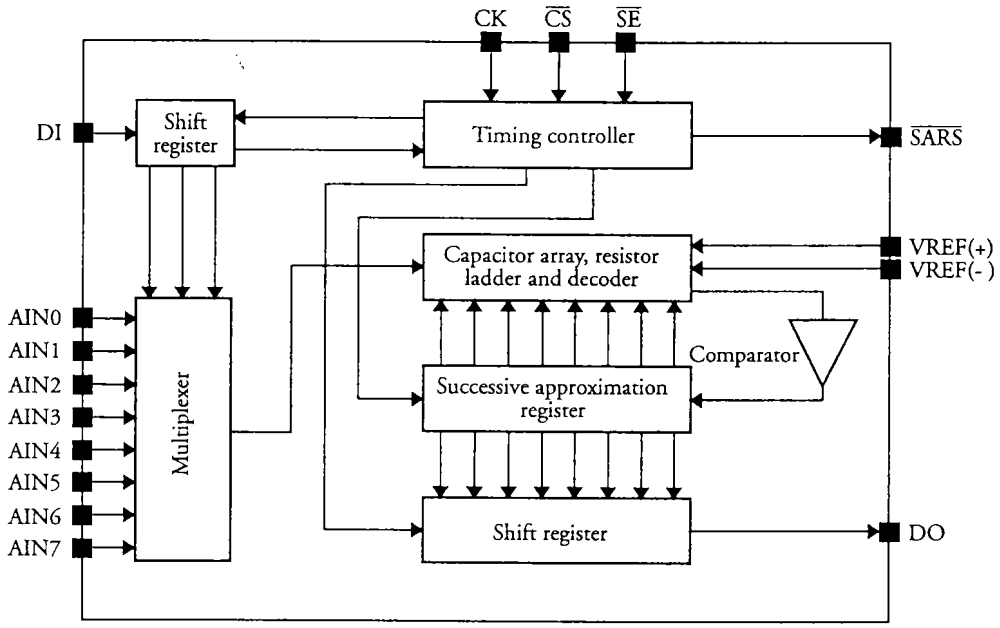
18-pin SOP



18-pin DIP



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	Description
1	AIN0	Analog input channel 0
2	AIN1	Analog input channel 1
3	AIN2	Analog input channel 2
4	AIN3	Analog input channel 3
5	AIN4	Analog input channel 4
6	AIN5	Analog input channel 5
7	AIN6	Analog input channel 6
8	AIN7	Analog input channel 7
9	VSS	Ground
10	VREF(–)	Reference voltage input pin (low end)
11	VREF(+)	Reference voltage input pin (high end)
12	$\overline{SE}$	Converted data output direction select pin. MSB first when HIGH, and LSB first when LOW.
13	DO	Converted data serial output pin
14	$\overline{SARS}$	LOW during conversion. Goes HIGH after conversion ends.
15	CK	Clock input
16	DI	Analog multiplexer select serial input
17	$\overline{CS}$	Chip select pin. Normal operation when LOW. Goes HIGH in standby mode. In standby mode, DI and $\overline{SARS}$ outputs go high impedance, and current consumption is reduced.
18	VDD	Supply voltage

SPECIFICATIONS

Absolute Maximum Ratings

$V_{SS} = 0$ V

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	−0.3 to 7.0	V
Input voltage range	V_{IN}	− 0.3 to V_{DD} + 0.3	V
Output voltage range	V_{OUT}	− 0.3 to V_{DD} + 0.3	V
Storage temperature range	T_{stg}	−40 to 125	°C
Power dissipation	P_D	250	mW
Soldering temperature	T_{sld}	255	°C
Soldering time	t_{sld}	10	s

Recommended Operating Conditions

$V_{SS} = 0$ V

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply voltage	V_{DD}		4.5	–	5.5	V
VREF(+)-to-VREF(−) voltage	V_{REF}		2.0	–	V_{DD}	V
Clock frequency	f_{CK}		0.01	–	1.0	MHz
Operating temperature	T_{opr}		−20	–	70	V

DC Electrical Characteristics

V_{DD} = 4.5 to 5.5 V, T_a = −20 to 70 °C unless otherwise noted

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
CK, $\overline{CS}$, $\overline{SE}$ and DI HIGH-level input voltage	V_{IH}			0.7V_{DD}	–	–	V
CK, $\overline{CS}$, $\overline{SE}$ and DI LOW-level input voltage	V_{IL}			–	–	0.3V_{DD}	V
CK, $\overline{CS}$, $\overline{SE}$ and DI HIGH-level input current	I_{IH}	$V_{IH} = V_{DD}$		–	–	1	µA
CK, $\overline{CS}$, $\overline{SE}$ and DI LOW-level input current	I_{IL}	$V_{IL} = V_{SS}$		−1	–	–	µA
$\overline{SARS}$ and DO HIGH-level output voltage	V_{OH}	I_{source} = 0.8 mA		V_{DD} − 0.4	–	–	V
$\overline{SARS}$ and DO LOW-level output voltage	V_{OL}	I_{sink} = 0.8 mA		–	–	0.4	V
$\overline{SARS}$ and DO high-impedance leakage current	I_{leak}	$V_{OUT} = V_{DD}$		–	–	3	µA
		$V_{OUT} = V_{SS}$		−3	–	–	µA
AIN0 to AIN7 analog input current	I_{AIN}	$V_{AIN} = V_{DD}$		–	–	3	µA
		$V_{AIN} = V_{SS}$		−3	–	–	µA
Operating current consumption	I_{DD}	f_{CK} = 1 MHz	V_{DD} = 5.5 V	–	0.5	2.0	mA
			V_{DD} = 4.5 V	–	0.1	–	mA

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Standby current	I_{DS1}	f_{CK} = 1 MHz	–	10	100	µA
	I_{DS2}	$V_{CK} = V_{SS}$ or V_{DD}	–	0.1	1	µA
VREF(+)-to-VREF(–) reference resistance	R_{REF}	Conversion operation	–	16	–	kΩ
		In standby mode	10	–	–	MΩ

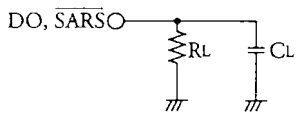
AC Electrical Characteristics

V_{DD} = 4.5 to 5.5 V, T_a = –20 to 70 °C unless otherwise noted

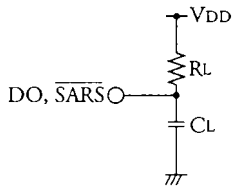
Parameter[1]	Symbol	Condition	Rating			Unit
			min	typ	max	
Output rise time[2]	t_{TLH}	C_L = 20 pF	–	–	100	ns
Output fall time[2]	t_{THL}	C_L = 20 pF	–	–	100	ns
3-state output enable time[3]	t_{PZH}, t_{PZL}	C_L = 20 pF, R_L = 1 kΩ	–	–	200	ns
3-state output disable time[4]	t_{PHZ}, t_{PLZ}	C_L = 20 pF, R_L = 1 kΩ	–	–	200	ns
CK data propagation delay	t_{PLH}, t_{PHL}	C_L = 20 pF	–	–	150	ns
CK to $\overline{SARS}$ propagation delay	t_{PLH}, t_{PHL}	C_L = 20 pF	–	–	150	ns
Data setup time	t_S		100	–	–	ns
Data hold time	t_H		100	–	–	ns
$\overline{CS}$ setup time[5]	t_{SCS}		100	–	–	ns

1. All times are measured from when the input control signal output level reaches the 50% point.
2. Rise and fall times are measured between the output level 10% and 90% points.
3. Measured with the following load circuit, when the data output has been 50% converted.
4. Measured with the following load circuit, when the data output has been 10% converted.
5. The setup time is measured from when $\overline{CS}$ goes LOW until the first rising edge of CK for which DI is LOW.

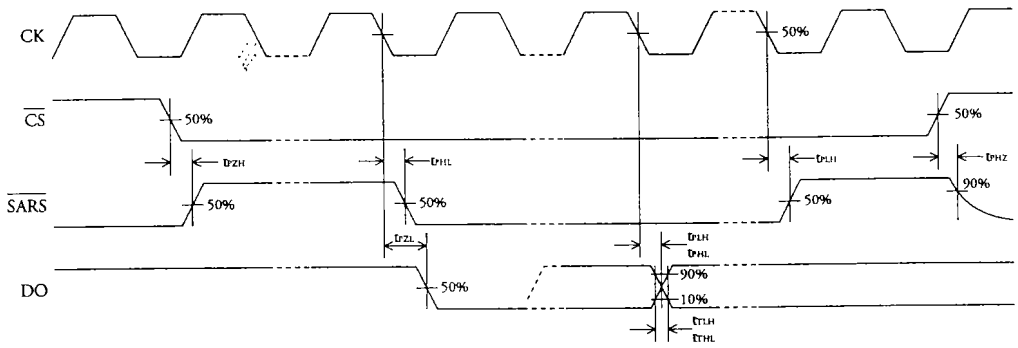
t_{PHZ}, t_{PZH} load circuit

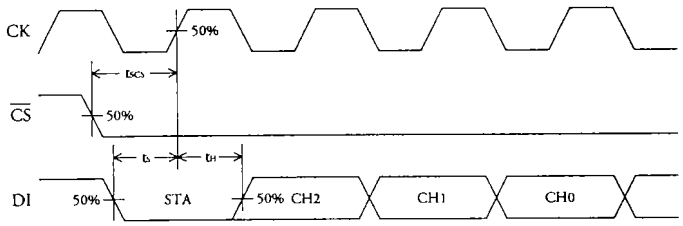


t_{PLZ}, t_{PZL} load circuit



AC Timing





Conversion Characteristics

V_{DD} = 2.8 to 5.5 V, VREF(+) = V_{DD}, VREF(−) = V_{SS}, T_a = −20 to 70 °C unless otherwise noted

Parameter	Condition	Rating			Unit
		min	typ	max	
Resolution		–	–	8	bits
Non-linearity error		–	–	±0.75	LSB
Differential non-linearity error		–	–	±0.75	LSB
Offset error[1]		–	–	±0.75	LSB
Full-scale error[1]		–	–	±0.75	LSB
Conversion time	f_{CK} = 1 MHz, $\overline{SE}$ = HIGH, MSB first output order	–	18	–	µs
		–	18	–	clock cycles

1. The offset error and full-scale error represent the error from the ideal transition points of 0.5 LSB and 254.5 LSB, respectively.

FUNCTIONAL DESCRIPTION

When $\overline{CS}$ is HIGH, outputs DO and $\overline{SARS}$ are high impedance. This effectively puts the device into power-save state with reduced current consumption.

When $\overline{CS}$ is LOW, conversion is enabled. $\overline{SARS}$ goes HIGH and the device waits for the channel select signal on input DI. The channel select serial data signal comprises a LOW-level start bit followed by channel select bits CH2, CH1 and CH0, in that

When $\overline{SE}$ is LOW, output DO is held high impedance while $\overline{SARS}$ is LOW. When $\overline{SARS}$ goes HIGH, the serial data output on DO comprises a LOW-level start bit followed by the 8-bit converted data (LSB first) followed by a HIGH-level stop bit.

The conversion time requires 18 clock cycles from when input DI goes LOW. The conversion cycle, therefore, requires a minimum of 18 cycles when $\overline{SE}$ is HIGH (MSB first) or 28 cycles when $\overline{SE}$ is LOW

8-channel Analog Multiplexer Switching

The input channel is selected according to serial data input on DI. When $\overline{CS}$ is LOW, the data signal comprises a LOW-level start bit followed by bits CH2, CH1 and CH0, in that order, synchronized to the CK signal. These bits select analog input signal channel as shown in the following table.

Input channel select truth table

Serial input data			Channel
CH2	CH1	CH0	
0	0	0	AIN0
0	0	1	AIN1
0	1	0	AIN2
0	1	1	AIN3
1	0	0	AIN4
1	0	1	AIN5
1	1	0	AIN6
1	1	1	AIN7