19-0317; Rev 1; 3/95

MAXIM

# MAX2101 Evaluation Kit

Evaluates: MAX2101

## General Description

The MAX2101 evaluation kit (EV kit) simplifies the evaluation of the MAX2101 quadrature digitizer. The board is assembled with a MAX2101, supporting circuitry such as a complete phase-locked loop, filter tuning circuitry, signal and data buffering, and supply conditioning for ease of characterization.

This manual provides complete instructions for using the EV kit. Separate sections discuss board interfacing, recommended test equipment, and measurement techniques.

## Ordering Information

| PART | TEMP. RANGE | BOARD TYPE |
|---|---|---|
| MAX2101EVKIT-SO | 0°C to +70°C | Surface Mount |

## Features

- **ADCs Provide Greater than 5.3 Effective Bits and $f_S$ = 60Msps Data Rate, $f_{IN}$ = 15MHz**
- **Integrated Lowpass Filters with Variable Bandwidth (10MHz to 30MHz)**
- **On-Board Phase-Locked Loop for Generation of Quadrature Detection Local Oscillator (450MHz to 650MHz)**
- **Buffered Baseband Signals (both I and Q) for Ease of Demodulator Characterization**
- **Buffered Baseband Data for Ease of ADC Characterization**
- **User Selectable Output Data Format (twos complement or offset binary)**
- **Programmable Counter for Variable Sample Rates**

## Component List

| DESIGNATION | QTY | DESCRIPTION |
|---|---|---|
| AR3 | 1 | Dual single-supply op amp (SO-8). Maxim MAX407CSA. |
| U21, U22 | 2 | Wideband transconductance amplifiers. Maxim MAX436CSD. |
| AR6 | 1 | OP27, low-noise op amp (SO-8). Maxim OP27GS. |
| U1, U2 | 2 | Octal 3-state buffers 74ABT541 (SO-20). Texas Instruments 74ABT541DW. |
| U3 | 1 | Voltage regulator LM337 (TO-220). National Semiconductor LM337T. |
| U4 | 1 | ECL phase frequency detector MC12040 (PLCC-20). Motorola MC12040FN. |
| U5 | 1 | ECL triple-line receiver MC10116 (PLCC-20). Motorola MC10116FN. |
| U6 | 1 | 6-bit quadrature digitizer MAX2101 (MQFP-100). Maxim MAX2101. |
| C1, C3–C6, C9, C10, C13–C16, C20, C33, C35, C39, C67–C73, C88, C89, C94, C95, C96, C101, C102, C103, C200, C300, C301 | 33 | 0.01µF, 20%, 50V ceramic capacitors |
| C7, C8 | 2 | 180pF, 5%, 50V ceramic capacitors |
| C11, C12 | 2 | 470pF, 5%, 100V ceramic capacitors |
| C18, C22, C302 | 3 | 100pF, 10%, 50V ceramic capacitors |
| C21, C25, C26, C29, C31, C32, C41, C42, C44, C46, C48, C50, C52, C58, C65, C74, C76, C90 | 18 | 0.1µF, 10%, 50V ceramic capacitors |
| C27, C36, C43, C45, C47, C49, C51, C53, C59, C60, C66, C75, C77, C91 | 14 | 1000pF, 10%, 50V ceramic capacitors |
| C78, C81 | 2 | 33µF, 20%, 20V tantalum capacitors. AVX TPSD336M020R0200. |
| C79, C80, C83, C104, C105 | 5 | 100µF, 20%, 10V tantalum capacitors. AVX TPSD107M010R0100. |
| C82 | 1 | 10µF, 20%, 25V aluminum capacitor. Nichicon UWX1E100M. |
| C54, C56, C61–C64, C84–C87, C97–C100 | 14 | 0.22µF, 10%, 25V ceramic capacitors |

## Component List (continued)

| DESIGNATION | QTY | DESCRIPTION |
|---|---|---|
| C92 | 1 | 2.0pF to 10pF, 100V ceramic variable capacitor. Tusonix 513016 A 2.0-10. |
| C2, C93 | 2 | 1pF, 10%, 25V ceramic capacitors |
| D_VARI | 1 | 2.0pF to 10pF, hyper-abrupt varactor diode (SOT-23). Alpha Industries 1204199 dual or M/A-COM MA45436. |
| VR100 | 1 | 12V zener diode (RV021C through-hole). Motorola 1N4742A. |
| L1, L2 | 2 | 8nH air-core inductors. CoilCraft A03T. |
| L3, L4, L6, L8 | 4 | 68nH, 10%, Q = 50 ceramic core inductors. CoilCraft 1206CS-680XKBC. |
| R12, R13, R16–R23, R60, R69–R85 | 28 | 51Ω, 5%, 0.125W resistors |
| R1, R3 | 2 | 100Ω, 5%, 0.125W resistors |
| R4, R5, R6, R36, R58, R59 | 6 | 20kΩ, 1%, 0.125W resistors |
| R7 | 1 | 5.6kΩ, 1%, 0.125W resistor |
| R8 | 1 | 2.21kΩ, 1%, 0.125W resistor |
| R25, R27, R37, R47 | 4 | 4.75kΩ, 1%, 0.125W resistors |
| R11 | 1 | 24.9Ω, 5%, 0.125W resistor |
| R14, R15, R24, R26, R33, R34 | 6 | 10kΩ, 5%, 0.125W resistors |
| R28–R31 | 4 | 47.5kΩ, 1%, 0.125W resistors |
| R32, R65 | 2 | 2.32kΩ, 1%, 0.125W resistors |
| R35, R61–R64, R66, R67 | 7 | 1kΩ, 5%, 0.125W resistors |
| R48 | 1 | 10kΩ, 25%, 0.25W variable resistor (single-turn) |
| R49, R50 | 2 | 2kΩ, 25%, 0.25W variable resistors (multi-turn through-hole) |
| R53, R54, R68 | 3 | 200Ω, 1%, 0.125W resistors |
| R55 | 1 | 121Ω, 1%, 0.125W resistor |
| R200, R201 | 2 | 221Ω, 5%, 0.125W resistors |
| R56 | 1 | 75Ω, 1%, 0.125W resistor |
| R301, R302 | 2 | 500Ω, 5%, 0.125W resistors |
| R38, R39, R41, R42 | 4 | 51.1kΩ, 1%, 0.125W resistors |
| R40, R43 | 2 | 576Ω, 1%, 0.125W resistors |
| R44, R51 | 2 | 5.9kΩ, 1%, 0.125W resistors |
| R45, R46 | 2 | 150Ω, 1%, 0.125W resistors |
| SW1 | 1 | Dip 6 SPST rocker switch |
| P1–P10 | 10 | SMA RF connectors, 50Ω, female |
| J1, J4, J7, J8 | 4 | 0.100"/center 1x2 male square pins |
| J2, J3, J5, J6 | 4 | 0.100"/center 1x6 male square pins |
| None | 1 | MAX2101 PC board. Maxim. |
| None | 1 | MAX2101 data sheet. Maxim. |
| SH1* | 1 | 0.5" x 1.0" x 0.5" brass RF shield (not mounted). Fotofabrication. |

** Optional for shielding the LO resonant tank circuit.*

## Component Suppliers

| SUPPLIER | PHONE | FAX |
|---|---|---|
| Alpha Industries | (617) 935-5150 | (617) 935-2359 |
| AVX | (207) 282-5111<br>(800) 282-4975 | (207) 283-1941 |
| CoilCraft | (708) 639-6400 | (708) 639-1469 |
| M/A-COM | (617) 564-3100 | (617) 564-3050 |
| Motorola | (602) 655-5058 | (602) 655-5020 |
| Nichicon | (708) 843-7500 | (708) 843-2798 |
| Fotofabrication | (312) 463-6211 | (312) 463-3387 |
| Tusonix | (602) 744-0400 | (602) 744-6155 |

## Test Equipment Required

### Signal Generators

Input (IFIN):
400MHz to 700MHz frequency range
(two sources necessary for intermodulation measurements)

LO Reference Oscillator:
20MHz to 50MHz frequency range

Master Sample Clock:
Under 1MHz to over 60MHz frequency range

### Measurement Equipment

Oscilloscope:
Over 200MHz bandwidth, Tektronix TDS 460

Logic Analyzer:
Over 100MHz data rate, Tektronix 3001HSM
(200 channels @ 200MHz)

## Getting Started

The MAX2101 EV kit is fully assembled and tested. To verify board functionality and proceed with evaluation, follow these start-up instructions. **Do not turn on the power supply until all connections are completed.**

### Power-Supply Connections

1) Connect a +15V supply to the pad marked +15V.
2) Connect a -15V supply to the pad marked -15V.
3) Connect a +5V supply to the pad marked +5V. Verify the supply is capable of sourcing 500mA of current, as noted on the board.
4) Connect a -5.2V supply to the pad marked -5.2V.
5) Connect power-supply ground to the pad marked GROUND.

### Signal Connections

1) Connect the input labeled IFIN to a signal generator through a 50Ω cable.
2) Connect the input labeled EXT'L OSC IN to a signal generator through a 50Ω cable.
3) Connect the input labeled MASTER CLK IN to a signal generator through a 50Ω cable.
4) To use external baseband anti-aliasing filters, connect the output labeled MIXOUTI to the input labeled BBINI through a coaxial cable and the intended filter. The filter must provide a DC signal path from MIXOUTI to BBINI. Follow the same procedure for the MIXOUTQ and BBINQ connections.
5) Connect the output labeled PLL TP to a frequency counter, an oscilloscope, or a spectrum analyzer, through a terminated 50Ω cable.
6) To characterize the time domain characteristics of the analog baseband signals, connect the output labeled BBOUTI to channel 1 of an oscilloscope through a terminated 50Ω cable, and connect the output labeled BBOUTQ to channel 2 of the same oscilloscope through a terminated 50Ω cable. This will facilitate analysis of the quadrature detection network.
7) To characterize the frequency domain characteristics of the analog baseband signal, connect the output labeled BBOUTI (or BBOUTQ) to a spectrum analyzer through a terminated 50Ω cable.
8) Connect the outputs labeled DATA OUT I, DATA CLK OUT, REF CLK OUT, and DATA OUT Q to a logic analyzer through a flexible 3MΩ cable with 2x20, 0.1" center female headers. Note that jumpers J2, J4, J6, and J8 are connected to ground to realize an efficient ground-return connection for the high-speed digital signals. The cable assembly should use alternating signal-ground assignments, connecting the data line's adjacent ground wire to the associated ground pin on the EV board. The cable assembly should be shielded. It is important that the grounded jumpers be connected as part of the logic analyzer interface cable.

### Initial Conditions

The MAX2101 EV kit comes tested and set to certain initial conditions, as stated in Table 1.

**Table 1. MAX2101 EV Kit Initial Conditions**

| PARAMETER | SETTING | ADJUSTMENT |
|---|---|---|
| External Oscillator In (P8) | 35MHz (LO = 560MHz) | C92 |
| Automatic Gain Control | Set for IF IN power of -30dBm | R50 |
| Filter Cutoff Frequency | 20MHz | R49 |
| Filter Temperature-Coefficient Adjustment | 0TC at 20MHz | R48 |
| Programmable Sample Rate | Maximum Sample Rate | S0, S1, S2 = 0 |
| Filter Select | Internal Filters | FLTRSEL = 0 |
| Offset Correction Enable | Enabled | ENOPB = GND |
| Data Format Select | Offset Binary | BINEN = 1 |

*Analysis*

1) Select all user settings (note that the EV board has been adjusted to the initial conditions found in Table 1): (a) ENOPB should normally be enabled, i.e. set to ground. (b) Determine the sample rate by setting S0, S1, and S2, referring to the Sample-Rate Control table (Table 1) in the MAX2101 data sheet. For maximum sample rate, set all inputs to logic low. (c) Select the baseband signal path (internal or external) by setting the FLTRSEL switch. For internal signal path, set FLTRSEL to logic low. For external signal path, set FLTRSEL to logic high. (d) Select the digitized baseband data format by setting BINEN. For twos-complement format, set BINEN to logic low. For offset binary format, set BINEN to logic high.

2) Establish LO: (a) Choose the desired LO frequency, $f_{LO}$; for this EV kit, the LO should be between 450MHz and 650MHz. The MAX2101 EV kit has been factory preset for a LO frequency of 560MHz. (b) Divide $f_{LO}$ by 16 to determine the External Reference Oscillator Frequency, $f_{REF}$:

$$f_{REF} = f_{LO} /16$$

(c) Apply $f_{REF}$ to the EXT'L OSC IN port, with a power level between -10dBm and 0dBm.

3) Establish the input and output signals: (a) Choose a baseband frequency, $f_{BB}$; for the MAX2101 EV kit, the frequency should be between 10kHz and 30MHz. (b) Determine the input frequency, $f_{IN}$, by adding or subtracting $f_{BB}$ from $f_{LO}$:

$$f_{IN} = f_{LO} \pm f_{BB}$$

(c) Choose a signal power for the input signal, $f_{IN}$; for the MAX2101, the power should be between -50dBm and -10dBm. (c) Apply $f_{IN}$ to the IFIN port.

4) Apply power to the board. Note the following supply sequence: (a) Turn on the +15V and -15V supplies. (b) Turn on the -5.2V supply. (c) Turn on the +5V supply. (d) Measure the voltage at Test Point 3, VREF; this voltage should be between 1.18V and 1.26V. (e) Adjust the variable capacitor, C92, until the frequency measured at the PLL TP output equals $f_{REF}$. (f) Verify the phase-locked loop is active by measuring the voltage at the output of the loop filter, at C13; this voltage should be between 0V and +11V. (g) If the loop is not locked, adjust capacitor C92, while periodically shorting the left node of VR100 to ground, until the loop locks. (h) Adjust the filters to ensure they are not attenuating the baseband signal by adjusting the FTUNE ADJUST potentiometer until the voltage measured on the rectangular pad next to R12 is greater than 3V. (i) Verify the correct baseband frequency by measuring the BBOUTI or BBOUTQ signal. (j) Adjust the AGC ADJUST potentiometer until the peak-to-peak amplitude of the signal at BBOUTI or BBOUTQ is 500mVp-p. (k) Adjust the FTUNE ADJUST potentiometer until the signals at BBOUTI and BBOUTQ are attenuated between 0% and 5%. (l) As a final check for proper operation, measure the voltage on OFFI by probing the left node of capacitor C97, and measure the voltage on OFFQ by probing the left node of capacitor C100. The measured voltages should be in the 1.5V to 3.5V range.

5) Acquire signals: (a) Measure all signals associated with DATA CLK OUT, DATA OUT I, and DATA OUT Q to verify proper logic levels. (b) Using the DATA CLK OUT signals as the synchronizing clock, acquire data at DATA OUT I and DATA OUT Q with a logic analyzer. Note the data frequency and edge

rate require proper high-speed design techniques to ensure proper data transmission. Each data pin has an associated ground pin. The data line should be AC terminated in the cable's characteristic impedance. Analysis may now be performed in the digital domain.

6) The analog quadrature demodulator front end may be analyzed by measuring signals at various ports. The analog baseband signals can be measured at the BBOUTI and BBOUTQ ports. The video amplifiers buffering BBOUTI and BBOUTQ can drive a ground referenced 50Ω load, such as a high-speed oscilloscope probe. The mixer output signals can be measured at MIXOUTI and MIXOUTQ. Select the external signal path with the FLTRSEL control to measure MIXOUTI and MIXOUTQ. The MAX2101 can drive a back-terminated AC-coupled impedance of 50Ω at this port. The AGC should be adjusted to provide -22dBm from MIXOUTI and MIXOUTQ, ensuring a full-scale signal at the BBINI and BBINQ ports. Measurements at these ports facilitate analysis of the IF front end and the quadrature demodulation networks, without adding effects due to baseband filters and amplifiers.

### *Resonator Shield*

The MAX2101 EV kit includes a shield to prevent EMI from pulling the resonator frequency or introducing noise into the resonator signal. You may attach the shield over the resonator network after setting the desired LO frequency (by adjusting C92). Attach the shield by (a) forming the shield following the indentations provided, and (b) soldering the shield to the grounded contact surrounding the resonator tank. If further adjustment of C92 is required, simply drill a hole into the shield, placed over the trimmer capacitor, with a diameter just large enough to allow insertion of a tool.

## Board Interface Descriptions

### *Power Supplies*

**+5V ±5%, 500mA.** Provides power for the MAX2101, the data buffers, and the single-supply op amps.

**-5.2V ±5%, 50mA.** Provides power for MC10116 line receiver and MC12040 phase frequency detector.

**Ground ±50mV.**

**+15V or -15V ±10%, 10mA.** Provides power for the phase-locked-loop op amp (AR6).

### *Inputs/Outputs*

**RF Input (P7).** Accepts a 400MHz to 700MHz signal, depending on the coarse setting of the resonant-tank variable capacitor. Signal level can be from -50dBm to -10dBm. Signal is DC referenced to ground, and is AC coupled through an impedance matching network to the MAX2101's IFIN input.

**I and Q Channel Mixer Outputs (MIXOUTI/Q) (P4, P5).** Intended to drive a lowpass filter, which drives the appropriate baseband input. Output is capable of driving 100Ω referenced to 2.4V.

**I and Q Channel Baseband Inputs (BBINI/Q) (P1, P6).** Accepts the filtered, downconverted signal from the appropriate mixer output port. Driving signal must be DC referenced to 2.4V. Signal level should be nominally 18mV, or -22dBm from a 50Ω source resistance.

**I and Q Channel Analog Baseband Outputs (BBOUTI/Q) (P2, P3).** The analog baseband signals prior to digitizing. The internal baseband signals are buffered, converted from differential to single-ended format, attenuated, and translated to ground reference. This signal is capable of driving 50Ω for ease of evaluation.

**LO Reference Oscillator In (P8).** This port accepts the external oscillator that determines the LO frequency. The LO frequency will be 16 times the reference signal frequency. To realize a LO frequency range of 400MHz to 700MHz, the external oscillator must supply a frequency range of 25MHz to 43.75MHz. The signal level should be between -7dBm and +5dBm from a 50Ω source resistance. The source should exhibit extremely low phase noise (better than -90dBc at 10kHz off the carrier) to ensure optimum phase-noise performance of the LO.

**Phase-Lock-Loop Test Point (P10).** Test point for examining the output of the MAX2101 prescaler. Capable of driving a low-impedance load directly ($R_L$ = 50Ω).

**Master Clock In (MCLK) (P9).** Port for accepting the master sample-clock signal. Signal level must be between 0dBm and +10dBm. Signal should exhibit low jitter characteristics (<40ps) to ensure proper sample jitter on the digitized data.

**Reference Clock Out (RCLK) (J7, J8).** Buffered output port from the MAX2101 providing a low-jitter replica of the master clock, divided by 6 in frequency. Output clock is in TTL/CMOS format.

**Data Clock Out (DCLK) (J1, J4).** Buffered output port from the MAX2101 providing the sample clock synchronized with the data. Data clock output is in differential TTL/CMOS format.

**Data Out I/Q (J2, J3, J5, J6).** Buffered output port from the MAX2101 providing the baseband digitized data for both I and Q channels. Data is in TTL/CMOS format.

*Adjustments*

**Automatic Gain Control (AGC) (R50).** A variable resistor sets the gain of the signal path. The variable gain adjusts for the signal level at the input (IFIN) to provide a full-scale signal to the ADCs.

**FTUNE Adjust (R49).** A potentiometer sets the voltage applied to a network to establish the cutoff frequency for the two internal lowpass filters. This adjustment sets both filters.

**TC Adjust (R48).** A variable resistor sets the temperature coefficient of the filter tuning network to compensate for the filters' temperature dependence. The 10kΩ potentiometer is used as a variable resistor. This resistor should be adjusted to 0Ω for a zero temperature coefficient at 20MHz cutoff frequency.

**Resonant Tank Trim (C92).** A variable capacitor establishes the coarse setting of the LO frequency.

*User-Selectable Settings*

**Programmable Sample Rate (S0, S1, S2).** The ADC sample rate is determined by the frequency of the master clock and the programmable sample-rate prescaler. The setting of this prescaler is determined by the logic levels set by toggle switches S0, S1, and S2, according to the Sample-Rate Control table (Table 1) in the MAX2101 data sheet.

**Filter Select (FLTRSEL).** The FLTRSEL logical input selects the signal path of the baseband signal out of the quadrature detection mixers. Logic level 0 (low) enables the internal signal path, through the internal lowpass filters. At this setting, MIXOUTI and MIXOUTQ are disabled. Logic level 1 (high) enables MIXOUTI and MIXOUTQ, and disables the internal signal path.

**Offset Correction Enable (ENOPB).** This input enables the internal op amps in the offset correction networks. ENOPB at 0V enables the op amps, while ENOPB at 5V disables the op amps.

**Data Format Select (Binary Enable) (BINEN).** This input selects the output data format. Logic level 0 (low) selects the twos-complement format, while logic level 1 (high) selects an offset binary format.

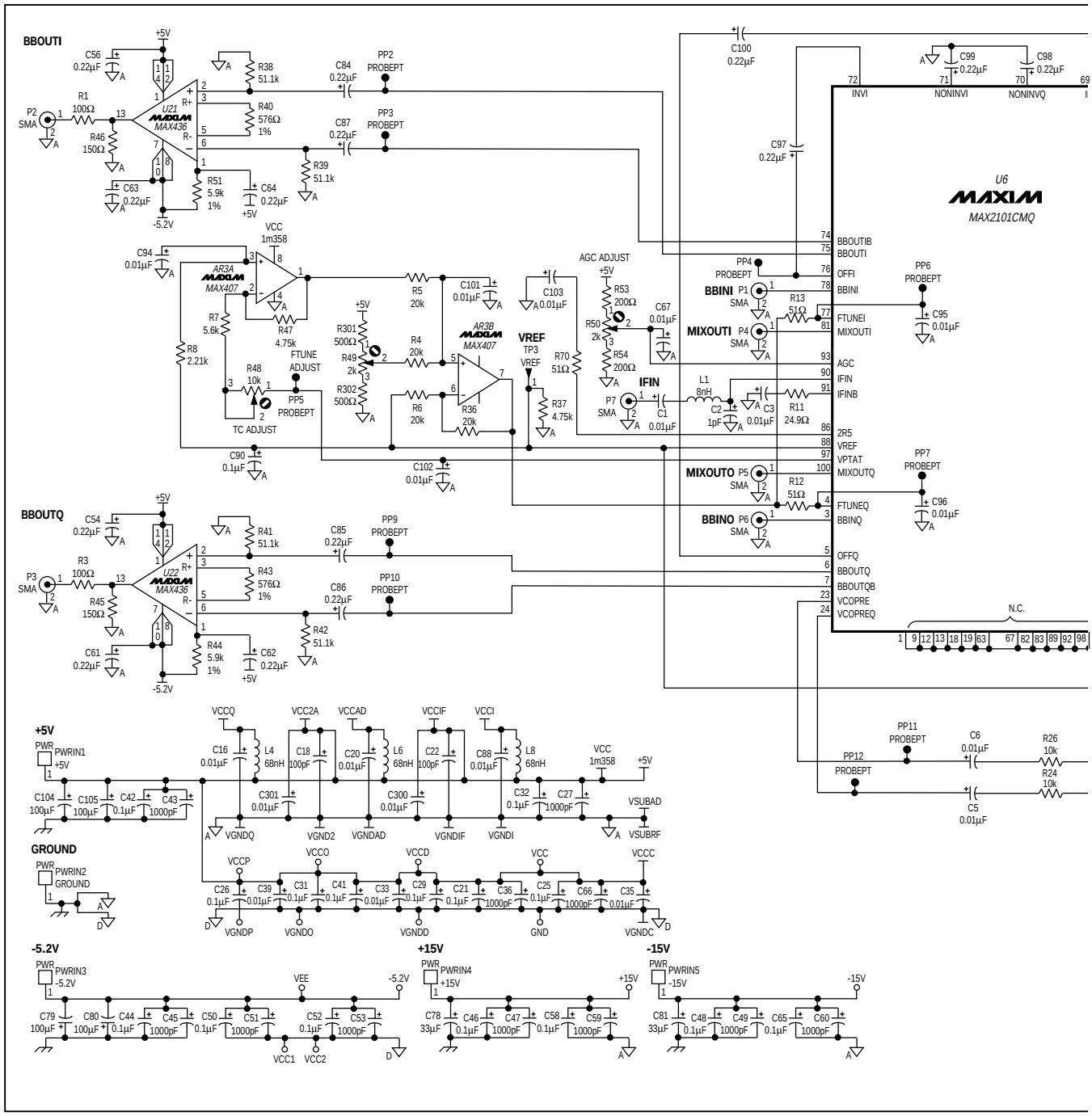
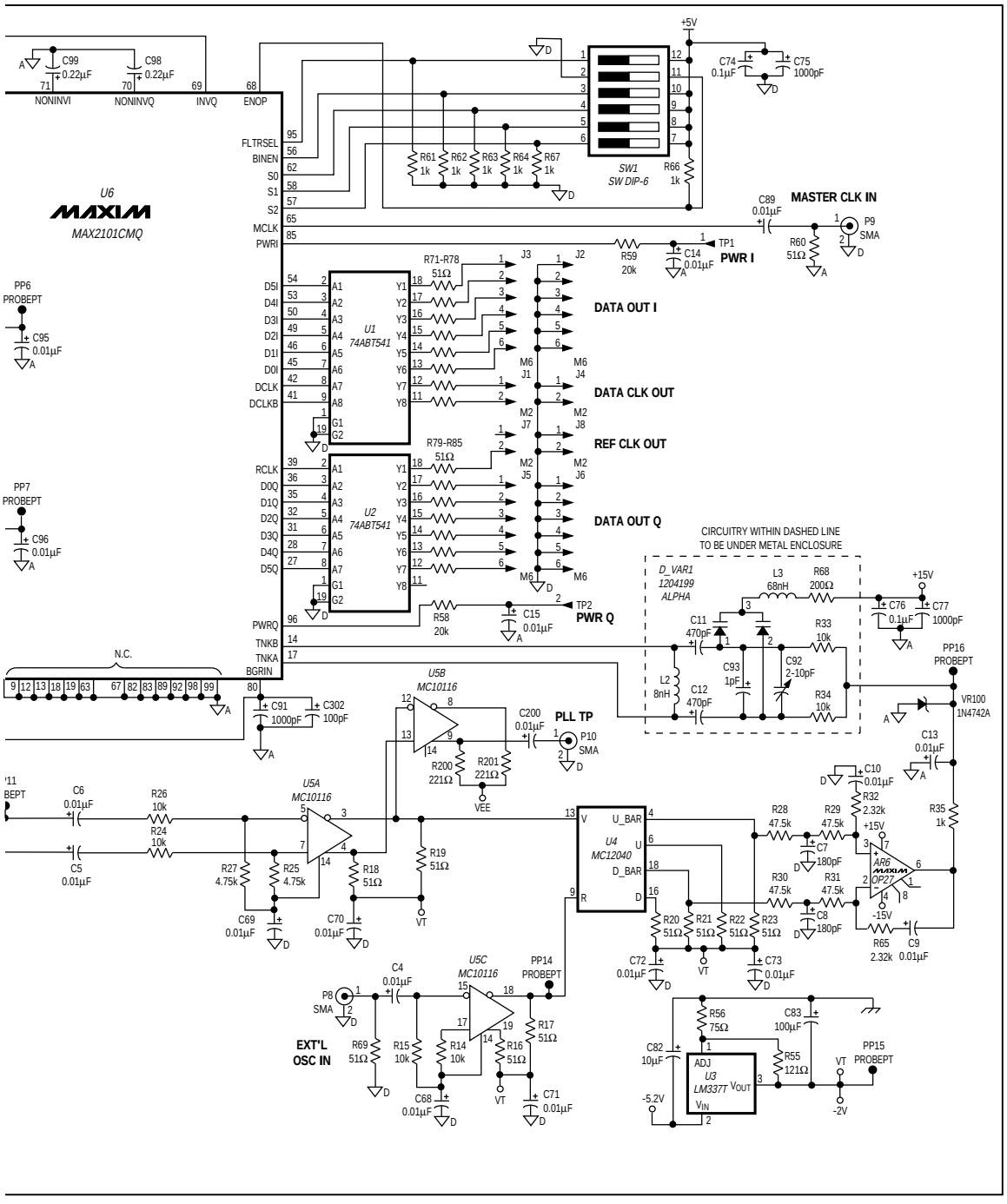



*Figure 1. MAX2101 EV Kit Schematic*


U6
MAXIM
MAX2101CMQ
NONINVI
NONINVQ
INVQ
ENOP
FLTRSEL
BINEN
S0
S1
S2
MCLK
PWRI
PWRQ
TNKB
TNKA
BGRIN
N.C.
SW1
SW DIP-6
+5V
MASTER CLK IN
P9
SMA
TP1
PWR I
TP2
PWR Q
DATA OUT I
DATA CLK OUT
REF CLK OUT
DATA OUT Q
U1
74ABT541
U2
74ABT541
PP6
PROBEPT
PP7
PROBEPT
PP14
PROBEPT
PP15
PROBEPT
PP16
PROBEPT
CIRCUITRY WITHIN DASHED LINE
TO BE UNDER METAL ENCLOSURE
D_VAR1
1204199
ALPHA
VR100
1N4742A
PLL TP
P10
SMA
U5B
MC10116
U5A
MC10116
U5C
MC10116
U4
MC12040
U_BAR
D_BAR
EXT'L
OSC IN
P8
SMA
U3
LM337T
ADJ
VOUT
VIN
-5.2V
-2V
+15V
-15V
VEE
VT
AR6
OP27

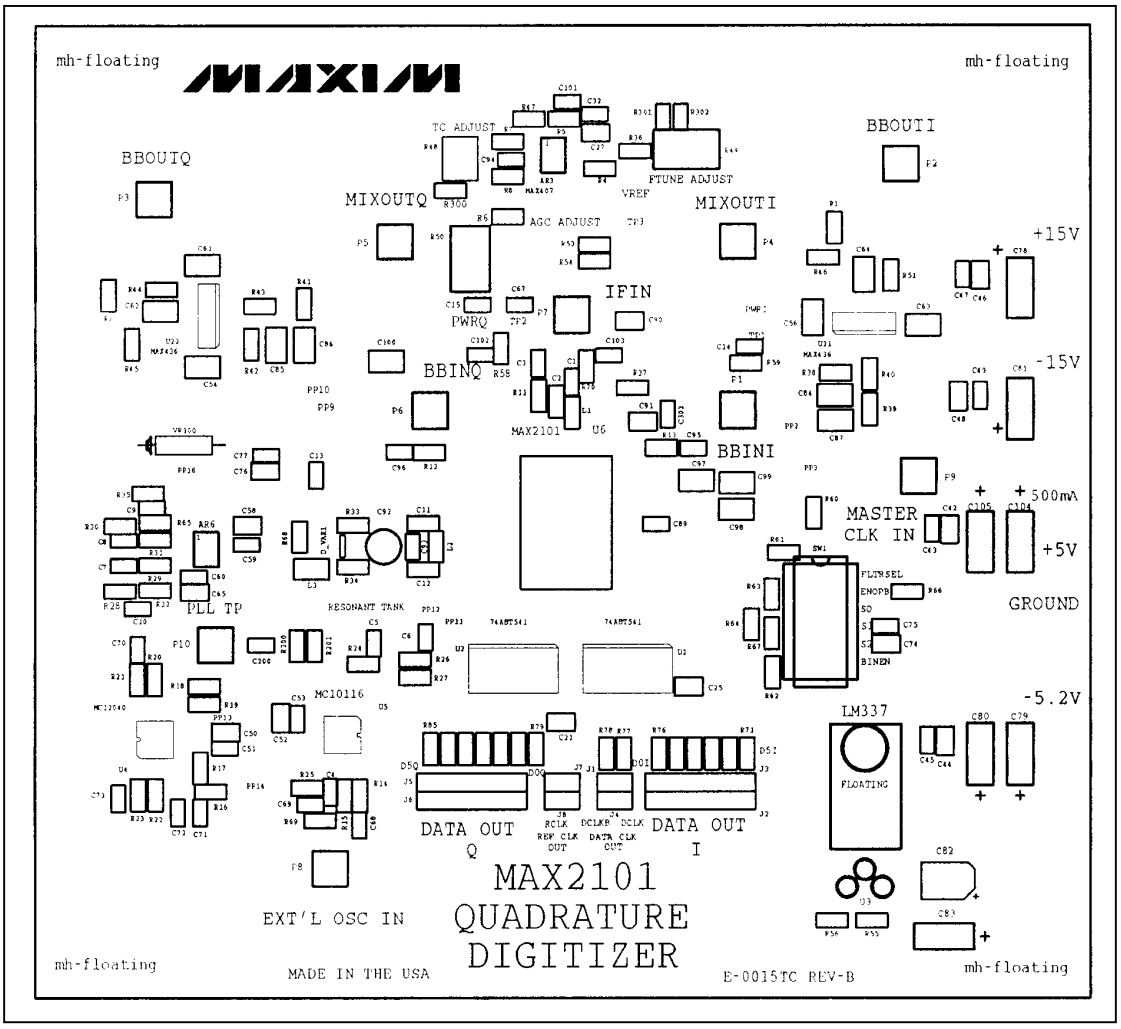



*Figure 2. MAX2101 EV Kit Component Placement Guide—Component Side (Positive Image)*

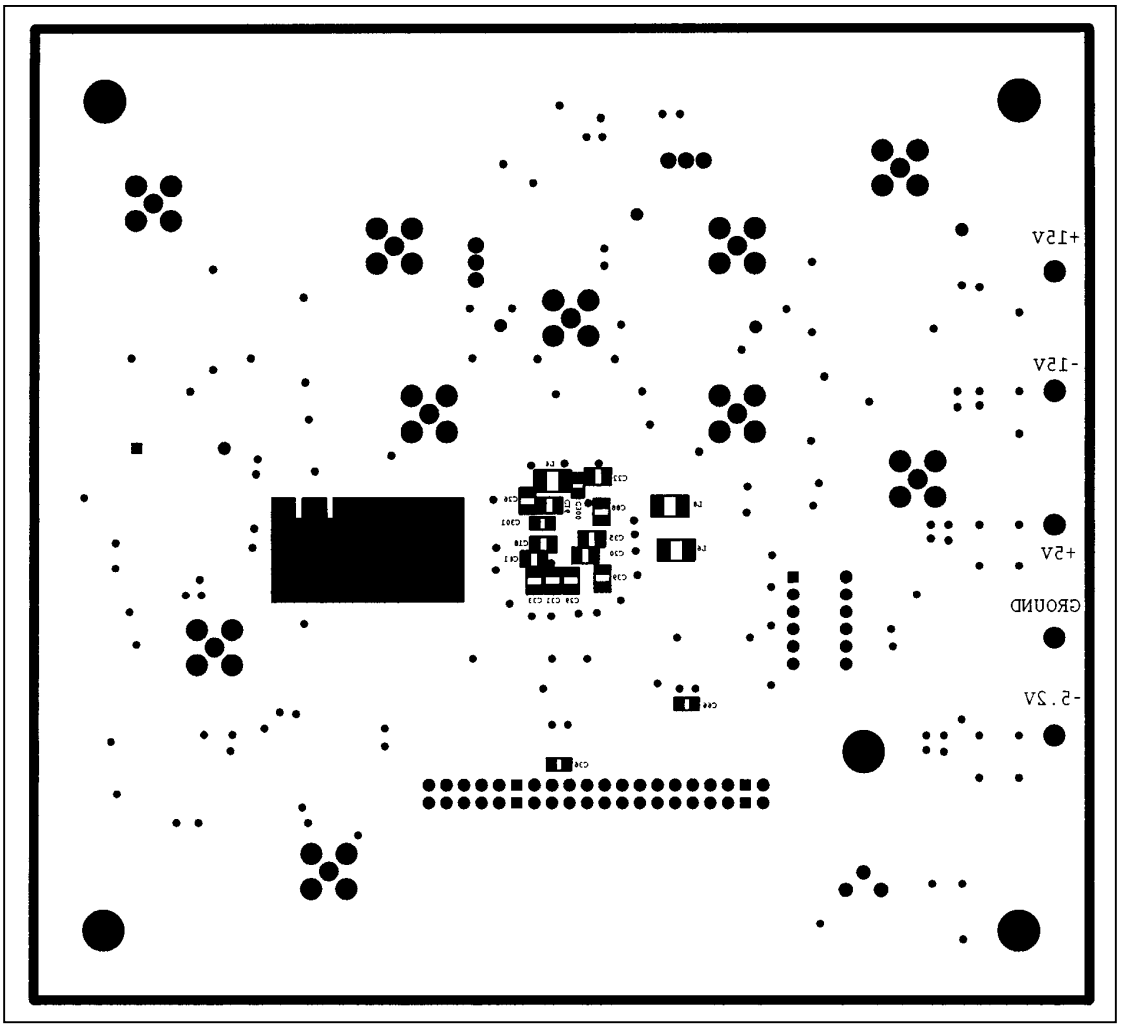



*Figure 3. MAX2101 EV Kit Component Placement Guide—Solder Side (Positive Image)*

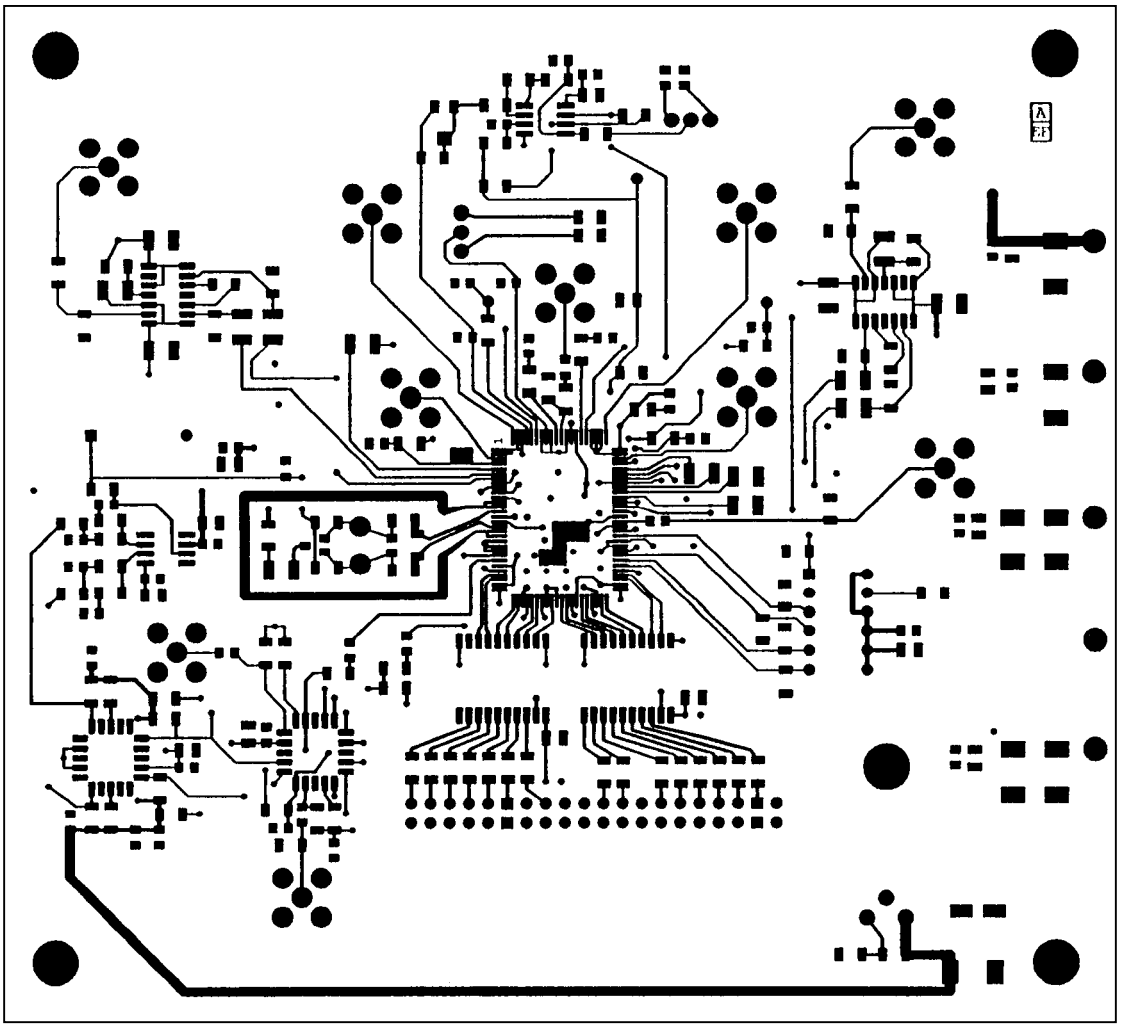


*Figure 4. MAX2101 EV Kit PC Board Layout—Component Side (Positive Image)*

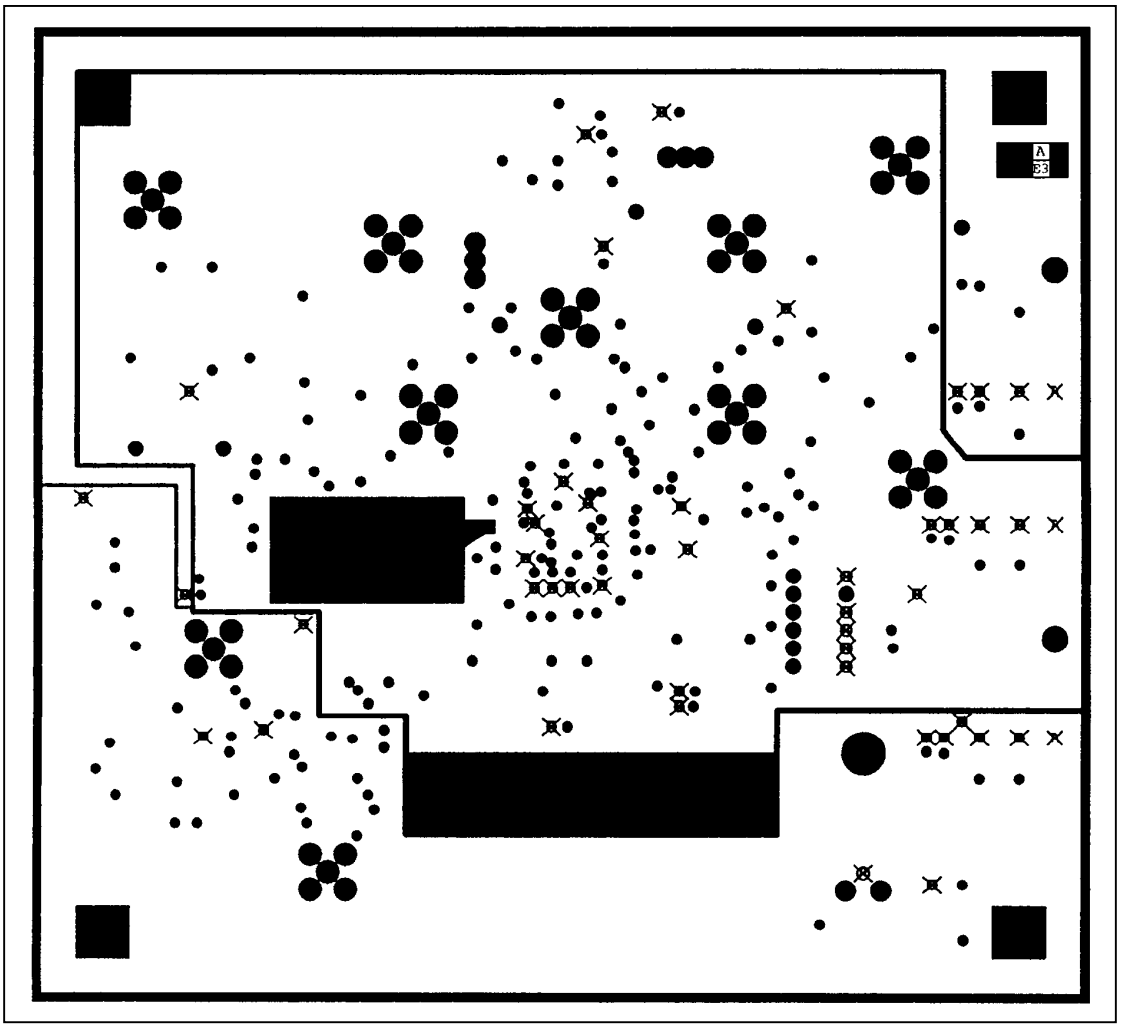


*Figure 5. MAX2101 EV Kit PC Board Layout—Supply Plane (Negative Image)*

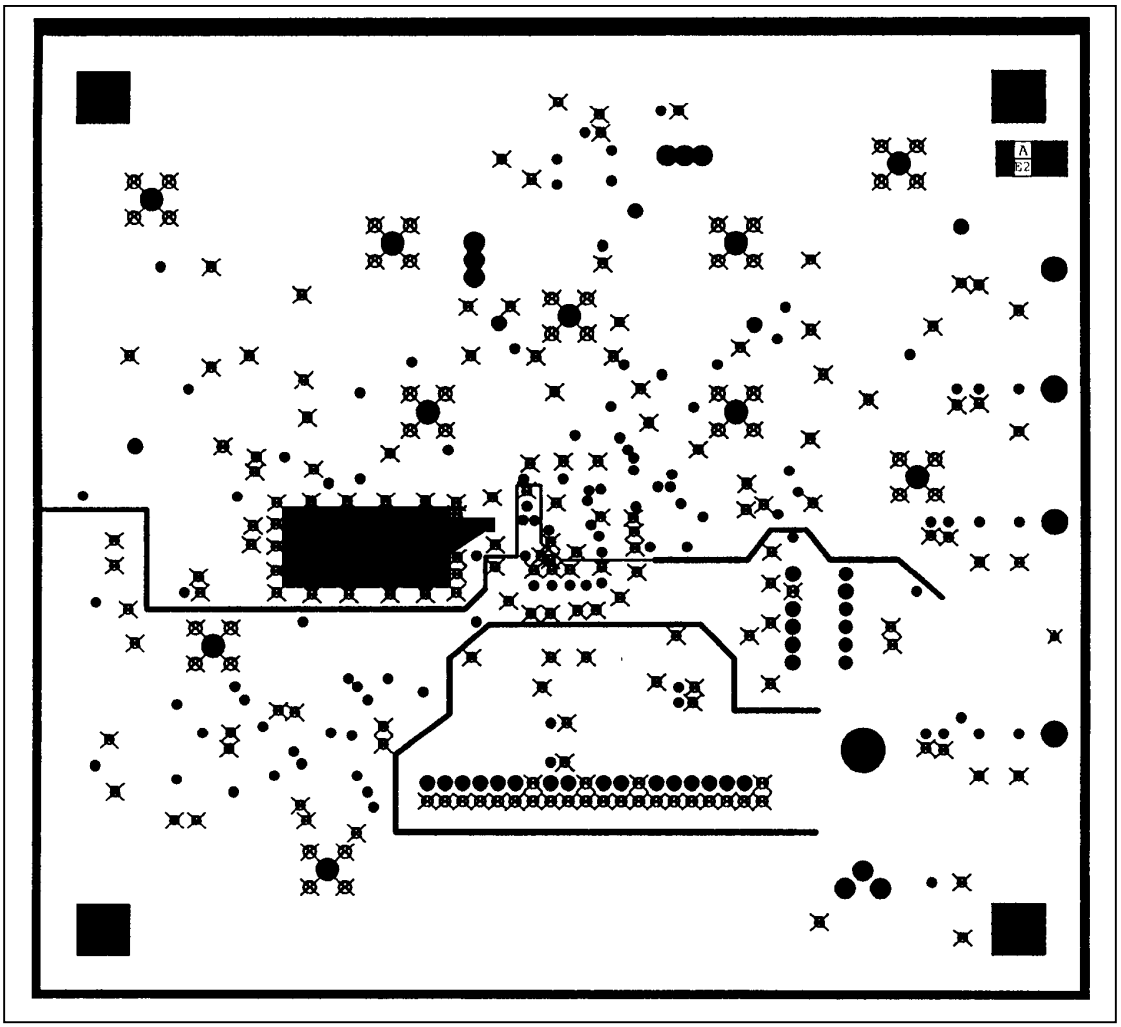


*Figure 6. MAX2101 EV Kit PC Board Layout—Ground Plane (Negative Image)*

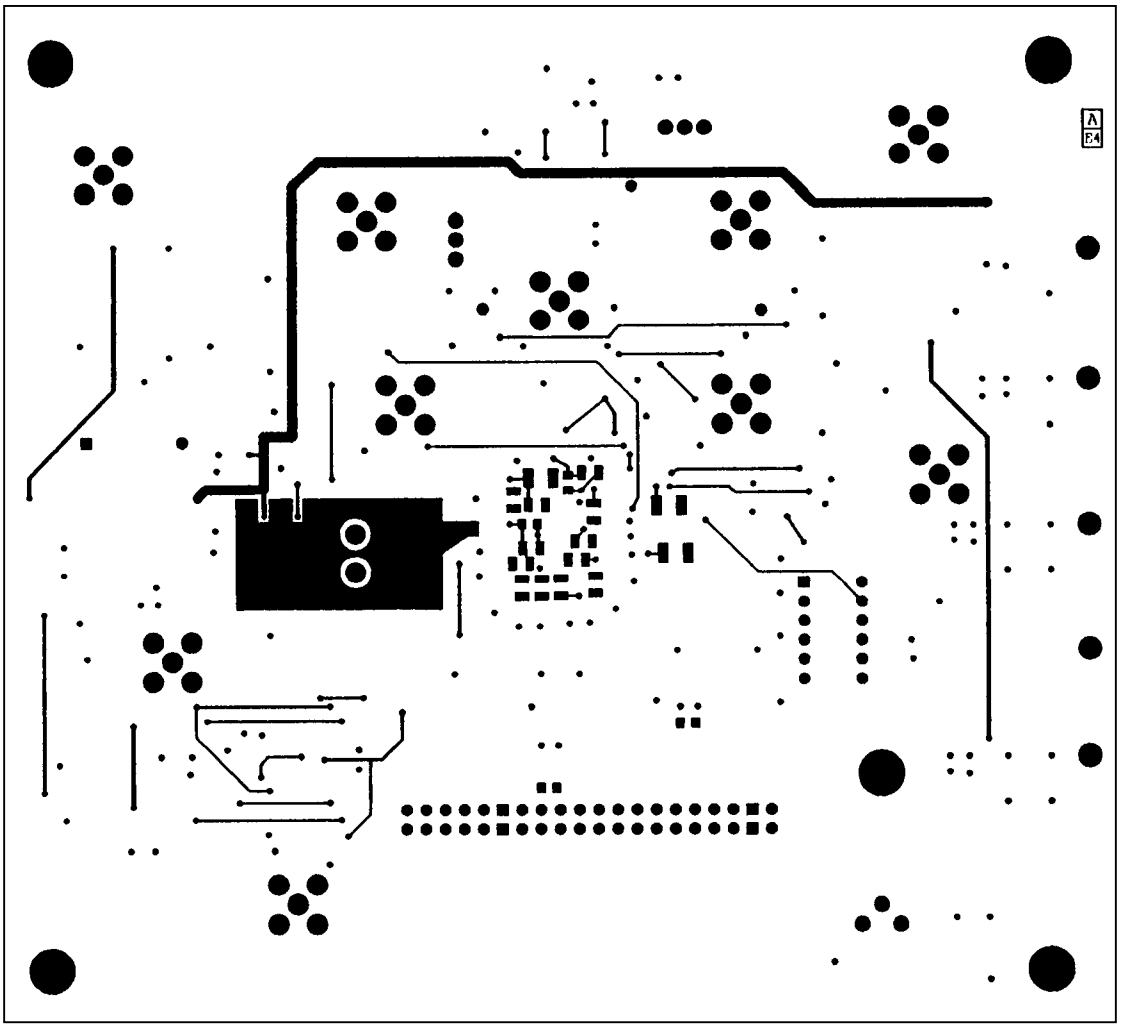


*Figure 7. MAX2101 EV Kit PC Board Layout—Solder Side (Positive Image)*

# 1994 EVALUATION KIT DATA BOOK FAXBACK OFFER


Accelerate your time to market with Maxim's evaluation kits (EV kits) that simplify design-in and prototyping. For your convenience, the *1994 Evaluation Kit Data Book* includes EV kit manuals and corresponding data sheets covering 95 products in one easy-to-use book. To receive your free data book, simply FAX this response card to your nearest Maxim office, or call toll-free 1-800-998-8800 (in the US only) for prompt fulfillment. We look forward to serving you.

FAX NUMBERS:

| | | | | | |
|---|---|---|---|---|---|
| **US** | (408) 737-7194 | **Italy** | (02) 99041981 | **Japan** | (03) 3232-6149 |
| **UK** | (01734) 305577 | **France** | (1) 30 64 73 48 | **Taiwan** | (35) 777659 |
| **Germany (Maxim GmbH)** | (089) 8544239 | | | | |

My application is: __| __| __| __| __| __| __| __| __| __| __| __| __| __| __| __| __| __| __| __| __| __| __| __| __| __|

My end product is: __| __| __| __| __| __| __| __| __| __| __| __| __| __| __| __| __| __| __| __| __| __| __| __| __| __|

Name _____ Title _____

Company _____

Address _____

City _____ State _____ Zip _____ Phone# _____

MAX2101 EV DS REV 0