Am25LS2568/Am25LS2569

Four-Bit Up/Down Counters with Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- 4-bit synchronous counter, synchronously programmable
- Both synchronous and asynchronous clear inputs
- Three-state counter outputs interface directly with bus organized systems
- Internal look-ahead carry logic and two count enable lines for high speed cascaded operation
- Ripple carry output for cascading
- Clock carry output for convenient modulo configuration
- Fully buffered outputs
- Second sourced as the 54LS/74LS568 and LS569
- Advanced Low-Power Schottky technology

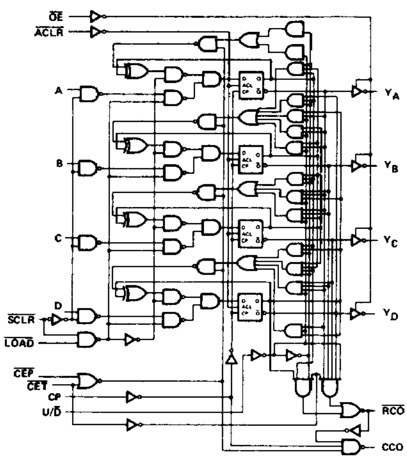
GENERAL DESCRIPTION

The Am25LS2568 and Am25LS2569 are programmable up/down BCD and Binary counters respectively with three-state outputs for bus organized systems. All functions except output enable ($\overline{OE}$) and asynchronous clear ($\overline{ACLR}$) occur on the positive edge of the clock input (CP).

With the $\overline{LOAD}$ input LOW, the outputs will be programmed by the parallel data inputs (A, B, C, D) on the next clock edge. Counting is enabled only when $\overline{CEP}$ and $\overline{CET}$ are LOW and LOAD is HIGH. The up-down input (U/$\overline{D}$) controls the direction of count, HIGH counts up and LOW counts down. Internal look-ahead carry logic and an active LOW ripple carry output ($\overline{RCO}$) allows for high-speed counting and cascading. During up-count, the $\overline{RCO}$ is LOW at binary 9 for the LS2568 (binary 15 for the LS2569) and upon down-count, it is LOW at binary 0. Normal cascaded operations require only the $\overline{RCO}$ to be connected to the succeeding block at $\overline{CET}$. When counting, the clocked carry output (CCO) provides a HIGH-LOW-HIGH pulse for a duration equal to the LOW time of the clock pulse and only when $\overline{RCO}$ is LOW. Two active LOW reset lines are available, synchronous clear ($\overline{SCLR}$) and a master reset asynchronous clear ($\overline{ACLR}$). The output control ($\overline{OE}$) input forces the counter output into the high-impedance state when HIGH and when LOW, the counter outputs are enabled.

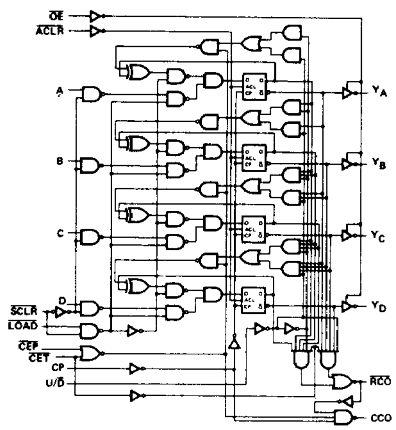
BLOCK DIAGRAM

Am25LS2568 (BCD)



BD001430

Am25LS2569 (BINARY)



BD001420

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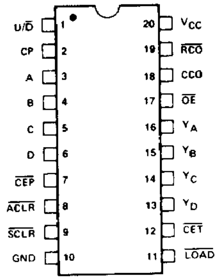
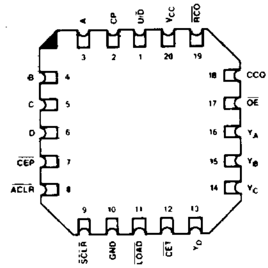
CONNECTION DIAGRAM
Top View

D-20-1



CD001640

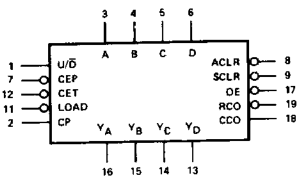
L-20-1



CD001650

Note: Pin 1 is marked for orientation

LOGIC SYMBOL



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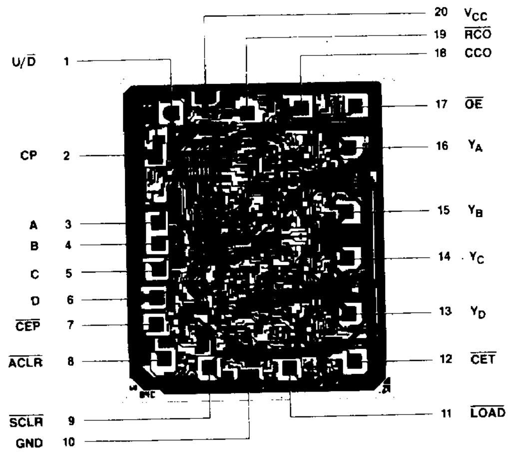
METALLIZATION AND PAD LAYOUT
Am25LS2568



DIE SIZE 0.087" x 0.103"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am25LS2568/69 D C B

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (−55°C to +125°C)
- **D** — Package
  - D – 20-pin CERDIP
  - F – 20-pin flatpak
  - L – 20-pin leadless chip carrier
  - P – 20-pin plastic DIP
  - X – Dice
- **Am25LS2568/69** — Device type
  - BCD and Binary Counters

Valid Combinations	
Am25LS2568/ Am25LS2569	DC, DCB, DM, DMB FM, FMB LC, LM, LMB PC, PCB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

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PIN DESCRIPTION

Pin No.	Name	I/O	Description
3, 4, 5, 6	A, B, C, D	I	The four programmable data inputs.
7	$\overline{CEP}$	I	Count Enable Parallel. Can be used to enable and inhibit counting in high speed cascaded operation. $\overline{CEP}$ must be LOW to count.
12	$\overline{CET}$	I	Count Enable Trickle. Enables the ripple carry output for cascaded operation. Must be LOW to count.
2	CP	I	Clock Pulse. All synchronous functions occur on the LOW-to-HIGH transition of the clock.
11	$\overline{LOAD}$	I	Enables parallel load of counter outputs from data inputs on the next clock edge. Must be HIGH to count.
1	$U/\overline{D}$	I	Up/Down Count Control. HIGH counts up and LOW counts down.
8	$\overline{ACLR}$	I	Asynchronous Clear. Master reset of counters to zero when $\overline{ACLR}$ is LOW, independent of the clock.
9	$\overline{SCLR}$	I	Synchronous clear of counters to zero on the next clock edge when $\overline{SCLR}$ is LOW.
17	$\overline{OE}$	I	A HIGH on the output control sets the four counter outputs in the high-impedance, and a LOW enables the output.
16, 15 14, 13	Y_A, Y_B, Y_C, Y_D	O	The four counter outputs.
19	$\overline{RCO}$	O	Ripple Carry Output. Output will be LOW on the maximum count on up-count. Upon down-count, $\overline{RCO}$ is LOW at 0000.
18	CCO	O	Clock Carry Output. While counting and $\overline{RCO}$ is LOW, CCO will follow the clock HIGH-LOW-HIGH transition.

Am25LS2568/2569
FUNCTION TABLE

	INPUTS												OUTPUTS					
MODE	LOAD	CEP	CET	$U/\overline{D}$	ASYNC CLEAR	SYNC CLEAR	$\overline{OE}$(1)	D_0	D_1	D_2	D_3	CP	Q_0	Q_1	Q_2	Q_3	RC	CLOCK CARRY
Clear (ASYNC)	X	X	X	1	0	X	0	X	X	X	X	X	0	0	0	0	1	1
	X	X	X	0	0	X	0	X	X	X	X	X	0	0	0	0	0	¯_¯ (2)
Clear (SYNC)	X	X	X	1	1	0	0	X	X	X	X	↑	0	0	0	0	1	1
	X	X	X	0	1	0	0	X	X	X	X	↑	0	0	0	0	0	¯_¯ (2)
Load	0	X	1	X	1	1	0	X	X	X	X	↑	$Q_n = D_n$				1	1
	0	X	0	0	1	1	0	0	0	0	0	↑	0	0	0	0	0	¯_¯ (2)
	0	X	0	1	1	1	0	1	1	1	1(3)	↑	1	1	1	1(3)	0	¯_¯ (2)
Count Up	1	0	0	1	1	1	0	X	X	X	X	↑	Q_{n+1}				(4)	(5)
Count Down	1	0	0	0	1	1	0	X	X	X	X	↑	Q_{n-1}				(6)	(5)
Inhibit	1	0	1	X	1	1	0	X	X	X	X	↑	N.C.				N.C.	1
	1	1	0	X	1	1	0	X	X	X	X	↑	N.C.				N.C.	1
	1	1	1	X	1	1	0	X	X	X	X	↑	N.C.				N.C.	1
Output Disable	X	X	X	X	X	X	1	X	X	X	X	X	Z	Z	Z	Z	N.C.	N.C.

↑ = CLOCK LOW-to-HIGH transition
X = Don't Care
D_n = D_0 thru D_3 input level prior to clock transition
Q_{n+1} = Next higher count in binary sequence
Q_{n-1} = Next lower count in binary sequence
N.C. = No change

Notes:
1. Register performs all correct logic for any state of $\overline{OE}$, but $\overline{OE}$ = 0 to view outputs.
2. Follows CLOCK if CET = CEP = 0, otherwise remains HIGH.
3. 1001 for LS68.
4. LOW for one full CLOCK cycle when maximum count is reached, otherwise remains HIGH.
5. Follows CLOCK when RC = 0.
6. LOW for one full CLOCK cycle when minimum count is reached, otherwise remains HIGH.

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Refer to Page 13-1 for Essential Information on Military Devices

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... −65°C to +150°C
Ambient Temperature Under Bias .... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous .... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State .... −0.5V to $+V_{CC}$ max
DC Input Voltage .... −0.5V to +7.0V
DC Output Current, Into Outputs 30mA
DC Input Current .... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature .... 0°C to +70°C
Supply Voltage .... +4.75V to +5.25V
Military (M) Devices
Temperature .... −55°C to +125°C
Supply Voltage .... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)				Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	Y_i	MIL, I_{OH} = −1.0mA		2.4	3.4		Volts
				COM'L, I_{OH} = −2.6mA		2.4	3.2		
			$\overline{RCO}$, CCO	I_{OH} = −440μA	MIL	2.5	3.4		
					COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}		I_{OL} = 4.0mA				0.4	Volts
				I_{OL} = 8.0mA				0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs				2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs.			MIL			0.7	Volts
					COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA						−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V		$\overline{ACLR}$, $\overline{OE}$, U/$\overline{D}$, $\overline{LOAD}$				−0.3	mA
				A, B, C, D, CP, $\overline{CEP}$				−0.4	
				$\overline{CET}$, $\overline{SCLR}$				−0.65	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V						20	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 7.0V						0.1	mA
I_{OZ}	Off-State (High-Impedance) Output Current	V_{CC} = MAX		V_O = 0.4V				−20	μA
				V_O = 2.4V				20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX				−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX					28	43	mA

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. $\overline{OE}$ = HIGH, all other inputs = GND, all outputs open.

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Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING CHARACTERISTICS ($T_A = +25°C$, $V_{CC} = 5.0V$)

Parameters	Description		Test Conditions	Min	Typ	Max	Units
t_{PLH}	Clock to Any Q; $\overline{Load}$ = LOW		$C_L = 15pF$ $R_L = 2.0k\Omega$		12	18	ns
t_{PHL}					14	21	
t_{PLH}	Clock to Any Q; $\overline{Load}$ = HIGH				12	18	ns
t_{PHL}					14	21	
t_{PLH}	$\overline{CET}$ to $\overline{RCO}$				11	16	ns
t_{PHL}					6	10	
t_{PLH}	U/$\overline{D}$ to $\overline{RCO}$				15	23	ns
t_{PHL}					13	20	
t_{PLH}	Clock to $\overline{RCO}$				24	35	ns
t_{PHL}					18	26	
t_{PLH}	Clock to $\overline{CCO}$				10	15	ns
t_{PHL}					10	15	
t_{PLH}	$\overline{CET}$ or $\overline{CEP}$ to $\overline{CCO}$				10	15	ns
t_{PHL}					17	25	
t_{PLH}	$\overline{ACLR}$ to Any Q				N.A.	N.A.	ns
t_{PHL}					17	26	
t_s	Set-up	A, B, C, D		22			ns
		$\overline{SCLR}$		20			
		$\overline{Load}$		30			
		U/$\overline{D}$		30			
		$\overline{CET}$, $\overline{CEP}$		25			
t_s	$\overline{SCLR}$ Recovery (inactive) to Clock			30			ns
t_h	Data Hold			0			ns
f_{max}	Maximum Clock Frequency (Note 1)			25	40		MHz
t_{pw}	Clock Pulse Width			25			ns
t_{PZH}	$\overline{OE}$ to Any Q; Enable					11	ns
t_{PZL}						19	
t_{PHZ}	$\overline{OE}$ to Any Q; Disable		$C_L = 5.0pF$ $R_L = 2.0k\Omega$			18	ns
t_{PLZ}						24	

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

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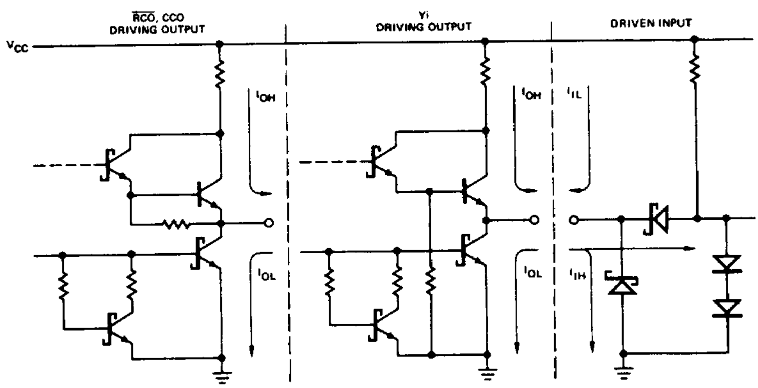
Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

Parameters	Description	Test Conditions	COMMERCIAL Am25LS Min	COMMERCIAL Am25LS Max	MILITARY Am25LS Min	MILITARY Am25LS Max	Units
t_{PLH}	Clock to Any Q; $\overline{Load}$ = LOW	C_L = 50pF, R_L = 2.0KΩ		22		24	ns
t_{PHL}				29		35	
t_{PLH}	Clock to Any Q; $\overline{Load}$ = HIGH			22		24	ns
t_{PHL}				29		35	
t_{PLH}	$\overline{CET}$ to $\overline{RCO}$			18		19	ns
t_{PHL}				17		21	
t_{PLH}	U/$\overline{D}$ to $\overline{RCO}$			26		28	ns
t_{PHL}				26		30	
t_{PLH}	Clock to $\overline{RCO}$			39		40	ns
t_{PHL}				34		39	
t_{PLH}	Clock to CCO			17		18	ns
t_{PHL}				22		27	
t_{PLH}	$\overline{CET}$ or $\overline{CEP}$ to CCO			16		17	ns
t_{PHL}				36		45	
t_{PLH}	$\overline{ACLR}$ to Any Q			N.A.		N.A.	ns
t_{PHL}				37		45	
t_s	Set-up: A, B, C, D		29		35		ns
	Set-up: $\overline{SCLR}$		25		30		
	Set-up: $\overline{Load}$		38		45		
	Set-up: U/$\overline{D}$		38		45		
	Set-up: $\overline{CET}$, $\overline{CEP}$		33		40		
t_s	SCLR Recovery (inactive) to Clock		39		50		ns
t_h	Data Hold		0		5		ns
f_{max}	Maximum Clock Frequency (Note 1)		20		18		MHz
t_{pw}	Clock Pulse Width		31		37		ns
t_{ZH}	$\overline{OE}$ to Any Q; Enable			16		20	ns
t_{ZL}				26		34	
t_{HZ}	$\overline{OE}$ to Any Q; Disable	C_L = 5.0pF, R_L = 2.0KΩ		20		22	ns
t_{LZ}				30		36	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.
N.A. not applicable.

Am25LS2568/2569 LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



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Note: Actual current flow direction shown.

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