

Receive Dual Low Noise Amplifier/Mixer

Description

The CXG1109EN is a receive dual low noise amplifier/mixer MMIC. This IC is designed using the Sony's GaAs J-FET process.

Features

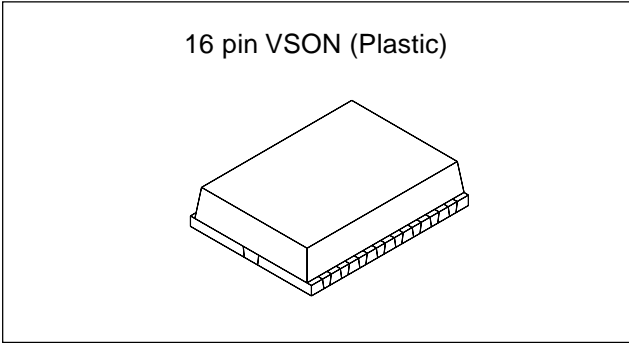
- High conversion gain: $G_p = 16.5$ to 17 dB (LNA Typ.)
 $G_c = 9.5$ to 10 dB (MIX Typ.)
- Low noise figure: $NF = 1.5$ dB (LNA Typ.)
 $NF = 4$ to 5 dB (MIX Typ.)
- Single 3V power supply operation
- Low LO input power operation $P_{LO} = -12.5$ dBm
- Single CTL pin achieved by the built-in inverter circuit
- 16-pin VSON package

Applications

800MHz Japan digital cellular telephones (PDC)

Structure

GaAs J-FET MMIC



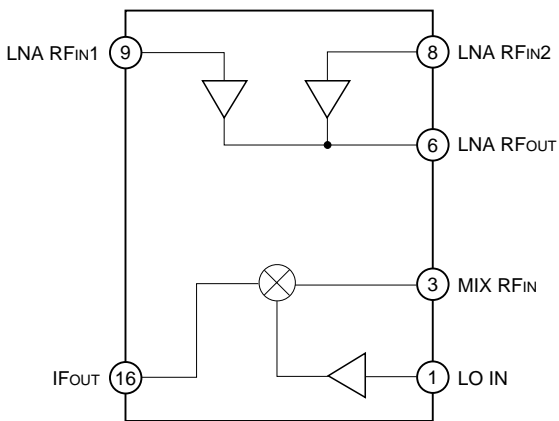
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V _{DD}	4.5	V
• Input power	P _{IN}	+13	dBm
• Current consumption	I _{DD}	15	mA
• Operating temperature	T _{opr}	-35 to +85	°C
• Storage temperature	T _{stg}	-65 to +150	°C

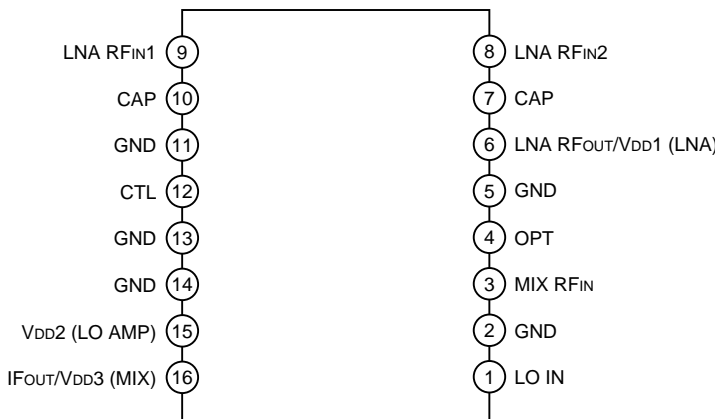
Recommended Operating Voltages

• Supply voltage	V _{DD}	2.7 to 3.3	V
• Control voltage	V _{CTL} (H)	2.4 to 3.3	V
	V _{CTL} (L)	0 to 0.3	V

Block Diagram



Pin Configuration



GaAs MMICs are ESD sensitive devices. Special handling precautions are required.

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Electrical Characteristics

Conditions: $V_{DD} = 3.0V$, $V_{CTL} (H) = 3.0V$, $V_{CTL} (L) = 0V$, $f_{RF1} = 885MHz$, $f_{RF2} = 810MHz$, $f_{LO} = f_{RF} - 130MHz$, $P_{LO} = -12.5dBm$, $T_a = 25^{\circ}C$, unless otherwise specified

Low Noise Amplifier Block

Item	Symbol	Path	RF frequency	V_{CTL}	Min.	Typ.	Max.	Unit	Measurement condition
Current consumption	I_{DD}	—	—	H	—	1.9	2.5	mA	When no signal
			—	L	—	1.9	2.5		
Control current	I_{CTL}	—	—	H	—	55	80	μA	
			—	L	-1	0	—		
Power gain	G_p	$RF_{IN1} \rightarrow RF_{OUT}$	f_{RF1}	H	15	16.5	19	dB	When a small signal
				L	—	-20	-15		
		$RF_{IN2} \rightarrow RF_{OUT}$	f_{RF2}	H	—	-26	-21		
				L	15	17	19		
Noise figure	NF	$RF_{IN1} \rightarrow RF_{OUT}$	f_{RF1}	H	—	1.5	2	dB	
		$RF_{IN2} \rightarrow RF_{OUT}$	f_{RF2}	L	—	1.5	2		
Input IP3	IIP3	$RF_{IN1} \rightarrow RF_{OUT}$	f_{RF1}	H	-11	-7.5	—	dBm	*1
		$RF_{IN2} \rightarrow RF_{OUT}$	f_{RF2}	L	-12.5	-9	—		
Isolation	ISO	$RF_{OUT} \rightarrow RF_{IN1}$	f_{RF1}	H	17	22	—	dB	When a small signal
		$RF_{OUT} \rightarrow RF_{IN2}$	f_{RF2}	L	18	23	—		

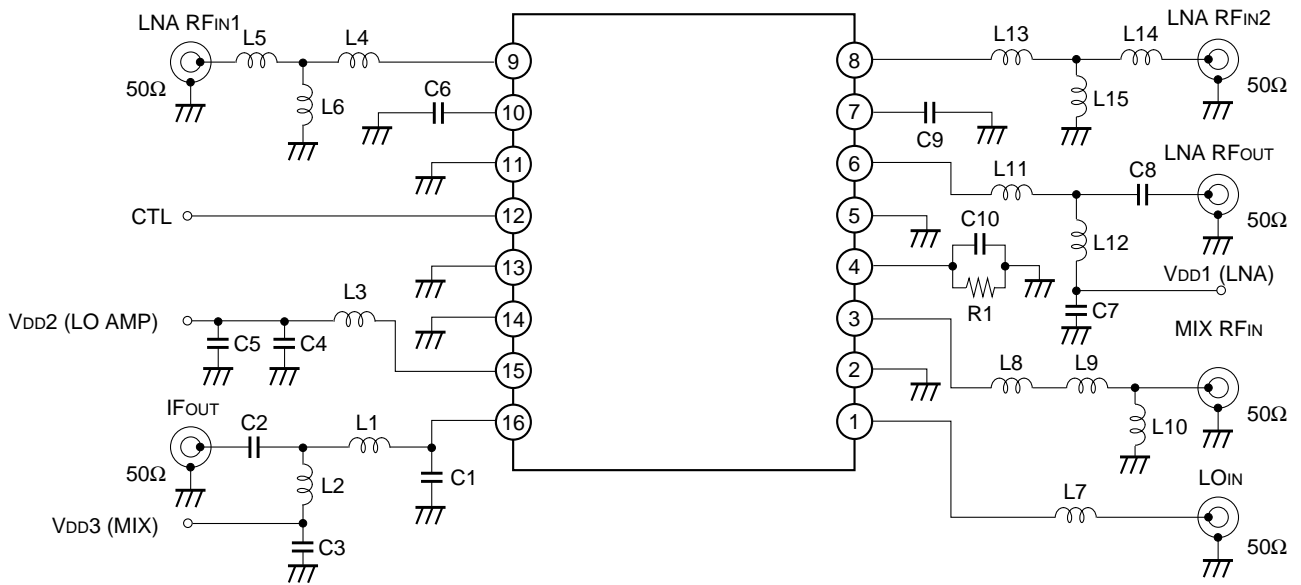
Mixer Block

Item	Symbol	RF frequency	Min.	Typ.	Max.	Unit	Measurement condition
Current consumption	I_{DD}	—	—	4.5	6.2	mA	When no signal
Power gain	G_c	f_{RF1}	9	10	11.5	dB	When a small signal
		f_{RF2}	8.5	9.5	11		
Noise figure	NF	f_{RF1}	—	5	6.5	dB	
		f_{RF2}	—	4	5.5		
Input IP3	IIP3	f_{RF1}	-1	1.5	—	dBm	*1
		f_{RF2}	-1.5	1.5	—		
LO to RF leak level	PIk	f_{RF1}	—	-22	-17	dBm	$f_{LO} = 755MHz$
		f_{RF2}	—	-24	-19		$f_{LO} = 680MHz$

The values shown above are the specified values on the Sony's recommended evaluation board.

*1 Conversion from the IM3 suppression ratio for two-wave input: PRF = -30dBm (low noise amplifier block)/ -22.5dBm (mixer block) at $f_{RFOffset} = 100kHz$.

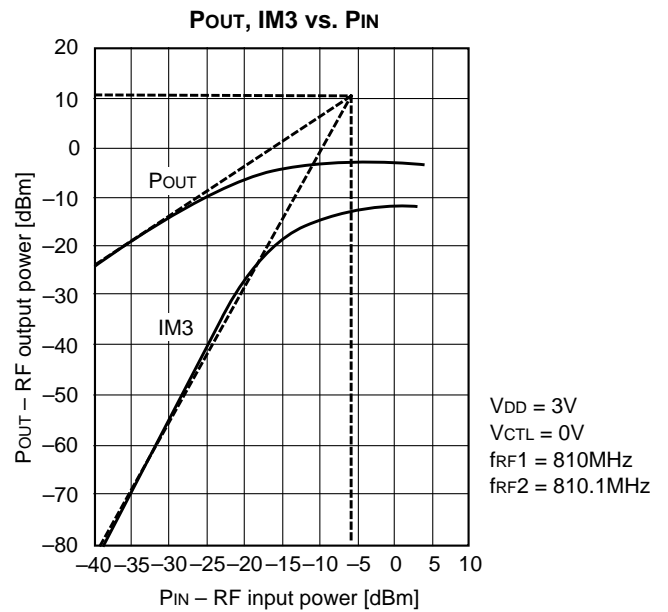
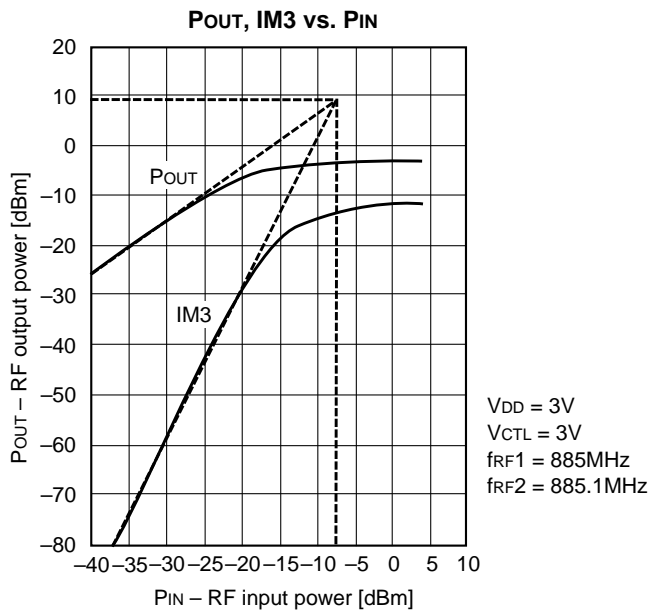
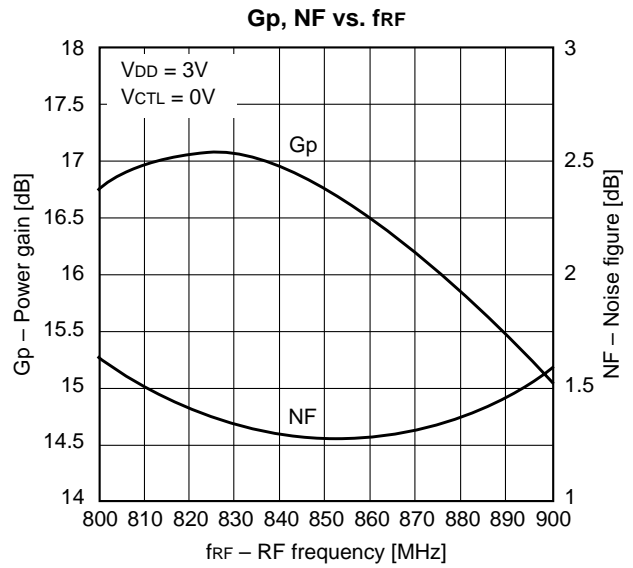
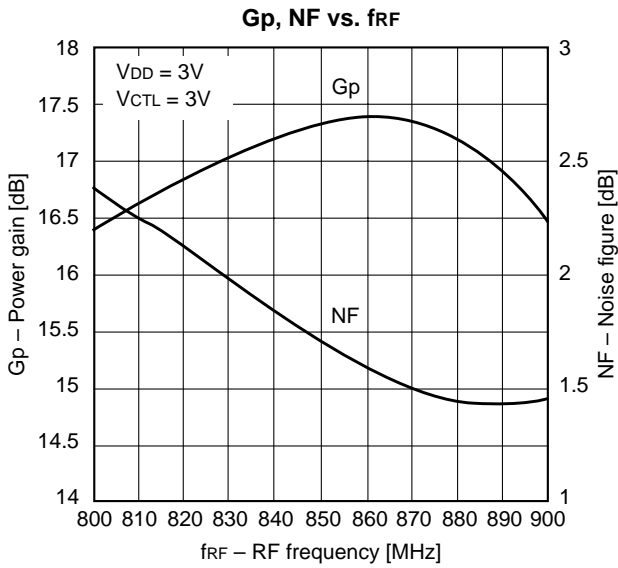
Recommended Evaluation Circuit



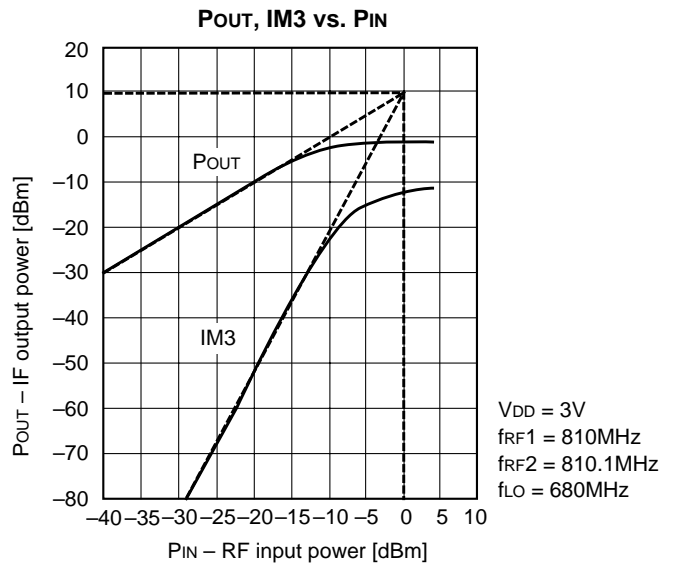
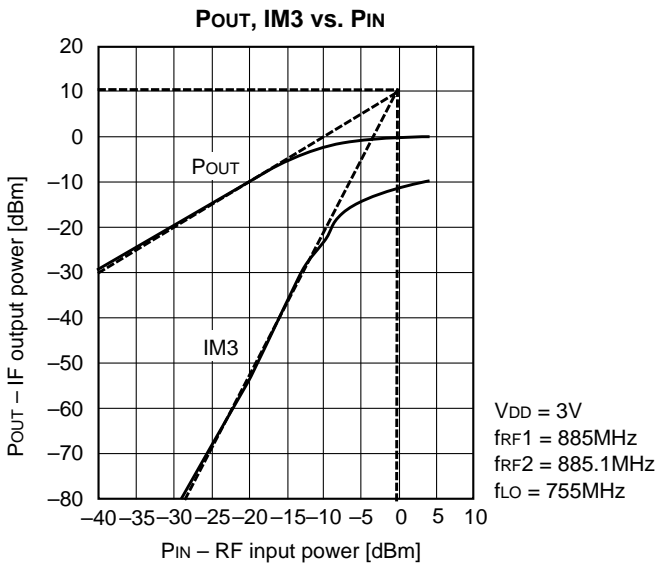
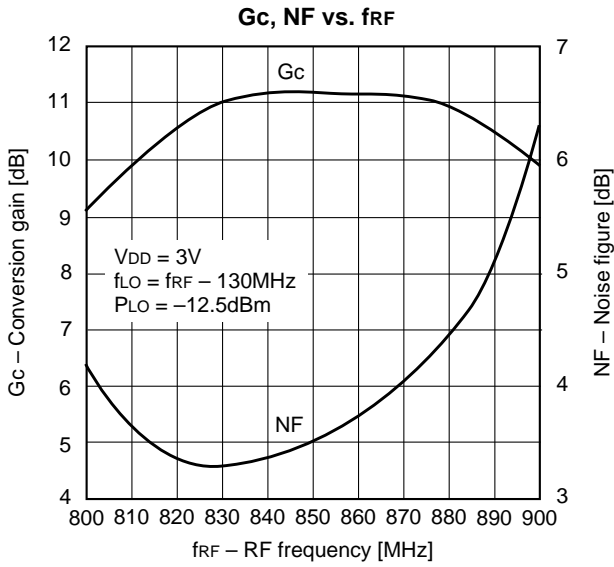
L1	220nH	L11	18nH	C6	18pF
L2	220nH	L12	12nH	C7	1000pF
L3	33nH	L13	22nH	C8	100pF
L4	18nH	L14	5.6nH	C9	47pF
L5	6.8nH	L15	27nH	C10	1000pF
L6	27nH	C1	5pF	R1	680Ω
L7	39nH	C2	1000pF		
L8	22nH	C3	1000pF		
L9	1.2nH	C4	100pF		
L10	8.2nH	C5	1000pF		

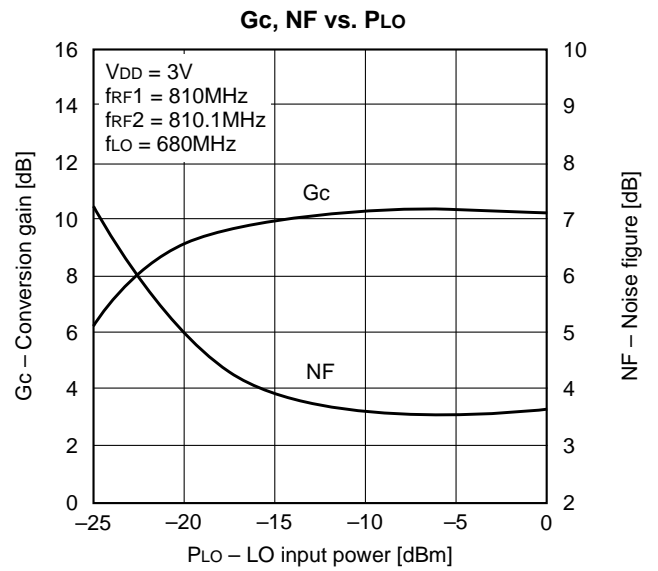
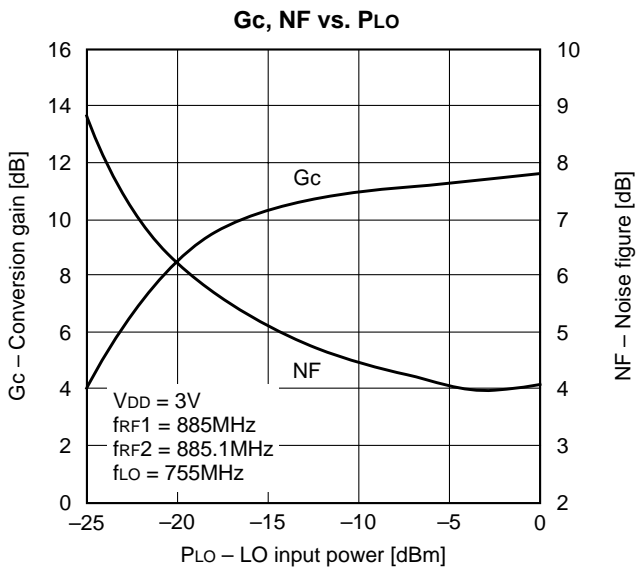
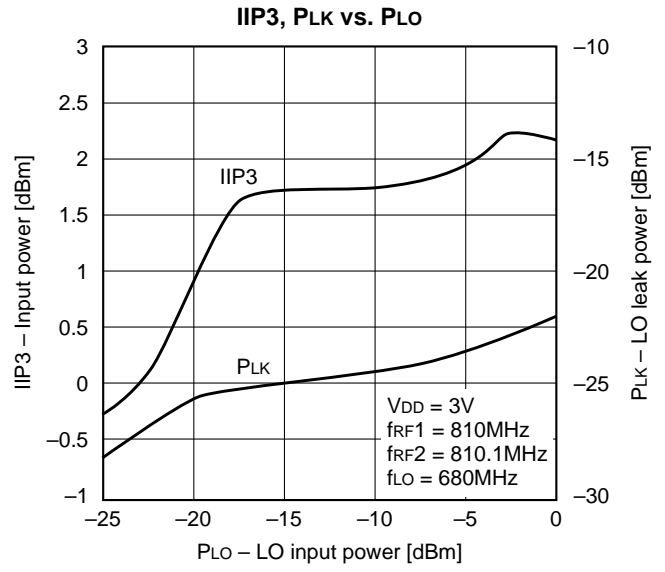
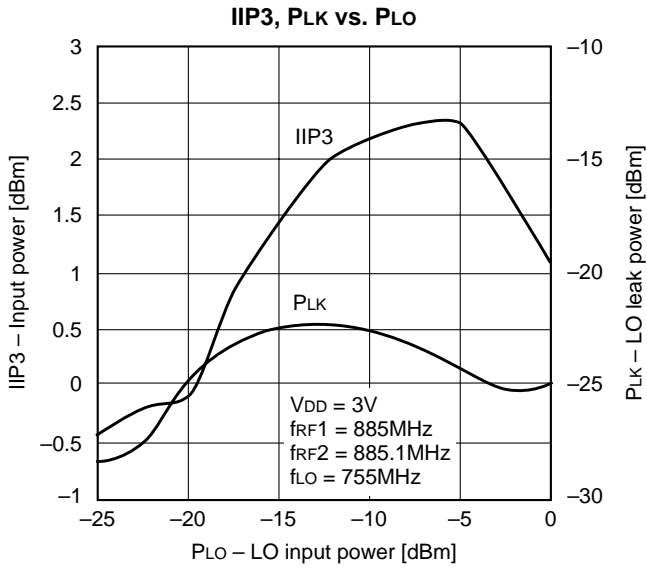
Example of Representative Characteristics (Ta = 25°C)

Low Noise Amplifier Block

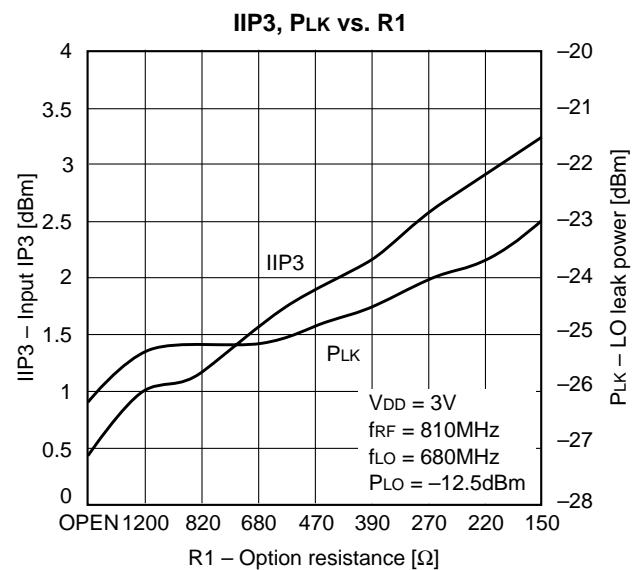
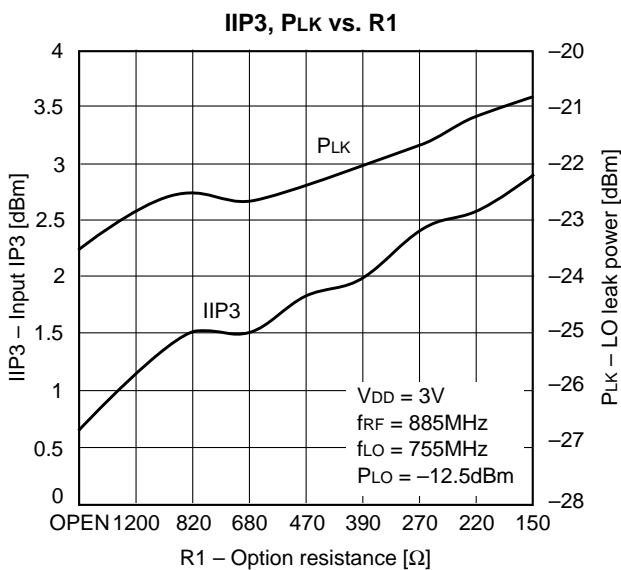
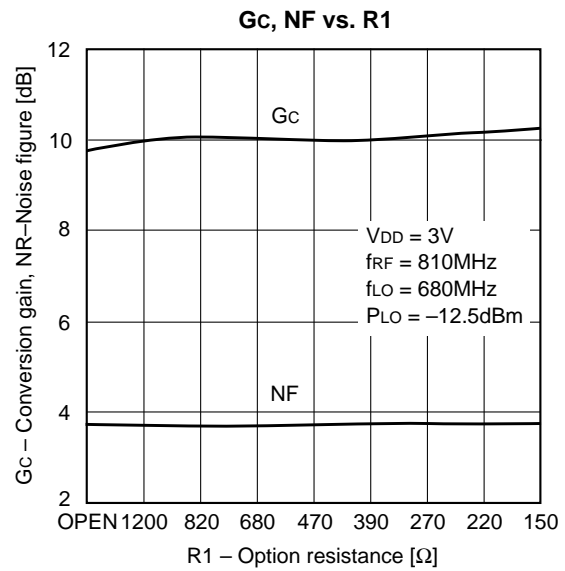
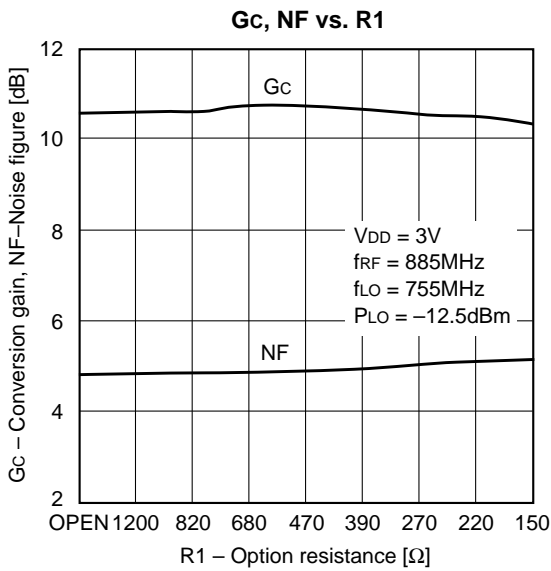
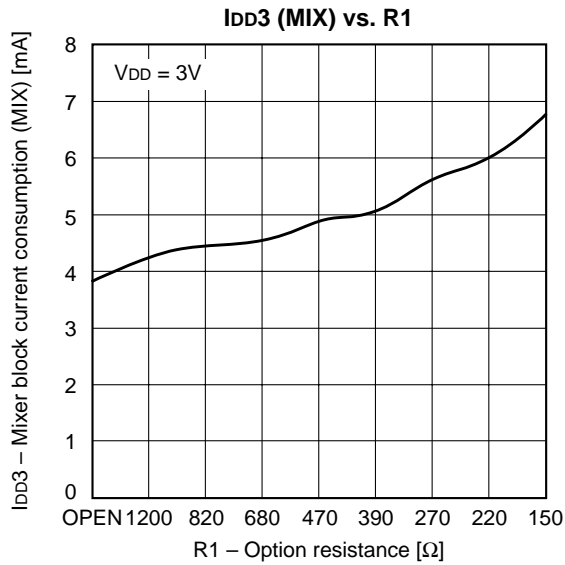


Mixer Block

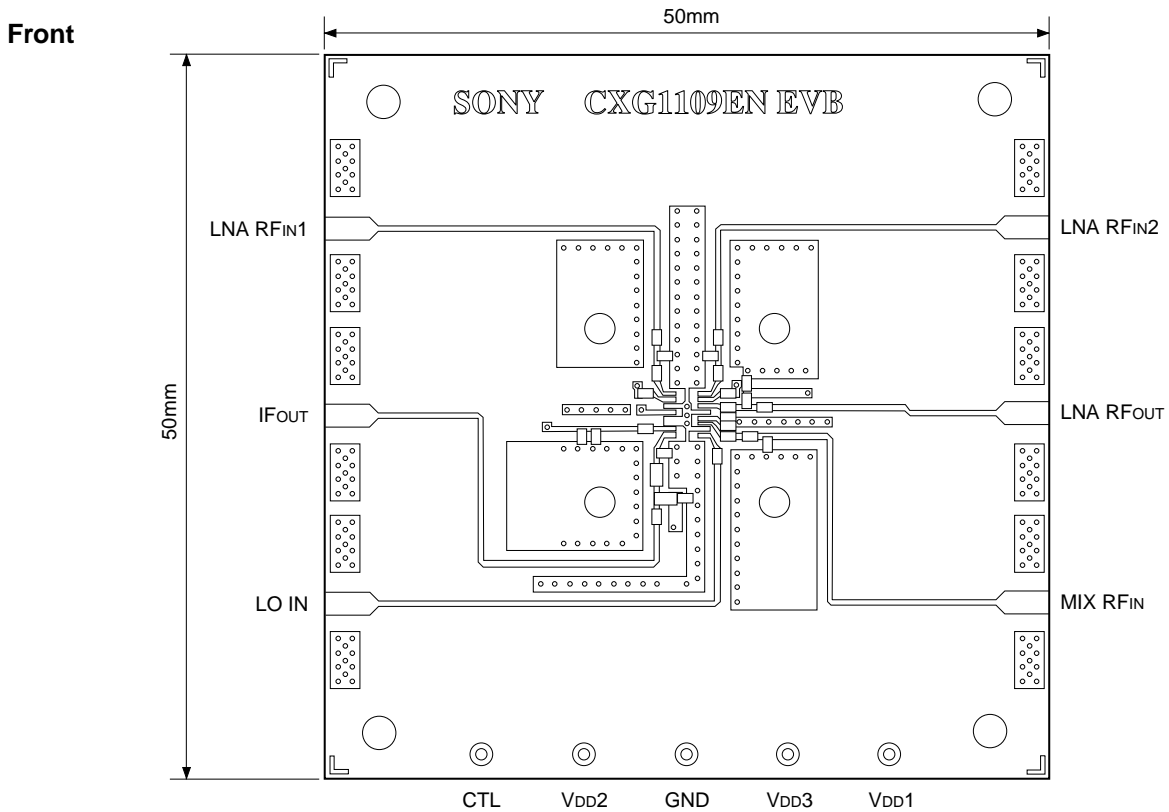




Example of Characteristics for Option Resistance R1 Changed (Ta = 25°C)

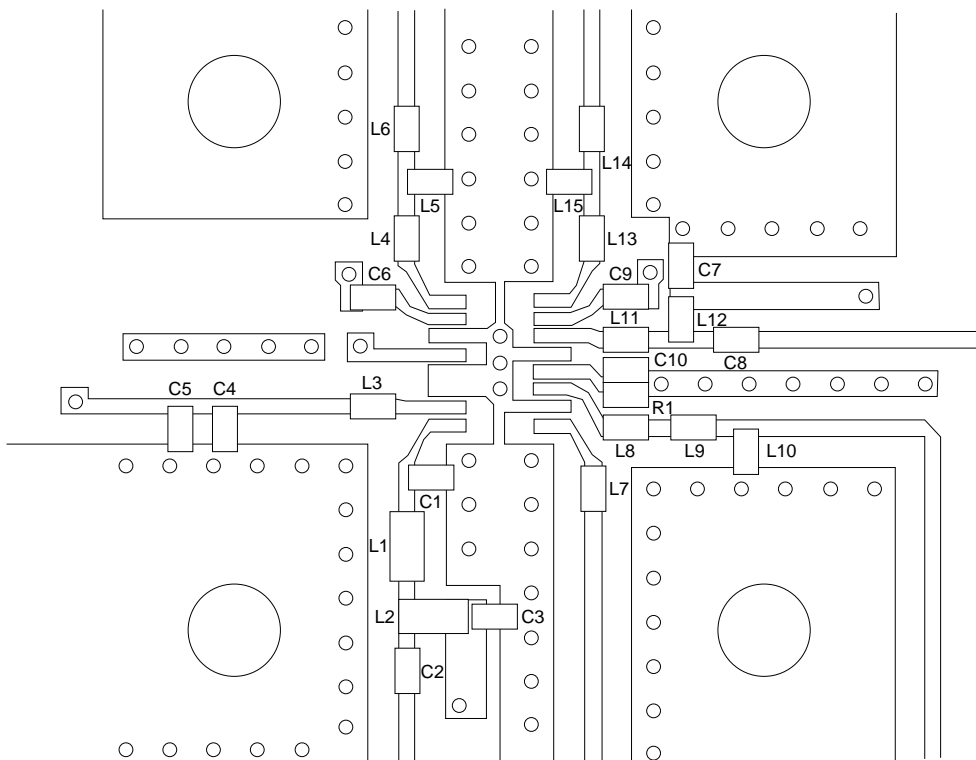


Recommended Evaluation Board



Glass fabric-base 4-layer epoxy board (thickness: 0.2mm × 2)
GND for the whole 2nd and 3rd layers

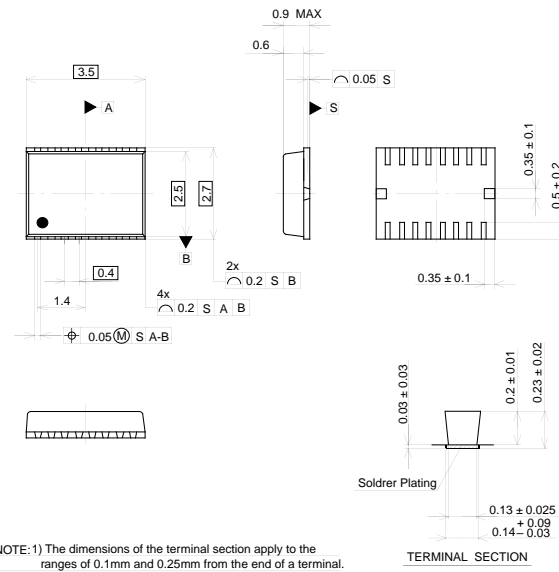
Enlarged Diagram of Center Part



Package Outline

Unit: mm

16PIN VSON (PLASTIC)



NOTE: 1) The dimensions of the terminal section apply to the ranges of 0.1mm and 0.25mm from the end of a terminal.

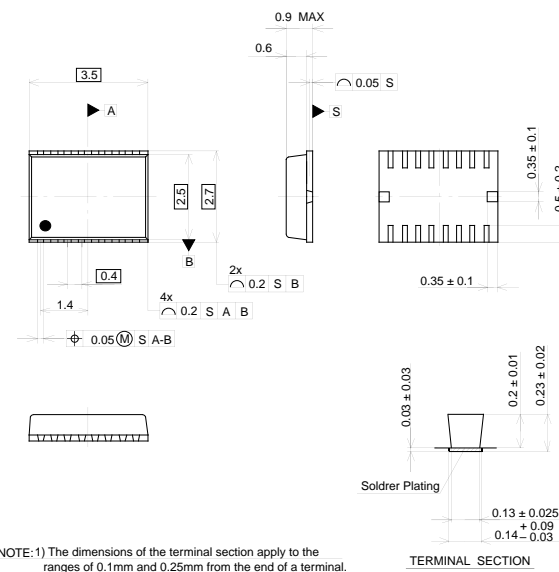
PACKAGE STRUCTURE

SONY CODE	VSON-16P-01
EIAJ CODE	
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.02 g

Kokubu Ass'y

16PIN VSON (PLASTIC)



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LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm