

TRIACS

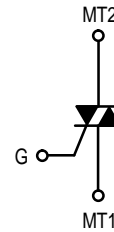
Silicon Bidirectional Thyristors

Designed for high volume, low cost, industrial and consumer applications such as motor control; process control; temperature, light and speed control.

- Small Size Surface Mount DPAK Package
- Passivated Die for Reliability and Uniformity
- Blocking Voltage to 800 V
- On-State Current Rating of 4.0 Amperes RMS at 108°C
- Low IGT — 10 mA Maximum in 3 Quadrants
- High Immunity to dv/dt — 50 V/μs at 125°C

ORDERING INFORMATION

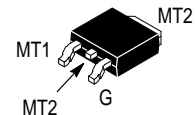
- To Obtain "DPAK" in Surface Mount Leadform (Case 369A)
Shipped in 16 mm Tape and Reel — Add "T4" Suffix to Device Number, i.e. MAC4DSNT4
- To Obtain "DPAK" in Straight Lead Version (Case 369) Shipped in Sleeves — Add "-1" Suffix to Device Number, i.e. MAC4DSN-1



MAC4DSM
MAC4DSN

Motorola Preferred Devices

TRIACS
4.0 AMPERES RMS
600 thru 800 VOLTS



CASE 369A-13
STYLE 6

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage ⁽¹⁾ (T _J = -40 to 125°C, Sine Wave, 50 to 60 Hz, Gate Open)	V _{DRM}	600 800	Volts
On-State RMS Current (Full Cycle Sine Wave, 60 Hz, T _C = 108°C)	I _{T(RMS)}	4.0	Amps
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz, T _J = 125°C)	I _{TSM}	40	
Circuit Fusing Consideration (t = 8.3 msec)	I ² t	6.6	A ² sec
Peak Gate Power (Pulse Width ≤ 10 μsec, T _C = 108°C)	P _{GM}	0.5	Watts
Average Gate Power (t = 8.3 msec, T _C = 108°C)	P _{G(AV)}	0.1	
Peak Gate Current (Pulse Width ≤ 10 μsec, T _C = 108°C)	I _{GM}	0.2	Amps
Peak Gate Voltage (Pulse Width ≤ 10 μsec, T _C = 108°C)	V _{GM}	5.0	Volts
Operating Junction Temperature Range	T _J	-40 to 125	°C
Storage Temperature Range	T _{stg}	-40 to 150	

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance — Junction to Case	R _{θJC}	3.5	°C/W
— Junction to Ambient	R _{θJA}	88	
— Junction to Ambient ⁽²⁾	R _{θJA}	80	
Maximum Lead Temperature for Soldering Purposes ⁽³⁾	T _L	260	°C

(1) V_{DRM} for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the device are exceeded.

(2) Surface mounted on minimum recommended pad size.

(3) 1/8" from case for 10 seconds.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

MAC4DSM MAC4DSN

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
Peak Repetitive Blocking Current (V _D = Rated V _{DRM} , Gate Open) T _J = 25°C T _J = 125°C	I _{DRM}	— —	— —	0.01 2.0	mA
Peak On-State Voltage (1) (I _{TM} = ±6.0 A)	V _{TM}	—	1.3	1.6	Volts
Gate Trigger Current (Continuous dc) (V _D = 12 V, R _L = 100 Ω) MT2(+), G(+) MT2(+), G(-) MT2(-), G(-)	I _{GT}	2.9 2.9 2.9	4.0 5.0 7.0	10 10 10	mA
Gate Trigger Voltage (Continuous dc) (V _D = 12 V, R _L = 100 Ω) MT2(+), G(+) MT2(+), G(-) MT2(-), G(-) MT2(+), G(+); MT2(+), G(-); MT2(-), G(-) T _J = 125°C	V _{GT}	0.5 0.5 0.5 0.2	0.7 0.65 0.7 0.4	1.3 1.3 1.3 —	Volts
Holding Current (V _D = 12 V, Gate Open, I _T = ±200 mA)	I _H	2.0	5.5	15	mA
Latching Current (V _D = 12 V, I _G = 10 mA) MT2(+), G(+) MT2(+), G(-) MT2(-), G(-)	I _L	— — —	6.0 10 6.0	30 30 30	mA

DYNAMIC CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Rate of Change of Commutating Current (1) (V _D = 400 V, I _{TM} = 3.5 A, Commutating dv/dt = 10 V/μsec, Gate Open, T _J = 125°C, f = 500 Hz, CL = 5.0 μF, LL = 20 mH, No Snubber) See Figure 15	di/dt(c)	3.0	4.0	—	A/ms
Critical Rate of Rise of Off-State Voltage (V _D = 0.67 X Rated V _{DRM} , Exponential Waveform, Gate Open, T _J = 125°C)	dv/dt	50	175	—	V/μs

(1) Pulse test: Pulse Width ≤ 2.0 msec, Duty Cycle ≤ 2%.

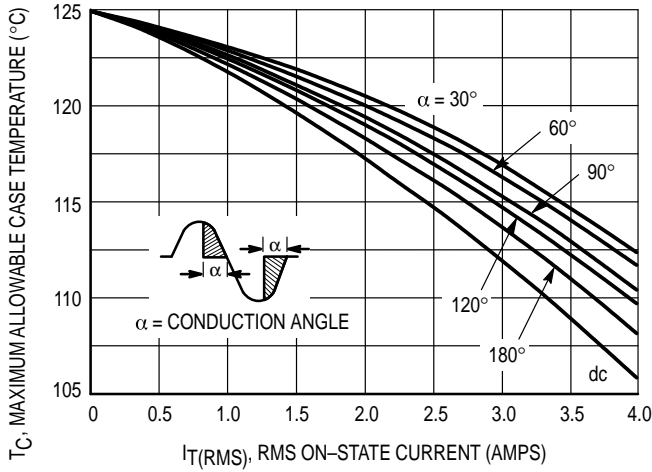


Figure 1. RMS Current Derating

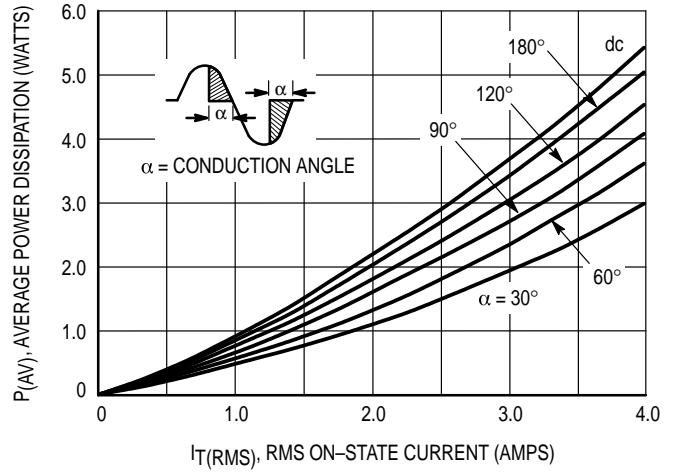


Figure 2. On-State Power Dissipation

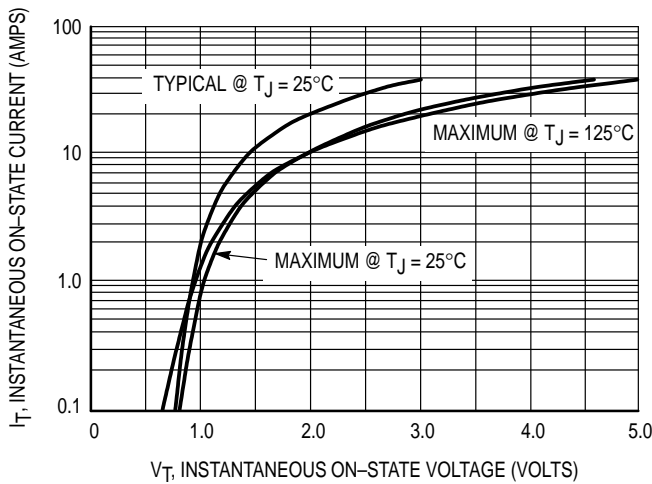


Figure 3. On-State Characteristics

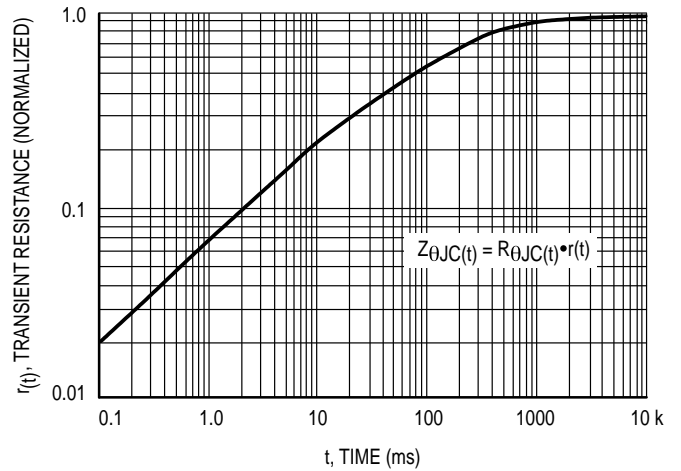


Figure 4. Transient Thermal Response

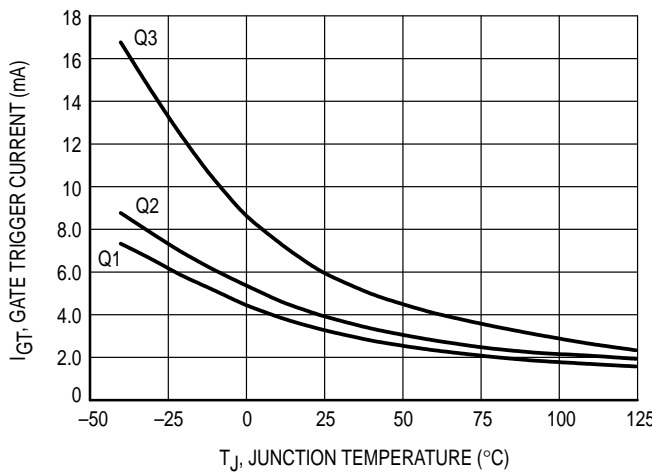


Figure 5. Typical Gate Trigger Current versus Junction Temperature

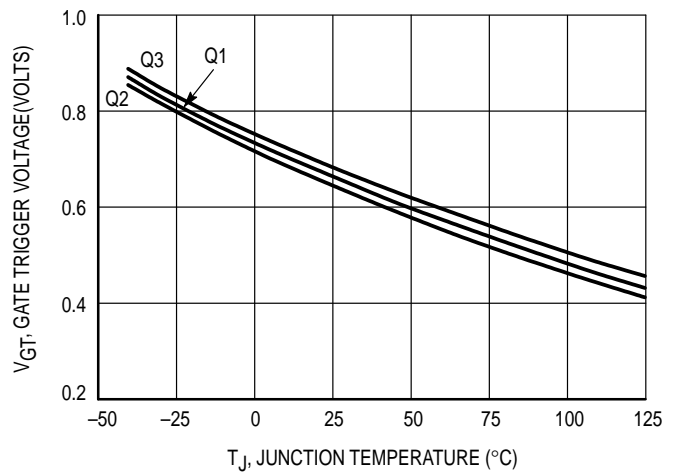


Figure 6. Typical Gate Trigger Voltage versus Junction Temperature

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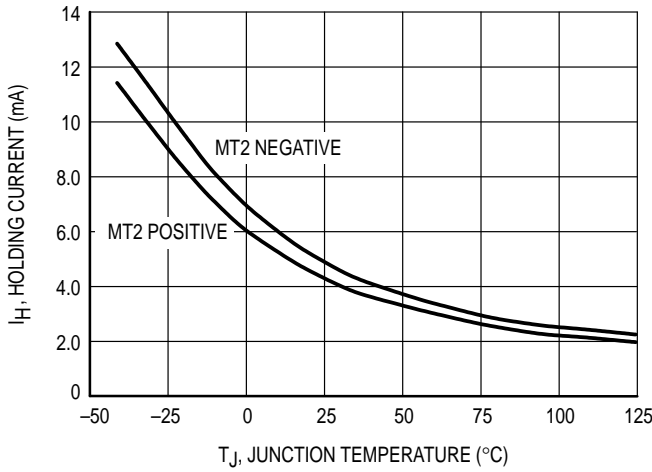


Figure 7. Typical Holding Current versus Junction Temperature

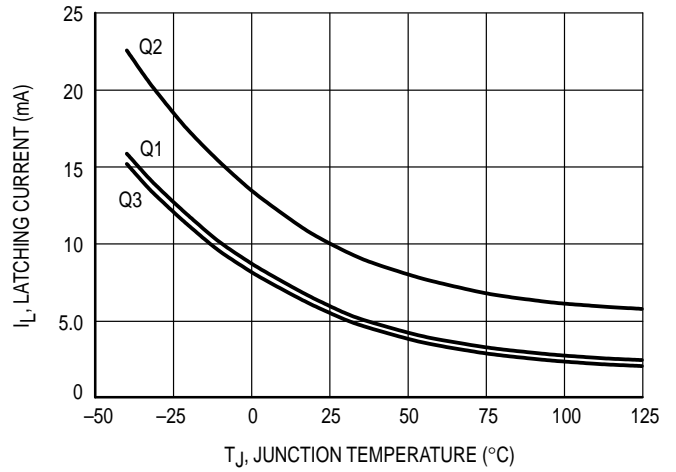


Figure 8. Typical Latching Current versus Junction Temperature

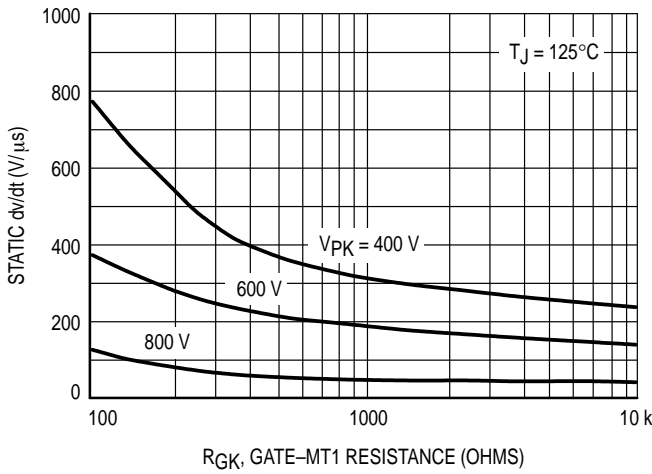


Figure 9. Exponential Static dv/dt versus Gate-MT1 Resistance, MT2(+)

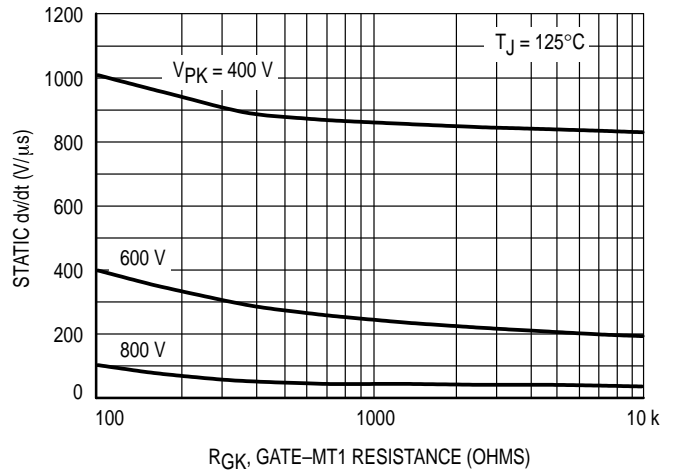


Figure 10. Exponential Static dv/dt versus Gate-MT1 Resistance, MT2(-)

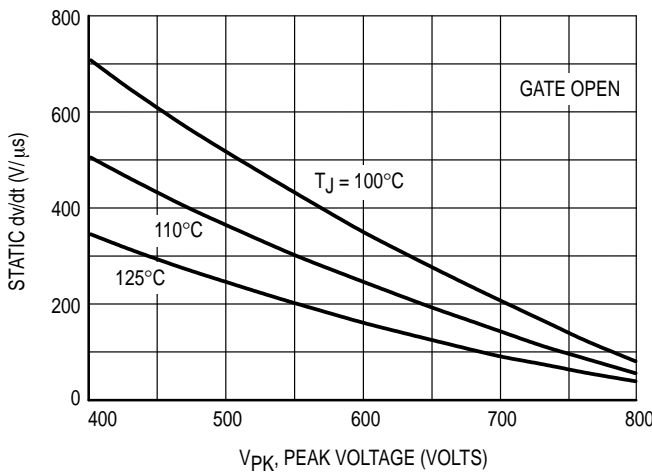


Figure 11. Exponential Static dv/dt versus Peak Voltage, MT2(+)

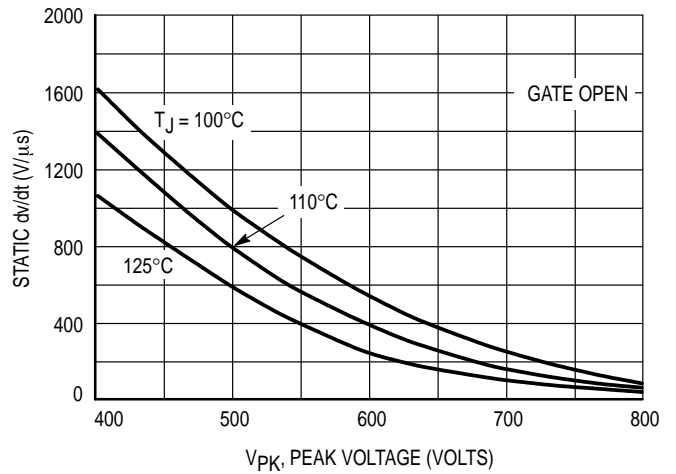


Figure 12. Exponential Static dv/dt versus Peak Voltage, MT2(-)

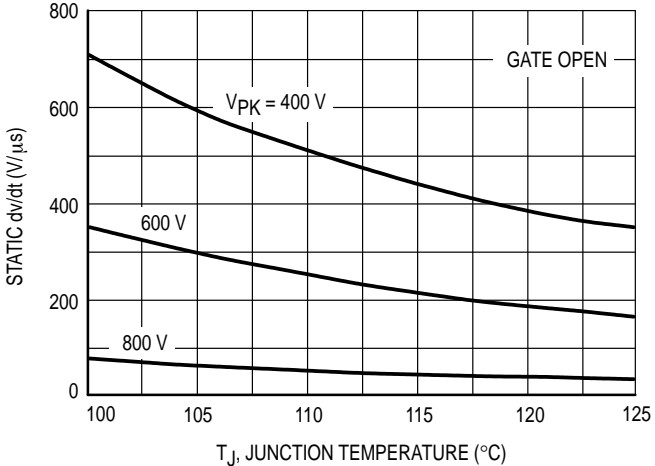


Figure 13. Typical Exponential Static dv/dt versus Junction Temperature, MT2(+)

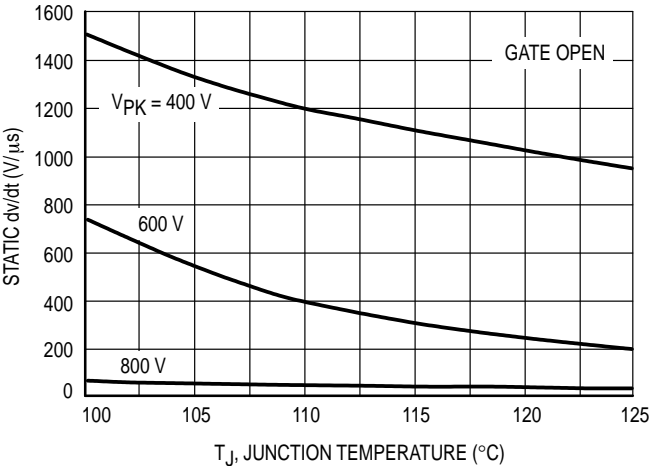


Figure 14. Typical Exponential Static dv/dt versus Junction Temperature, MT2(-)

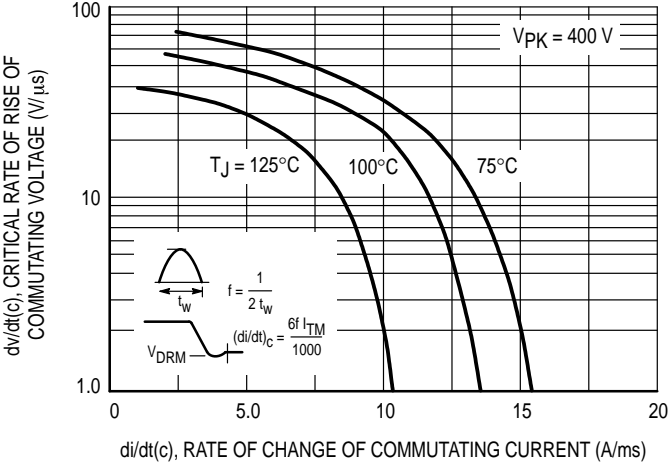


Figure 15. Critical Rate of Rise of Commutating Voltage

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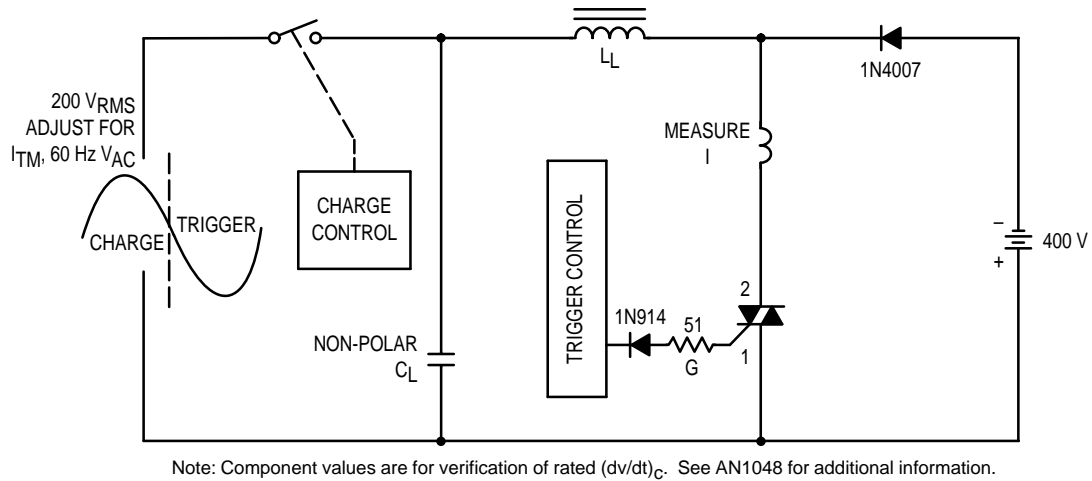
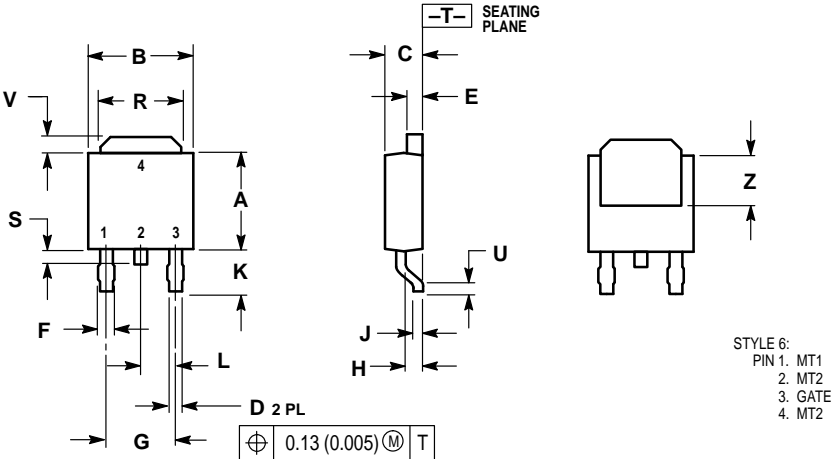


Figure 16. Simplified Test Circuit to Measure the Critical Rate of Rise of Commutating Voltage

PACKAGE DIMENSIONS




- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.175	0.215	4.45	5.46
S	0.020	0.050	0.51	1.27
U	0.020	—	0.51	—
V	0.030	0.050	0.77	1.27
Z	0.138	—	3.51	—

CASE 369A-13
 ISSUE Z

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