PM5346

S/UNI-™ 155-LITE

INTERFACING AND PC BOARD LAYOUT SUGGESTIONS FOR THE S/UNI-LITE

APPLICATION NOTE

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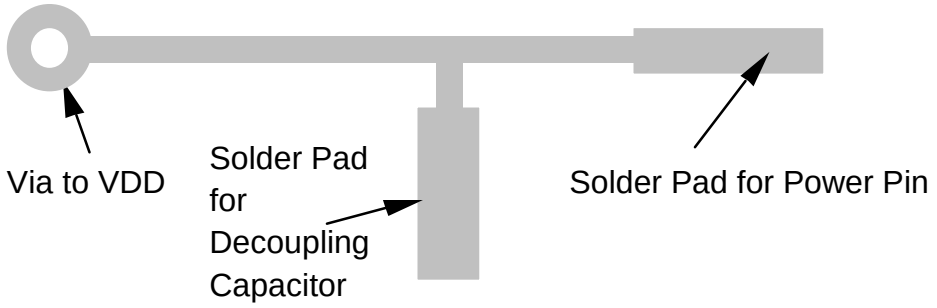
1 SUGGESTIONS FOR S/UNI-LITE BOARD LAYOUT

1.1 Decoupling Capacitors on Analog Power

Decoupling capacitors (0.1 µF Ceramic X7R) are recommended for each analog power pin (TAVD1, TAVD2, TAVD3, TXVDD, RAVD1, RAVD2, RAVD3, RAVD4) placed as close to the package pin as possible according to the layout recommendation in figure 1 below. In particular, separate decoupling capacitors are strongly recommended for the TAVD1, TAVD2, RAVD1 and RAVD2 pins.

Separate decoupling is recommended to prevent transmit from coupling transient noise into the receiver. TAVD1 and RAVD1 are power supplies for voltage reference circuitry for the transmit and receive PLLs respectively. There must be separate decoupling of TAVD2 from TAVD1; RAVD2 must be separately de-coupled from RAVD1. This prohibits transients from coupling into the references (i.e., RAVD1 and TAVD1).

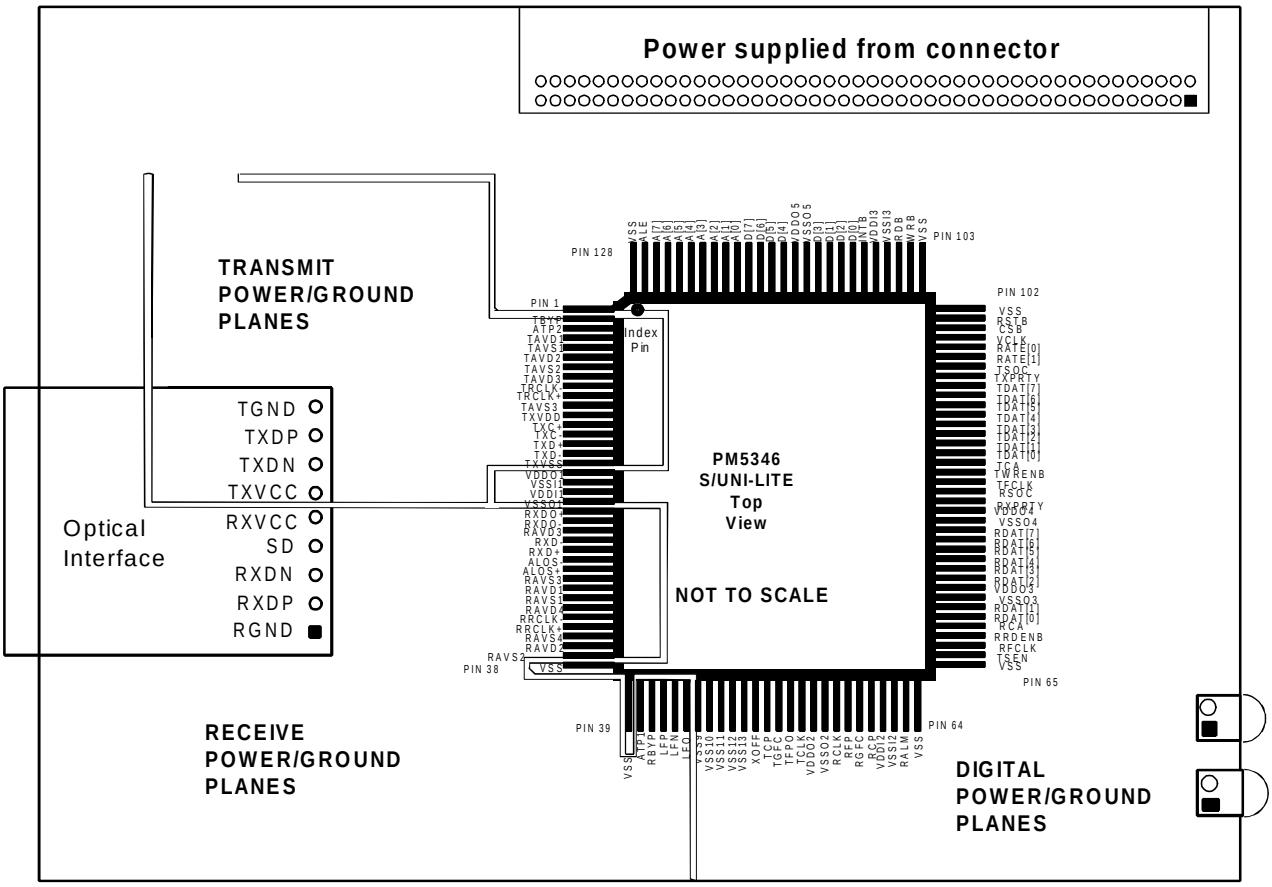
Figure 1 - Recommended Layout for VDD Decoupling Connection to Analog Power Pins



1.2 Power and Ground Connections

It is advisable to separate the S/UNI-LITE transmit power/ground pins from the receive power/ground pins by splitting the power and ground planes in the area surrounding these pins as shown in figure 2.

Figure 2 -



Power and Ground requirements are a function of the noise environment on a board and the performance target of the board. Ground and power supply noise will degrade the bit error performance of the S/UNI-LITE and introduce intrinsic jitter on the transmitted data. Table 1 is a summary of all power and ground connections for the S/UNI-LITE. The “Supply Noise Sensitivity” column highlights pins that are sensitive to perturbations on the supply rails. The “Current” column identifies the current consumption for a particular pin as either dynamic (fluctuating over time) or static (constant over time). The “Layout Consideration” column provides further detail regarding the layout requirements for each pin.

Table 1 - S/UNI-LITE Power/Ground Pins

Pin Name	Type	Supply Noise Sensitivity	Current	Pin No.	Layout Consideration
RAVS1	Ground	High	Static	31	The ground (RAVS1) pin for analog voltage reference circuitry
RAVS2	Ground	High	Dynamic	37	The ground (RAVS2) pin for receive loop filter and VCO.
RAVS3	Ground	High	Dynamic	29	The ground (RAVS3) pin for the RXD+/- & ALOS+/- PECL inputs.
RAVS4	Ground	High	Dynamic	35	The ground (RAVS4) pin for the RRCLK+/- PECL inputs.
TAVS1	Ground	High	Static	5	The ground (TAVS1) pin for analog voltage reference circuitry
TAVS2	Ground	High	Dynamic	7	The ground (TAVS2) pin for the transmit clock synthesizer VCO.
TAVS3	Ground	High	Dynamic	11	The ground (TAVS3) pin for the transmit PECL inputs.

Pin Name	Type	Supply Noise Sensitivity	Current	Pin No.	Layout Consideration
TXVSS	Ground	High	Dynamic	17	The transmit pad ground (TXVSS) is the return path for the TXC+/- and TXD+/- outputs. TXVSS is physically isolated from the other device ground pins and should be noise free for good performance.
VSSI1H VSSI2 VSSI3	Ground	Low	Dynamic	19 62 106	The core ground (VSSI1 - VSSI3) pins should be connected to GND in common with VSSO.
VSSO1 VSSO2 VSSO3 VSSO4 VSSO5	Ground	Low	Dynamic	21 56 72 80 113	The pad ring ground (VSSO1 - VSSO5) pins should be connected to GND in common with VSSI.
VSS1, VSS2, VSS3, VSS4, VSS5, VSS6, VSS7, VSS8, VSS9, VSS10, VSS11, VSS12, VSS13	Thermal Ground	Low	Dynamic	1 38 39 64 65 102 103 128, 45, 46, 47, 48, 49	The thermal grounds (VSS1 - VSS13) provide a low thermal resistance for the dissipated heat. These pins must be connected to DIGITAL GND only for correct operation. Note: these pins are electrically connected together internally

Pin Name	Type	Supply Noise Sensitivity	Current	Pin No.	Layout Consideration
RAVD1	Power	High	Static	30	The power (RAVD1) pin for analog voltage reference circuitry.
RAVD2	Power	High	Dynamic	36	The power (RAVD2) pin for receive loop filter and VCO.
RAVD3	Power	High	Dynamic	24	The power (RAVD3) pin for the RXD+/- and ALOS+/- PECL inputs.
RAVD4	Power	High	Dynamic	32	The power (RAVD4) pin for the RRCLK+/- PECL inputs.
TAVD1	Power	High	Static	4	The power (TAVD1) pin for analog voltage reference circuitry.
TAVD2	Power	High	Dynamic	6	The power (TAVD2) pin for the transmit clock synthesizer VCO.
TAVD3	Power	High	Dynamic	8	The power (TAVD3) pin for the transmit PECL inputs.

Pin Name	Type	Supply Noise Sensitivity	Current	Pin No.	Layout Consideration
TXVDD	Power	High	Dynamic	12	The transmit pad power (TXVDD) supplies the TXC+/- and TXD+/- outputs. TXVDD is physically isolated from the other device power pins and should be a well regulated +5 V DC and noise free for good performance.
VDDI1 VDDI2 VDDI3	Power	Low	Dynamic	20 61 107	The core power (VDDI1 - VDDI3) pins should be connected to a well decoupled +5 V DC in common with VDDO.
VDDO1 VDDO2 VDDO3 VDDO4 VDDO5	Power	Low	Dynamic	18 55 73 81 114	The pad ring power (VDDO1 - VDDO5) pins should be connected to a well decoupled +5 V DC in common with VDDI.

1.3 Ferrite Beads on Digital Power Supply

Power supply isolation using Ferrite beads is not advisable in digital switching circuits as di/dt noise is introduced into the power rail. Sufficient capacitive decoupling on all digital power pins is recommended.

1.4 Ferrite Beads on Analog Power Supply

Ferrite beads for power supply isolation can be used in analog (and ECL) circuitry where there is no di/dt noise due to single ended switching currents. If this not the case, or it is uncertain that the circuitry is operating in a balanced fashion, then using RC filtering or local bulk decoupling to filter local di/dt noise is recommended.

1.5 Regulating the Analog Power Supply (Optional)

In applications that provide a +12V supply, a 5V regulator can be used to supply a low-noise analog power supply. The regulator should supply all analog power pins (TAVD1-4 and RAVD1-4); the total power draw of the analog circuitry in the S/UNI-LITE is less than 30mW. At a minimum, the regulator should power RAVD1, RAVD2, TAVD1, and TAVD2.

1.6 Analog Test Pins

The Analog test pins must be grounded. ATP1 should be connected to the Receive analog ground plane. ATP2 should be connected to the Transmit analog ground plane.

1.7 Loop Filter Components

The loop filter components should be placed such that they sit over the Receive analog ground plane.

1.8 Unused Input Pins

All unused input pins should be tied to their appropriate inactive level.

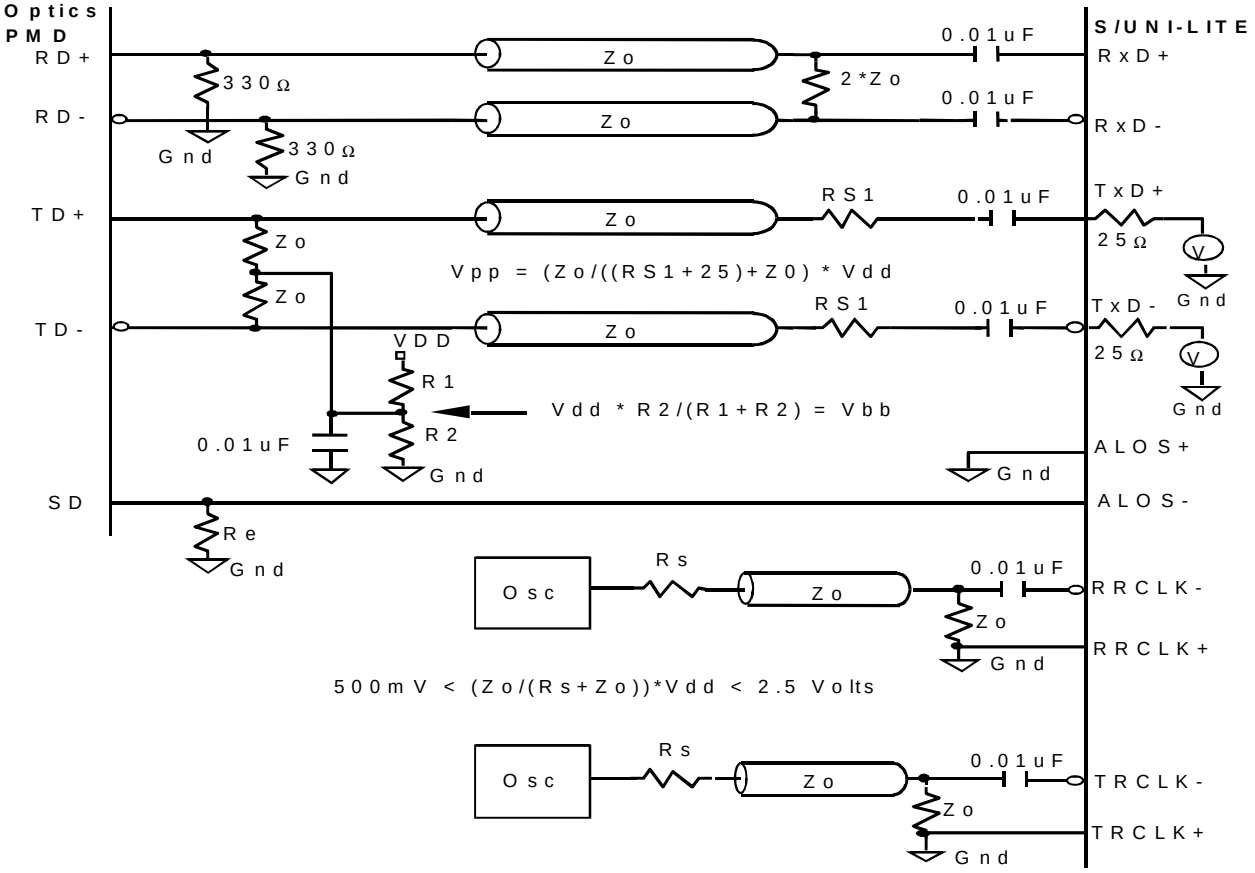
1.9 Dealing with high-speed return currents

At low speeds, return current follows the path of least resistance back to the driver. At high speeds, however, the return current follows the path of least inductance which lies on the plane directly under the signal trace, as the total loop area between the outgoing and returning paths is minimized. In other words, the high-speed return current follows a path that is almost the "mirror image" of the signal trace on the plane underneath the trace. This tight coupling provides good flux cancellation so that common-mode current is reduced. High speed traces should not cross cuts or heavily perforated areas (where tight spacing through-hole components reside) on the power and ground planes, as

any cuts on these planes may interrupt the return currents, causing them to seek alternative paths back to the driver. The different routes taken by the outgoing and return currents will both induce common-mode noise on other nearby signal traces. In addition, by routing high speed signals over continuous power planes, the return current paths of these signals are known and other signals will not cross over these return currents, reducing the possibility of noise coupling. Detailed discussions on high-speed design are provided by the references.

2 SUGGESTIONS FOR S/UNI-LITE PECL TERMINATIONS

Figure 3 - S/UNI-LITE to PMD and Reference Oscillator Terminations



Notes for Figure 3:

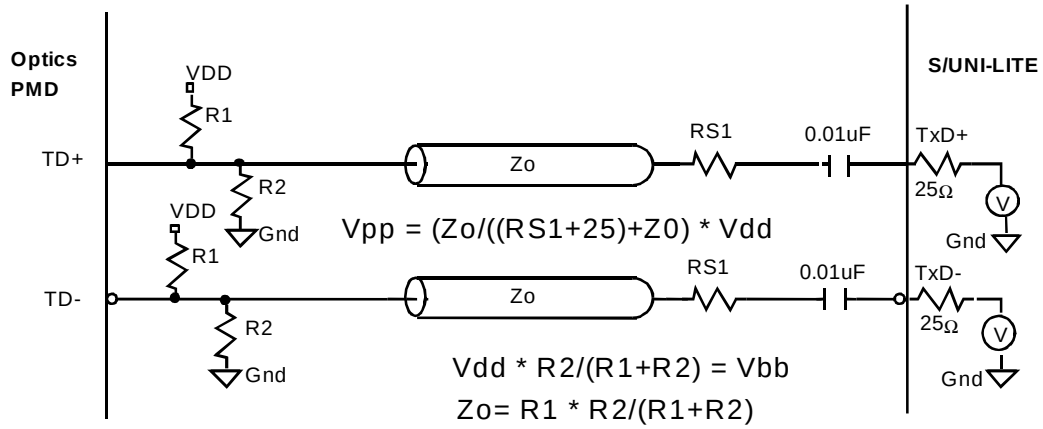
- Vpp is minimum input swing required by the optical PMD device.
- Vbb is the switching threshold of the PMD device (typically Vdd – 1.3 Volts).
- Vpp is Voh – Vol (typically 800 mVolts).
- The value of Re is dependent on the signal trace characteristic impedance and the ECL or PECL supply voltage (-4.5 V, +5 V).
- Values in the range of 200-300 Ω are recommended.

- A single oscillator can be used to drive both RRCLK and TRCLK.

2.1 S/UNI-LITE TxD to PMD

The TxD outputs from the S/UNI-LITE may also use Thévenin termination resistors that provide the Vbb bias voltage rather than the resistor-divider shown above. While this circuit uses one less component (0.01 µF decoupling capacitor), it is more susceptible to common mode noise.

Figure 4 -



Notes: Vpp is minimum input swing required by the optical PMD device.
Vbb is the switching threshold of the PMD device (typically Vdd - 1.3 volts)
Vpp is Voh - Vol (typically 800 mVolts)
For Zo = 50 Ω, R1=67 Ω, R2 = 192.3 Ω, RS1=237Ω

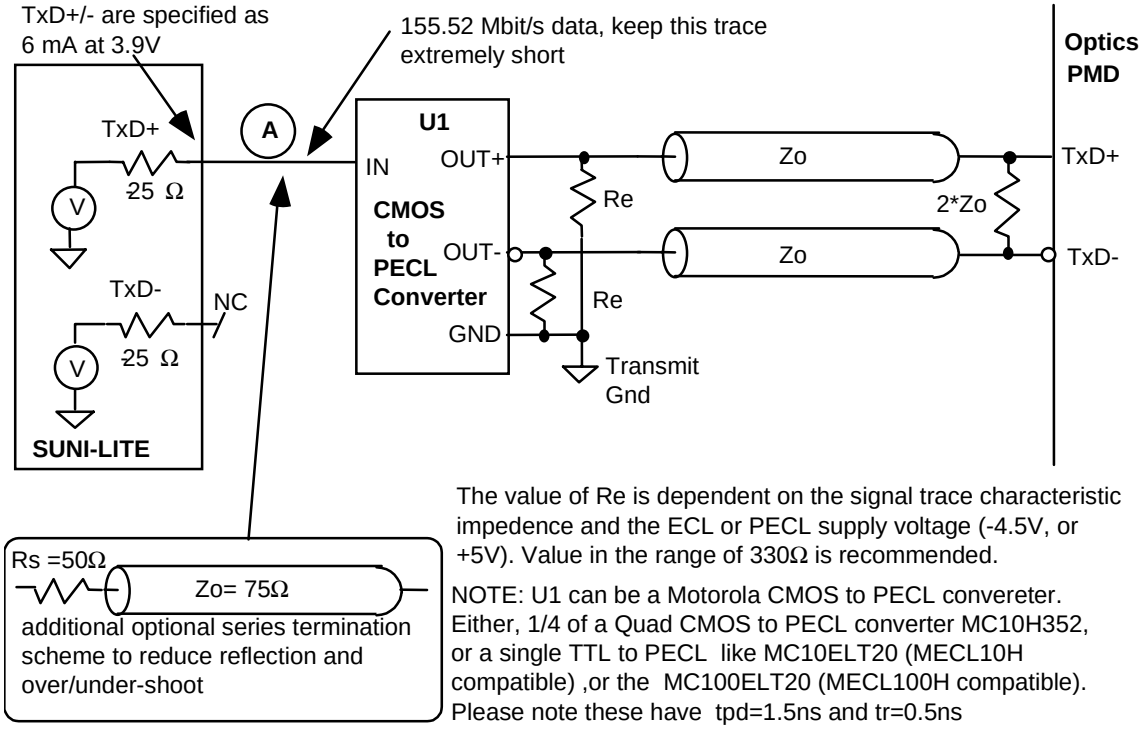
2.2 DC coupled TxD+ via CMOS to PECL converter

Schemes (1) and (2) above use AC-coupling capacitors on the TXD+/- S/UNI-LITE outputs. A disadvantage of this scheme is that Diagnostic LOS (DLOS register bit) can no longer be used because the AC-coupled all zero transmit data will cause the PMD inputs to float to the Vbb threshold. This can result in the PMD transmitting pulses due to board noise. A way to eliminate this is to use a CMOS to PECL converter, between the S/UNI-LITE TXD+/- outputs and the ODL. Due to the high data rate, and this single ended CMOS I/F, make sure the converter is located right at the S/UNI-LITE TXD output.

Care must be taken to maintain signal integrity for low jitter. Connection 'A' below, must be an extremely short signal trace (less than 1") with no termination. Optionally, for slightly longer trace, a series termination and a controlled

transmission trace is required. The length limit of such a terminated CMOS trace depends on factors such as system ground noise, Zo and Rs. The value of Rs depends on the SUNI-LITE source driver impedance (about 25Ω) and the Zo of the controlled signal PCB trace (Zo=25Ω+Rs).

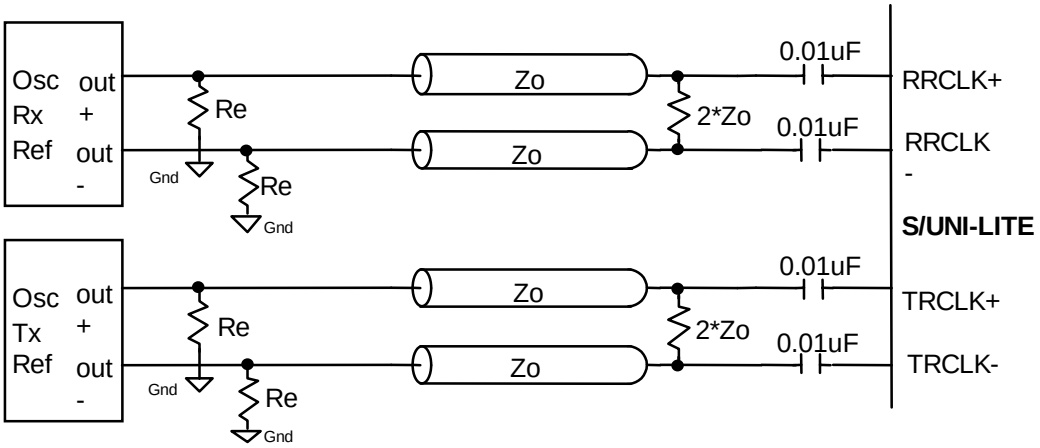
Figure 5 - CMOS to PECL Converter



2.3 Differential Reference Oscillator Terminations

For optimum jitter performance on the transmit side and noise immunity on the receive side the reference clocks should be connected differentially.

Figure 6 - Reference Oscillator Terminations



The value of Re is dependent on the signal trace characteristic impedence and the ECL or PECL supply voltage (-4.5 V, + 5 V). Values in the range of 200-330 Ω are recommended

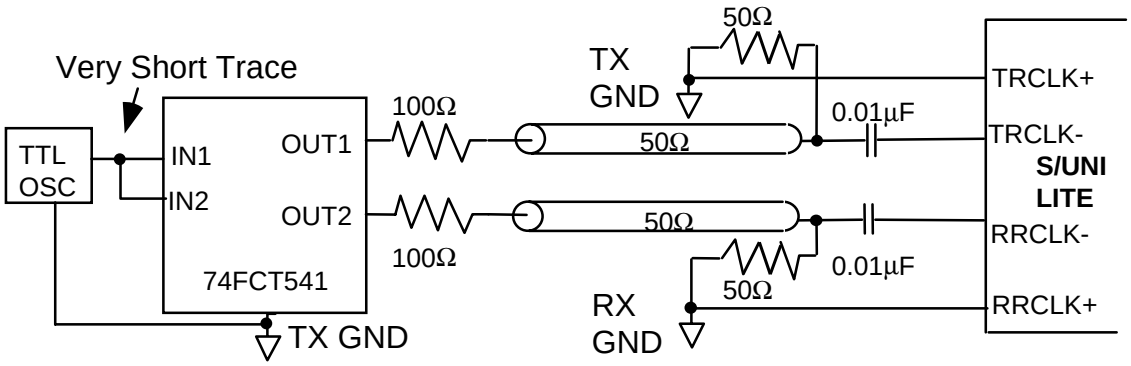
2.4 Single TTL/CMOS Reference Oscillator Driving Both RRCLK and TRCLK

If a single TTL or CMOS oscillator is used to drive these inputs, the RRCLK- and TRCLK- inputs can be used while RRCLK+ and TRCLK+ signals are connected to their respective grounds. The single clock signal must be properly terminated, however, it is not a good idea to connect the clock trace to either RRCLK- or TRCLK- and then run the trace to the other input and terminate at the far end. The transmit and receive grounds are isolated by channels cut into the ground plane, so potential differences between transmit and receive grounds will affect one of the reference clock inputs. For example, if the reference clock signal is run to the TRCLK input and then is terminated to the receive ground near the RRCLK input, the TRCLK input (which is referenced to the transmit ground) will require the clock swing to be large enough to accommodate the difference between grounds. Otherwise, the TRCLK input will be more sensitive to noise than the RRCLK input. A second problem may arise if the clock signal trace crosses the cuts in the ground plane (i.e. from transmit ground island to receive ground island). In that case the ground return current from the receive side cannot follow the signal trace back to the driver. Instead, it will seek an

alternative path of least inductance. Consequently, this ground current will induce common-mode noise on signals nearby.

The solution is to run two separate reference clock signals and terminate them at each input[1]. The following diagram illustrates how to use a single TTL level oscillator to drive the RRCLK- & TRCLK- signals via a 74FCT541 buffer. The TRCLK+ and RRCLK+ signals are connected to their respective grounds.

Figure 7 -



The TTL oscillator should be placed as close to the buffer as possible as it is unterminated. The TTL oscillator is used to match the 74FCT541's TTL input level in order to avoid duty cycle distortion caused by differences in output levels and input switching thresholds.

[1] A layout alternative could be to run a 50 ohm clock trace to the vicinity of the RRCLK- & TRCLK- inputs and then split into two 100 ohm traces. Each one of these two traces could then be connected to the RRCLK- or TRCLK- input and each terminated with 100 ohm to the receive or transmit analog ground respectively. However, this is not recommended because the resulting the width of a 100 Ohm trace is very narrow (less than 3 mil). This width will be difficult for board manufacturers to fabricate accurately and reliably. Inaccuracy in the trace impedance will cause the signals to be improperly terminated.

3 S/UNI-LITE CLOCK RECOVERY LOOP FILTER COMPONENTS

The asymmetrical loop filter values were chosen to achieve maximum performance in the LAN environment. As well, to eliminate the power drain of the above mentioned emitter-follower and to achieve maximum jitter tolerance, the jitter transfer 20 db/decade, 130 kHz -3dB point can be sacrificed. Since the S/UNI-LITE is a terminating device and will not be used as a regenerator, the jitter transfer -3 dB point is not relevant.

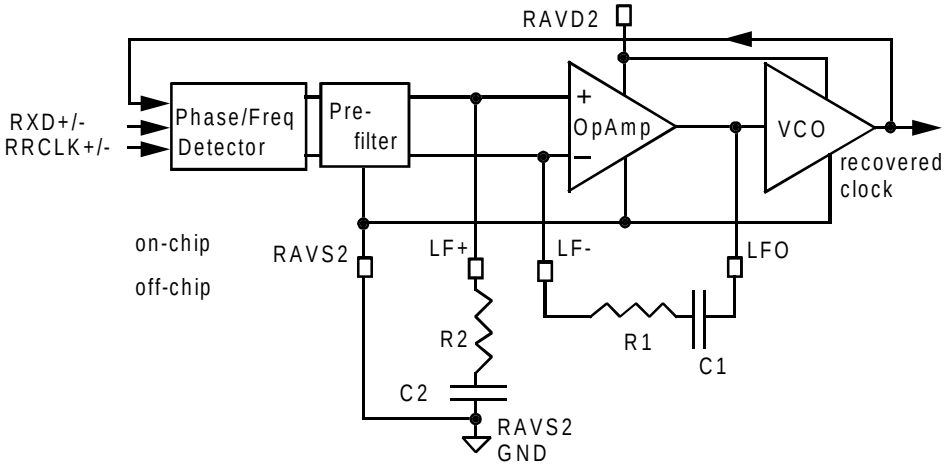
All resistors are 1% metal film (1/8 or 1/10 watt) resistors and all capacitors should be ±10% and non-polarized since under some cases the capacitors may be reversed biased by up to 2 Volts DC. A non-polarized ceramic capacitor or series connected polarized Tantalum capacitors may be used as shown below. Type X7R or X5R dielectric monolithic ceramic capacitors are recommended as these have the most desirable temperature coefficient, are non-polarized and the 0.47µF devices are readily available from several vendors, including AVX, Philips, TDK, Vitramon, and Prestidio.

Table 2 - Recommended Component Values

Line Rate (Mbit/s)	R1 (Ω)	R2 (Ω)	C1, C2 (µF) min	Transfer Function BW
155.52 & 51.84	200	412	0.47 µF	450 kHz
25.92 & 12.96	200	412	2.2 µF	75 kHz

Recommended capacitor values will maintain jitter transfer peaking below the required 0.1 dB level. The capacitor values are the minimum recommended values; larger values of capacitance can be used on any of the line rates.

Figure 8 - Loop Filter Using Ceramic Non-Polarized Capacitors



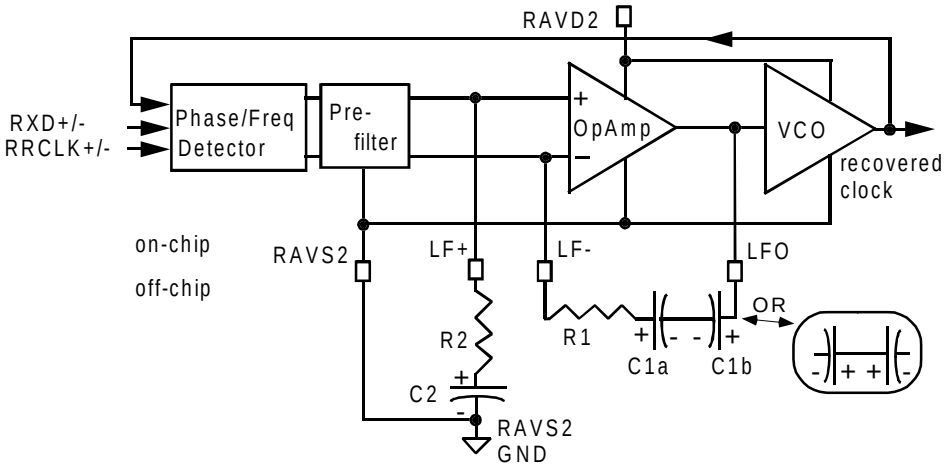
3.1 Polarized Tantalum Capacitors Connected in Series

For lower line rates, a 2.2 µF capacitor is required. Due to footprint requirements, or sourcing constraints, two polarized Tantalum capacitors connected in series may be a more desirable option. Either back to back (-'ve to -'ve) or anode to anode (+'ve to +'ve) may be used to form one non-polar capacitor. Since the effective capacitance will be halved, two 4.7 µF capacitors must be used to form a 2.35 µF non-polar capacitor. Since the LF+ pin will always have a positive DC bias (about +1 Vdc when in lock), C2 may be a single polarized capacitor with the positive terminal connected to the LF+ pin. However, C1 is made up of a series combination of C1a and C1b as shown in the schematic below. AVX corporation publishes several articles on back to back tantalums.

Table 3 -

Line Rate (Mbit/s)	R1 (Ω)	R2 (Ω)	C2 (µF) min.	C1a (µF) min.	C1b (µF) min.	Transfer Function BW
25.92 & 12.96	200	412	2.2	4.7	4.7	75 kHz

Figure 9 - Loop Filter Using Tantalum Polarized Capacitors



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NOTES

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