PM5344

GENERATING TRIBUTARY MULTIFRAME ALIGNMENT DURING A RECEIVED STS-3/STM-1 LOSS OF POINTER.

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OVERVIEW

This application note describes the external circuitry required to generate a stable tributary multiframe alignment (V1 pulse) on the SPTX's DROP BUS during an STS-3/STM-1 loss of pointer condition. The intent of this application note is to address designs that utilize mappers with a common multiframe indication to control both ADD and DROP traffic. Normally, the multiframe synchronization of the ADD traffic and the multiframe synchronization of the DROP traffic is independent; made possible by mappers that have independent multiframe control capability for both directions. In those cases, where the ADD and DROP traffic is independently controlled by two independent multiframe synchronization's, this application note need not be applied.

In most real life LOP situations (i.e. not tester induced LOP) the H4 byte received on the SPTX's RECEIVE BUS cannot be guaranteed to be at the position expected by the SPTX. In this situation the SPTX will read the erroneous data from what it perceives to be the correct H4 byte and will (most likely) proceed to generate an invalid V1 synchronization. The V1 on the DC1J1V1 will in fact become erratic and unusable. The circuitry discussed in this application note corrects the erratic V1 synchronization so that it becomes aligned to the same synchronization as was attained before receiving the LOP condition. The retainment of the old synchronization is desired so that the downstream mapper circuit does not take a hit on the added traffic into the network during the transition to the LOP state. The hit to this traffic during the re-acquisition of the pointer is inevitable and cannot be avoided.

This application note also discusses an alternative reduced gate count circuit to generate an arbitrarily aligned freewheeling V1 pulse. Because the V1 synchronization in this smaller circuit is arbitrarily aligned (as opposed to keeping the old alignment that existed prior to LOP), the mapper circuit will take a one time hit on the added traffic during the transition to the LOP state. It will take a further hit again when the SPTX refinds the pointer.

V1 Pulse Generation Locked To Pre LOP Alignment:

The diagram in figure 1 shows the generation of "GEN_C1J1V1" as a direct replacement for the SPTX's DC1J1V1 output. The circuitry contains four main blocks of logic besides the AND gate, OR gate and INVERTER functions. The four blocks are "3 BIT SHIFT REG", "SPE NUM DECODE", "MUX" and "V1 & J1 GEN".

In normal operation the complete drop bus control signals generated by the SPTX are propagated to the downstream device unaltered. In particular the DC1J1V1 output is completely translated into GEN_C1J1V1 without any modification. During an LOP condition the DC1J1V1 output from the SPTX is modified by an operation that replaces the V1 pulse of the DC1J1V1 with the flywheeling output from the "V1&J1 GEN" block. The GEN_C1J1V1 output can now be used by a

downstream device to add traffic at the alignment indicated by the freewheeling V1 pulses.

The GEN_C1J1V1 output allows the downstream tributary mapper device to add traffic into the network at the same multiframe alignment as was originally attained during normal operation. With a high probability, the added traffic will not be hit in the transition to the LOP state as explained in the "V1&J1 GEN" section below. There exists a low probability that the added traffic will be hit when the SPTX undergoes a change of multiframe alignment before declaration of the LOP state. In such a circumstance the added traffic will be hit once only and will not be hit again until the LOP state is removed. The drop traffic will always be hit since all traffic (passed on by the SPTX to the tributary mapper device) will be lost as long as the LOP state exists.

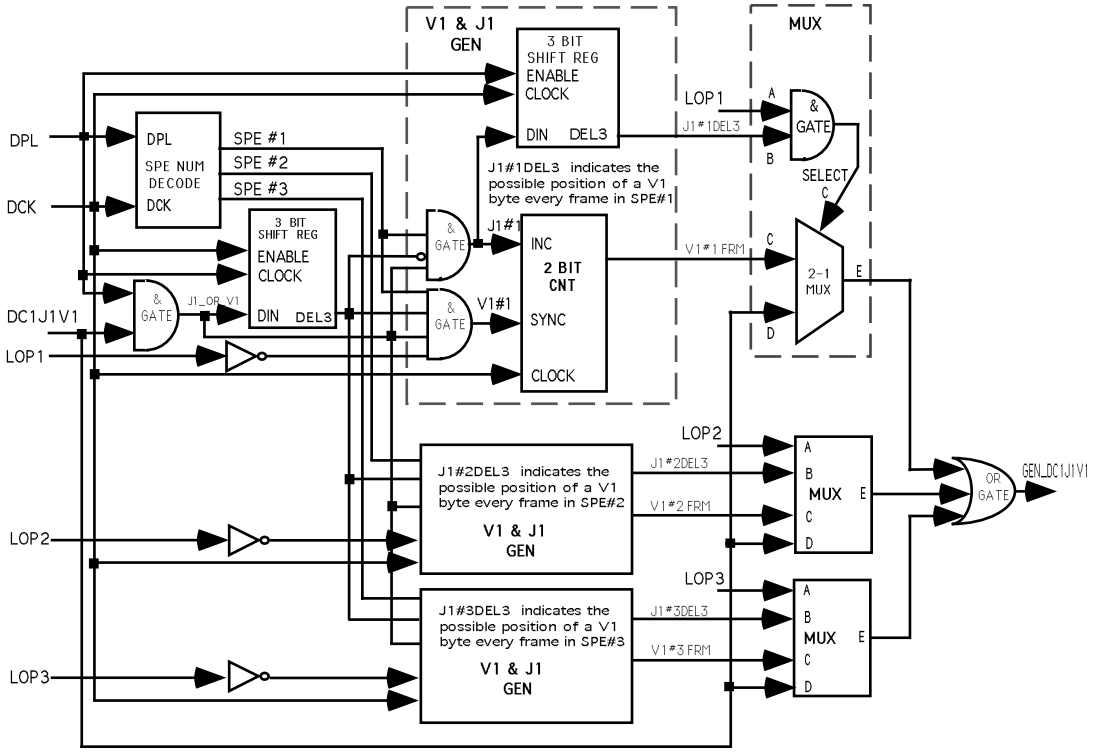

Figure 1: COMBUS Format V1 Generation During LOP

3 BIT SHIFT REGISTER Block:

This block delays its DIN input by three DCK clock cycles. The shifting is inhibited

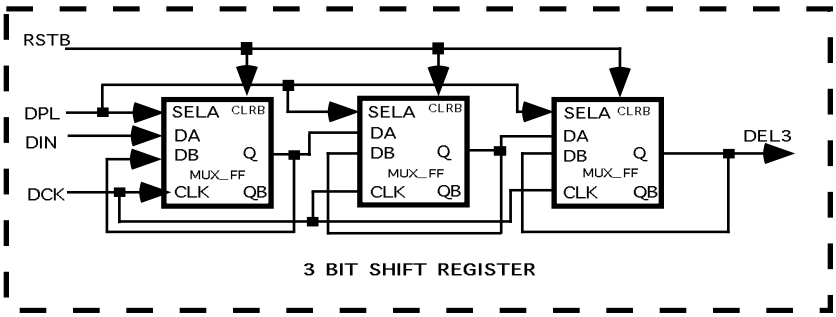

Figure 2: 3 BIT SHIFT REGISTER

during non payload bytes indicated by its DPL input being logic 0. This register is reset during power up reset when RSTB is logic 0.

SPE NUM DECODE Block:

This block generates an indication that identifies the byte time of SPE#1 or SPE#2 or SPE#3. When the SPE#1 output is logic 1 then the byte on the SPTX's DROP BUS belongs to STS-1 #1/STM-0 #1 within an STS-3/STM-1. When the SPE#2 output is logic 1 then the byte on the SPTX's DROP BUS belongs to STS-1 #2/STM-0 #2 within an STS-3/STM-1. When the SPE#3 output is logic 1 then the byte on the SPTX's DROP BUS belongs to STS-1 #3/STM-0 #3 within an STS-3/STM-1.

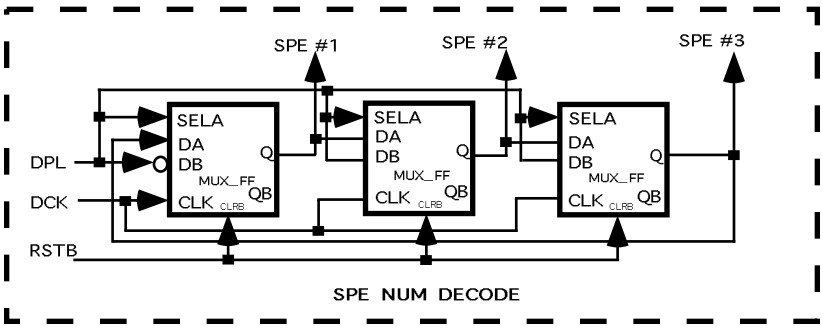

Figure 3: SPE NUM DECODE

When the SPTX is transmitting transport overhead bytes (DPL is logic 0) on the DD[7:0] outputs this block will halt processing. At the beginning of a row of SPE bytes (DPL is logic 1) on the SPTXs' DD[7:0] outputs this block is released from its halt position and will indicate a logic 1 on SPE#1 and logic 0 on SPE#2 and SPE#3 outputs. Thereafter, for the duration of DPL being logic 1, the three MUX_FF's act as a shift register. When DPL goes low for the next transport overhead bytes the register is again held in a halted state.

MUX Block:

This block is explicitly shown as a part of figure 1. It contains one AND gate and one 2:1 MUX. In LOP operation, its functionality is to select input "C", the

generated V1 indication on the "V1#nFRM output. Otherwise, during normal operation, this block will select input "D", the SPTX generated V1 indication. The C1 and J1 indication on the SPTX's DC1J1V1 output is always selected through to the GEN_DC1J1V1 output.

V1 & J1 GEN Block:

This block contains a 2 bit counter, a "3 Bit Shift Register" block (discussed previously) a 3 input AND gate and a 4 input AND gate. There are three instantiations of this block and its only function is to decode the delayed version of J1#n (J1#nDEL3) and the flywheeling V1#n (V1#nFRM). Where n is 1 for STS1 #1, 2 for STS1 #2 or 3 for STS1 #3). The first instantiation decodes indications associated with STS1 #1, the second instantiation decodes indications associated with STS1 #2, the third instantiation decodes indications associated with STS1 #3.

The three input AND gate decodes a J1 byte time on the SPTXs' DROP bus. This indication is used to increment the 2 bit counter (i.e. an increment for each frame) and is input to the shift register function. The four input AND gate is used to decode the V1 byte time on the SPTXs' DROP bus. When not in LOP this indication is used to synchronize the 2 bit counter. The counter therefore always holds the correct multiframe synchronization on the DROP BUS. When in LOP, this AND gate is inhibited and the 2 bit counter keeps flywheeling at the previous synchronization. It is assumed that the LOP output from the SPTX will be asserted before the V1 resynchronization on the SPTXs' DC1J1V1 occurs. This assumption is based on the fact that the change of multiframe alignment will take a minimum of 5 frames (after the beginning of the LOP process, which itself takes eight frames), but most likely it will take greater than the 8 frames required to declare LOP. The likelihood that resynchronization will be established within 8 frames is achieved when random data on the H4 byte occurs in the 4 byte sequence of xxxxxx00 followed by xxxxxx01 followed by xxxxxx10 followed by xxxxxx11 after a previous H4 byte that was anything other than xxxxxx11. This is, intuitively, very small and will be assumed to be negligible for the remainder of this application note. However, in the event that the SPTX actually does establish a V1 resynchronization before declaration of LOP, the circuit described will still generate a flywheeling V1 pulse although it will be at some random alignment. This is not considered to be a major drawback.

V1 Pulse Generation Not Locked To Pre LOP Alignment:

In the event that an initial hit on the added traffic by the tributary mapper device is not considered to be a problem (in most cases this is true) then the circuit can be reduced to a much simplified form. The simplification would be to remove the "SPE NUM DECODE" block, remove two of the "V1&J1 GEN" blocks and two of the "MUX" blocks shown in figure 3. Also, the "V1&J1 GEN" block would not need to decode for the signal that controls the counter synchronization. Figure 4 shows the resulting circuit.

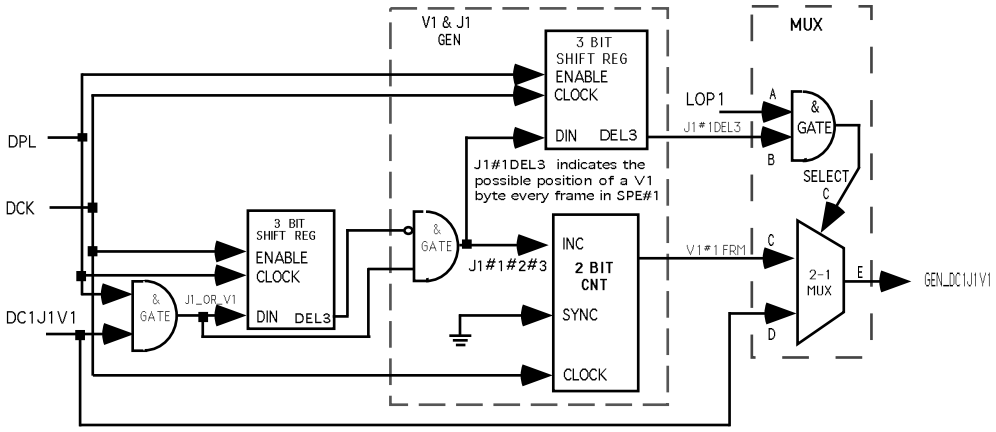

Figure 4: Simplified COMBUS Format V1 Generation During LOP

REFERENCES

[1] PMC-Sierra data book PM5344 (SPTX), May, 1995.

NOTES

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