PM4341A

T1XC

ANSWERS TO FREQUENTLY ASKED QUESTIONS REGARDING THE T1XC

Issue 2: July, 1997

CONTENTS

REFERENCES

- ANSI T1.102 (1993), "Digital Hierarchy — Electrical Interfaces"
- ANSI T1.107 (1995), "Digital Hierarchy — Formats Specifications"
- ANSI T1.403 (1995), "Network-to-Customer Installation — DS1 Metallic Interface"
- Bellcore TR-TSY-000008 (August 1987), "Digital Interface Between the SLC96 Digital Loop Carrier System and a Local Digital Switch"
- Bellcore TA-TSY-000278 (November 1985), "Digital Data System (DDS) — T1 Data Multiplexer (T1DM)"
- ITU-T Recommendation G.703, Blue Book Vol. III, Fascicle III.4 (November 1988), “Physical/Electrical Characteristics of Hierarchical Digital Interfaces”
- ITU-T Recommendation G.704, Blue Book Vol. III, Fascicle III.4 (November 1988), “Synchronous Frame Structures Used at Primary and Secondary Hierarchical Levels”
- PMC-Sierra, PMC-900602R5, Issue 5, Data Book for PM4341A T1XC T1 Framer Transceiver.

DEFINITIONS AND TERM GLOSSARY

AIS — Alarm Indication Signal. This is a signal consisting of unframed all-ones serial digital data. It is transmitted when there is no good data to transmit (due to an upstream failure), and is useful for maintaining a timing reference to downstream equipment. This signal can be detected and transmitted by the T1XC.

AMI — Alternate Mark Inversion. This is a ternary coding scheme for electrical transmission of digital data. Each binary one that is transmitted is represented by a RZ pulse which is of opposite polarity of the preceding pulse. Each binary zero that is transmitted is represented by a space (no pulse).

ANSI — American National Standards Institute. This is a non-profit, non-government federation of standards-making and standards-using organizations. It publishes standards, but does not develop them. Compliance with an American National Standard is voluntary and does not preclude anyone from manufacturing, marketing, purchasing, or using products, processes, or procedures not conforming to the standards.

B8ZS — Block Eight Zeros Substitution. This refers to a zeros suppression scheme which replaces eight consecutive zeros with a decodeable sequence of LCVs. Zero suppression is important to ensure proper operation of clock recovery circuits

CDRC — Clock and Data Recovery unit. This is PMC-Sierra's mnemonic to refer to the functional block in the T1XC which recovers the timing of the received signal, then uses that timing to sample the received data.

CRC — Cyclic Redundancy Check. This is a scheme for error monitoring by making a Boolean cyclic polynomial calculation over a digital data payload. The transmitter transmits the results of this calculation, and the receiver compares this to it's own calculation. If there is a difference, it is assumed that one or more bits have been corrupted during transmission of the digital payload. Of the standardized DS1 formats, only ESF uses a CRC.

DAC — Digital-to-Analog Converter. This term is used generically to refer to a circuit which converts digital information into an analog signal. In the T1XC, a DAC is used to create the transmitted line pulses.

DJAT — Digital Jitter Attenuator. This is PMC-Sierra's mnemonic for the functional block within the T1XC which attenuates phase jitter on the transmit timing reference. It contains a digital PLL to create a jitter-attenuated clock, and a FIFO to absorb the phase jitter.

DS1 — Digital Signal, Level 1. This term refers to a standardized (ANSI T1.107) format for transmitting serial digital data at 1.544Mbps.

DSX-1 — Digital Signal Cross-Connect, Level 1. This term refers to the interface at a digital cross-connect (a convenient central point of cross-connecting, rearranging, patching and testing digital equipment and facilities) operating at the DS1 level.

ELST — Elastic Store. This is PMC-Sierra's mnemonic for the functional block within the T1XC which provides the elastic store function. The ELST is used for adapting the received data to the system backplane rate. Since these signals are not necessarily synchronized, they may slip with respect to each other. The function of the ELST is to control the slips such that they occur on the frame boundaries indicated on the backplane. For example, if the received data is faster than the system backplane then the ELST will drop full frames of data while maintaining the timeslot alignment on the backplane.

ESF — Extended Superframe Format. This is a standardized (ANSI T1.107) DS1 format. It makes use of the DS1 F-Bits to provide a 24-frame signaling multiframe, CRC error checking, and an out-of band maintenance channel.

F-Bit — Framing Bit. This term denotes the first bit of each DS1 frame which is used for carrying the framing overhead information. The specific use of this bit depends on the DS1 framing format.

FEAC — Far-End Alarm and Control. This term is applied to channels in a transmitted data stream which are reserved for carrying alarm and control information to and from the far-end equipment.

FIFO — First-In First-Out buffer. This term refers to a digital buffer which outputs data in the same order as it was input.

ISDN — Integrated Services Digital Network. This is a world-wide public telecommunications network that is implemented as a set of digital switches and paths supporting a broad range of services.

ITU-T International Telecommunication Union - Telephony. This is a committee within a United Nations treaty organization. The charter is "to study and issue recommendations on technical, operating, and tariff questions relating to telegraphy and telephony." Its primary objective is end-to-end compatibility of international telecommunications connections.

LCV Line Code Violation. This term denotes a received bipolar pulse which violates the AMI or B8ZS ternary coding scheme. LCV events are detected and accumulated by the T1XC.

Long-Haul This term applies to T1 interconnections over 100Ω twisted pair cable which are more than the 655 feet specified in DSX-1 electrical interface specifications (e.g. ITU-T G.703). Cable distance up to 6000ft are typical of long-haul connections. ANSI T1.403 specifies that the signal attenuation that can be expected over a long-haul cable span is 22dB, although most long-haul receivers are designed to operate with attenuation up to 36dB.

LOS Loss-of-Signal. This term refers to the state a clock recovery unit is in when there is no input signal. Since DS1 requires either a minimum pulse density or the use of a zero code suppression scheme (such as B8ZS), the T1XC monitors for LOS by monitoring the number of consecutive spaces (zeros) received.

NRZ Non-Return-to-Zero. This refers to the common electrical coding scheme for serial digital data. Logical ones are represented as a pulse which is high for the full bit period. Logical zeros are represented as no pulse for the full bit period. This scheme is useful for serial digital data which has an associated clock signal.

OOF Out-Of-Frame alignment. This is the state an DS1 framer is in if it cannot find the frame alignment pattern within the received serial 1.544Mbps data.

PCM Pulse-Coded Modulation. A term encompassing digital serial data which is encoded into electrical pulses. AMI and B8ZS are PCM coding schemes.

PLL Phase-Locked Loop. The generic term for a feed-back system which generates a clock with a fixed (locked) phase/frequency relationship to some reference clock.

RPSC Receive Per-Channel Serial Controller. This is PMC-Sierra's mnemonic for the functional block of the T1XC which allows per-channel functions to be performed on the received PCM and signaling data, before being passed to the receive backplane.

RSLC Receive Pulse Slicer. This is PMC-Sierra's mnemonic for the functional block of the T1XC which receives the analog line pulses conforming to ANSI T1.102 and ITU-T G.703 electrical interface specifications.

RZ Return-to-Zero. This refers to an electrical coding scheme for serial digital data. Logical ones are represented as a pulse which is high for half the bit period then returns to low (zero) for the remainder of the bit period. Logical zeros are represented as no pulse. This scheme is useful for serial digital data from which a clock must be recovered.

SF Superframe Format. This is a standardized (ANSI T1.107) DS1 format. It makes use of the DS1 F-Bit to maintain a 12-frame signaling multiframe.

SIGX Signaling Extractor. This is PMC-Sierra's mnemonic for the functional block of the T1XC which extracts and stores the received robbed-bit (channel-associated) signaling information. It also provides some per-channel functions on the received PCM data.

SLC®96 Subscriber Loop Carrier 96. This is a standardized (Bellcore TR-TSY-000008) DS1 format. It is similar to SF, but makes use of the F-Bits such that it also carries a datalink. This datalink is used for concentrating up to four DS1 streams for an aggregate of 96 (4 x 24) 64kbps channels.

T1 Transmission format level 1. This term is used loosely to describe systems carrying DS1-formatted signals electrically over cable.

T1DM T1 Data Multiplexer. This is a standardized (Bellcore TA-TSY-000278) DS1 format. It uses Timeslot 24 of the DS1 frame to pass additional framing information as well as a datalink.

T1XC T1 Transceiver. This is PMC-Sierra's mnemonic for the PM4341A T1 framer/transceiver device.

TPSC Transmit Per-Channel Serial Controller. This is PMC-Sierra's mnemonic for the functional block of the T1XC which allows per-channel functions to be performed on the PCM and signaling data from the transmit backplane, before transmission.

XPLS — Transmit Pulse driver. This is PMC-Sierra's mnemonic for the functional block of the T1XC which generates the analog transmit pulses conforming to ANSI T1.102 and ITU-T G.703 electrical interface specifications.

BACKGROUND AND OVERVIEW

PMC-Sierra's PM4341A T1 Framer/Transceiver is a full-featured device for terminating 1.544Mbps digital telecommunications links.

Due to the versatility of the T1XC, the data book for that device is quite lengthy. In order to help customers quickly find the answers to their questions, the following list of answers to frequently asked questions has been compiled.

FREQUENTLY ASKED QUESTIONS

Q1) How should the T1XC be initialized by software?

A1) There are four main configurations of the T1XC corresponding to the four T1 framing formats: SF, ESF, SLC®96, and T1DM.

The T1XC is designed modularly, so each functional block in the device needs to "know" what framing format is being used. In the Operations section of the T1XC data book, there are tables which explain how to configure the T1XC from reset for the various framing formats.

In addition to setting up the framing format, there is some additional initialization which should be done: setting the timing options, initializing the per-channel serial controllers (the RPSC, TPSC, and SIGX functional blocks), and selecting internal versus external HDLC processing.

The timing options are configured using Register 07H in the T1XC. The proper timing option depends on the hardware connections used. The description of Register 07H in the T1XC data book explains which timing option is suited to particular hardware implementations.

The per-channel serial controllers use internal indirect registers for controlling the per-channel functions. These internal indirect registers do not come up in a known default state — they must be initialized if the per-channel serial controllers are enabled. The method of programming and initializing the per-channel serial controller indirect registers is explained in the section entitled "Using the Per-Channel Serial Controllers" in the T1XC data book. The values to which these indirect registers should be initialized depends on the application.

The T1XC provides the ability (with the RFDL and XFDL functional blocks) to process the HDLC (LAPD) information carried on the ESF facility datalink. Alternatively, the ESF facility datalink or ISDN primary rate D-Channel (carried in Timeslot 24) can be extracted to the RDLSIG output and inserted from the TDLSIG input. When the RFDL and XFDL are enabled, the HDLC payload and status information is available through registers. This information can either be accessed via the host microprocessor, or an external DMA controller can be dedicated to this task. To facilitate the use of an external DMA controller, the RDLSIG, RDLCLK, TDLSIG and TDLCLK pins can operate as interrupt signals. All of these options for HDLC processing are controlled in Register 02H. Additionally, the XFDL and RFDL, if used, are enabled with the EN bits in Registers 34H and 38H respectively.

Q2) How can the T1XC be configured to operate its receiver in un-framed (transparent) mode?

A2) Receiving un-framed mode implies that the framer does not "care" if a framing pattern is present in the incoming data. Therefore, the frame alignment is unknown.

To receive un-framed data on the T1XC, the UNF bit in Register 00H should be set to a logic one. This holds the FRMR functional block in reset (suppressing framer alarms), and disables the ELST from overwriting the trouble code (contained in Register 1EH) on the backplane receive data.

The CDRC and ALMI functional blocks continue to operate in un-framed mode, so LOS, LCVs, and AIS can still be detected.

Q3) How can the T1XC be configured to operate its transmitter in un-framed (transparent) mode?

A3) Transmitting un-framed mode implies that the T1XC does not overwrite any of the data from the transmit backplane (applied to the BTPCM input). Therefore, no framing overhead should be written, no robbed-bit signaling inserted, no in-band signaling, and no destructive zero code suppression schemes (B8ZS is allowed).

To transmit un-framed data on the T1XC:

- The framing overhead insertion by the XBAS functional block should be disabled by setting the FDIS bit in Register 06H to logic one
- The TPSC functional block should be disabled by clearing the PCCE bit in Register 30H to logic zero
- The in-band code generation by the XIBC functional block should be disabled by clearing the EN bit in Register 46H to logic zero
- The pulse density enforcing by the XPDE functional block should be disabled by clearing the STUFF bit in Register 59H to logic zero

Note that it is allowable to enable B8ZS encoding (by setting the B8ZS bit in Register 44H to logic one) when transmitting un-framed data.

Q4) What is the difference between using a 37.056MHz and a 12.384MHz clock to drive the XCLK input of the T1XC?

A4) Although the T1XC allows the use of either a 37.056MHz or a 12.384MHz clock as the XCLK input, the 37.056MHz XCLK is recommended for most designs, especially those requiring jitter attenuation or the transmission of analog DSX-1 pulses (rather than a digital transmit interface).

The DJAT functional block of the T1XC requires a 37.056MHz oscillator to operate. Therefore, the 37.056MHz XCLK is necessary if jitter attenuation is desired.

Additionally, the XPLS functional block of the T1XC requires a 12.384MHz clock that is synchronous to the transmit timing reference. Since DJAT provides this functionality, a 37.056MHz XCLK is generally necessary for applications using the transmit analog interface.

Q5) Why is there a specification of a ±32ppm frequency tolerance on the XCLK input?

A5) There are two digital phase-locked loops within the T1XC. The XCLK input is used as the high-speed clock for both PLLs, and therefore sets the free-running frequency of these PLLs.

The frequency capture and lock ranges of a PLL is a function of the free-running frequency. Therefore, to ensure that the specified capture and lock ranges of the PLLs are met, it is important to use an XCLK input with a better than ±32ppm frequency tolerance. Oscillator manufacturers usually provide ±25ppm oscillators which are suitable.

Note that the frequency tolerance of the transmitted line rate will depend on the frequency tolerance of the transmit frequency reference (e.g. the BTCLK or TCLKI input), *not* the XCLK input.

Q6) What are some recommended oscillator manufacturers?

A6) Any reputable crystal oscillator manufacturer should be able to provide the required 37.056MHz oscillator to source the T1XC's XCLK input signal. Since this is a non-standard frequency, they will generally have to be custom cut. The 1100 series of custom-cut crystal oscillators is suitable and available from most manufacturers. The oscillator should output TTL (or TTL-compatible) levels.

Some manufacturers which PMC-Sierra has used in-house with the T1XC are: Champion Technologies, Connor-Winfeld, Ecliptek Corporation, and Fox Corporation. These should be available from most electronics components distributors.

Custom cut oscillators can have very long lead times (16 weeks typical) so they should be ordered well in advance of when they will be needed.

Q7) Can PMC-Sierra specify the line protection circuitry for line cards using the T1XC?

A7) Due to the liability associated with line protection circuitry, PMC-Sierra is limited to specifying the functional requirements of the line interface. However, there are independent consultants available to make these specifications. Also, the manufacturers of the line interface components (particularly the transformers) should have information related to line protection circuitry.

If circuitry is added to the line interface circuitry recommended in the T1XC data book (in the Functional Description of the RSLC and XPLS functional blocks), then PMC-Sierra's Application Support Engineers are available to review the design to ensure that the functional operation of the line interface is not adversely affected by the additional protection circuitry.

Q8) What are some recommended transformer manufacturers?

A8) Most reputable telecommunications transformer manufacturers will be able to provide a product compatible with the T1XC. The typical characteristics of a compatible transformer are:

Turns Ratio (PRI:SEC)	OCL (mH min.)	$C_{w/w}$ (pF max.)	L_L (µH max.)	DCR pri. (Ω max.)	DCR sec. (Ω max.)
1:2 for Rx, 1:1.36 for Tx	1.20	35	0.80	0.80	1.2

where OCL is the open-circuit inductance,
$C_{w/w}$ is the inter-winding capacitance,
L_L is the leakage inductance, and
DCR is the DC resistance.

Some transformer manufacturers which PMC-Sierra has used in-house with the T1XC are: Pulse Engineering, and BH Electronics.

Some other transformer manufacturers which produce transformers compatible with the T1XC are: Filtran, Midcom, and Schott. These should be available from most electronics components distributors.

Q9) How should a DSX-1 pulse template be measured?

A9) ANSI T1.102 Section 5.1 explains the procedure for pulse template testing. Section 6.1.2 of that same standard gives the specific requirements for DSX-1 electrical interfaces.

It is important to realize that the DSX-1 pulse is measured for compliance at the input port. The compliance template is normalized to account for the cable loss, but the transmitter must still compensate for the cable — especially the low-pass characteristics. In the T1XC, Register 14H controls the line length setting. The SM bit in that register should be set to logic one and the ILS[2:0] bits set according to the length of the physical cable between the transmitter and the termination (input port) where the template test is being performed.

Proper cable (meeting ANSI T1.403 Annex E cable characterization parameters) must be used. This means that the cable has a characteristic impedance of 100Ω measured at 772kHz. T1 cable from a telco should be adequate although compliance test houses use specially calibrated cable. Also, the test must be performed with the cable properly terminated (100Ω resistively). Test houses use a 0.01% resistor, but 1% should be adequate.

Isolated pulses must be used. ANSI T1.403 defines an isolated pulse as "a pulse free from the effects of other pulses in the same signal. A suitable testing signal for DS1 is a pulse preceded by at least four zeros and followed by at least one zero."

No "weird" oscilloscope functions (i.e. averaging, enveloping, etc.) should be enabled although some test systems use some averaging to eliminate the effects of noise (which are not taken into account by the T1.102 specification).

PMC-Sierra only guarantees the template matching capability of the T1XC when the recommended transmit line interface circuit is used (in the Functional Description of the XPLS functional blocks). Additionally, the T1XC must be operated within its stated operating environment.

Q10) What are typical results of DSX-1 template testing on the T1XC?

A10) Appendix A of this document contains typical template tests results for the T1XC.

Q11) How is a long-haul circuit implemented using the T1XC?

A11) In terms of functionality, long-haul implies that cable lengths that cause up to 36dB of attenuation (corresponding to approximately 6000 ft) can be used on a long-haul T1 span.

The long-haul requirement mainly affects the receiver implementation, usually requiring an integrated equalizer. The RSLC (Receive Pulse Slicer) functional block on the T1XC is designed for DSX-1 interfaces, not long-haul. Therefore, in order to add long-haul capability to the T1XC, a long-haul LIU or repeater should be used in conjunction with the T1XC.

There is a PMC-Sierra application note (PMC-940934) available which explains the functional considerations necessary for a long-haul design based on the T1XC. Contact your local PMC-Sierra Sales Representative to obtain a copy of that application note.

Q12) How are mimic framing patterns guarded against?

A12) When the T1XC is trying to find the frame alignment within the received serial data, it may encounter a mimic framing pattern. A mimic framing pattern occurs when more than one bit within a 193-bit window are following the framing pattern sequence. The T1XC will consider both of these as "framing bit candidates" and will need additional information to figure out which one is the real alignment pattern and which are mimics.

In general, the spurious mimic framing patterns are present in random data. However, these are transient and infrequent enough that they will not cause a DS1 framer undue problems when trying to find frame alignment.

More persistent mimic framing patterns can occur though. One case is the "malicious" user that transmits a mimic framing pattern in a user channel. Another common case is when the CRC-6 overhead of an ESF-formatted signal mimics the framing pattern (which is also cyclic every six bits). This latter case occurs often when the ESF payload is made up of idle channels filled with certain constant patterns.

In order to alert the system to the presence of mimic framing patterns, the T1XC provides the MFPI and MFP bits in Register 22H. Additionally, for ESF framing mode, the T1XC provides an alternate framing algorithm to meet the requirements of ITU-T G.706 Section 2.2.2 which specifies that, "when the CRC-6 code is utilized for error performance monitoring, it may also be used to provide immunity against spurious frame alignment signals." To enable that algorithm, the ESFFA bit in Register 20H should be set to logic one when in ESF framing mode. This alternate algorithm uses the CRC-6 information to validate a framing bit candidate — it is extremely improbable that a mimic framing pattern will also contain the correct CRC-6 information.

Q13) What is the relationship between the BRFPI input and the BRFPO output of the T1XC?

A13) The BRFPI input is only used when the ELST functional block is active. (This is controlled by the ELSTBYP bit in Register 00H.)

With the ELST enabled, BRFPO is generated as a divide-down of BRCLK. The modulo of the counter is determined by the receive backplane rate setting (controlled by the BRX2M bit in Register 01H): for the 1.544MHz backplane the counter divides BRCLK by 193; for the 2.048MHz backplane the counter divides BRCLK by 256. Provided that there is a BRCLK signal, BRFPO will always be present.

The counter generating BRFPO from BRCLK is synchronously reset by the BRFPI input such that the BRFPI and BRFPO signals are aligned.

BRFPO can be configured as a superframe pulse (controlled by the BRXSFP bit in Register 01H). When BRFPO is configured as a superframe pulse, then another counter is activated which further divides the regular frame pulse by 12 (or 24) to indicate the superframe (or extended superframe) boundaries.

There is another bit, ALTBRFP, provided in Register 01H which can divide the BRFPO by another factor of 2. This bit is mainly used for SF-to-ESF interworking where the 12-frame SF superframe indication is converted into a 24-frame pulse suitable for the ESF formatted signal.

The counter generating the superframe pulse is *not* reset by the BRFPI input. This means that a superframe pulse applied to BRFPI will not necessarily be aligned with a superframe pulse output on BRFPO, although there will be an integral number of frames separating them. This is shown in the T1XC data book's Timing Diagrams section in the figure entitled "1.544MHz Receive Backplane Interface — without signaling alignment."

When the T1XC is in frame alignment, the F-Bit position in the BRPCM and BRSIG output signals will always be aligned to the BRFPO pulse. It is recommended that BRFPO, rather than BRFPI, should be used to indicate the backplane frame alignment to external circuitry although BRFPI is permissible.

Q14) Can BRFPO be connected to BRFPI on the T1XC?

A14) Yes, there is no problem with feeding back BRFPO as the BRFPI for the same ESLT. The BRFPI resets the counter generating BRFPO such that no clocking loop will occur.

With BRFPO connected to BRFPI, the BRFPO counter will chose some arbitrary point to assert the BRFPO signal after a reset (software or hardware) of the T1XC. From then on, the feedback to the BRFPI input will keep the BRFPO at that same position with respect to BRCLK.

Q15) Does the T1XC require a BRFPI signal to generate BRFPO?

A15) No. It is valid to tie BRFPI low (to digital ground) and allow BRFPO to free-run as a divide-down of the BRCLK input.

In this case, the BRFPO counter will chose some arbitrary point to assert the BRFPO signal after a reset (software or hardware) of the T1XC. From then on, the BRFPO will continue to be generated every time the counter "rolls over" thus maintaining that alignment with respect to BRCLK.

Q16) If the ELST is bypassed, how is the BRFPO output signal generated?

A16) The ELST can be bypassed by setting the ELSTBYP Bit in Register 00H to a logic one.

When the ELST is bypassed, the BRFPO, BRPCM, and BRSIG output signals will be updated with RCLKO, and the BRCLK and BRFPI inputs are ignored. Note that with the ELST bypassed, the system receive backplane must be timed to the recovered line rate (indicated on the RCLKO output).

BRFPO is a feed-through of the RFP signal, but will not be aligned with the RFP output due to differences in the path delays. The BRFPO signal will indicate the frame alignment (the F-Bit position) on the BRPCM and BRSIG signals.

Additionally, BRFPO can be configured as a superframe pulse (controlled by the BRXSFP bit in Register 01H). When BRFPO is configured as a superframe pulse (BRXSFP=1), then a counter is activated which divides the 8kHz frame pulse by 12 (or 24) to indicate the superframe (or extended superframe) boundaries.

There is another bit, ALTBRFP, provided in Register 01H which can divide the BRFPO by another factor of 2. This bit is mainly used for SF-to-ESF interworking where the 12-frame SF superframe indication is converted into a 24-frame pulse suitable for the ESF formatted signal.

Note that the F-Bit position (frame alignment) of the BRPCM and BRSIG output signals will always be aligned to the BRFPO pulse.

Q17) How can the T1XC be configured to operate in Looptime and Source Time?

A17) The T1XC can be configure to operate in Looptime by setting the PLLREF1 bit in register 07H to logic one and the PLLREF0 bit to logic zero. This will feed the RCLKO clock to the transmit output clock, TCLKO. The BTCLK line should be tied to the TCLKO line externally to avoid slip in the transmit FIFO.

To operate T1XC in Source time, the PLLREF[1:0] bits in register 07H are set to “11”. This selects the external clock source from the TCLKI input as the reference source for the TCLKO output line. The BTCLK line should be tied to the TCLKO line externally to provide synchronization.

Q18) When utilizing the T1XC/SUNI-PDH, how do I configure the registers in the two devices for Looptime and Source Time Configurations?

A18) The T1XC can be interfaced to the S/UNI-PDH by connecting the BTCLK pin to the TCLK pin on the PDH, the TCLKO pin to the PDH’s TICLK pin, and the TCLKI pin to an external oscillator. Single rail data line should be selected by both devices to provide framing information.

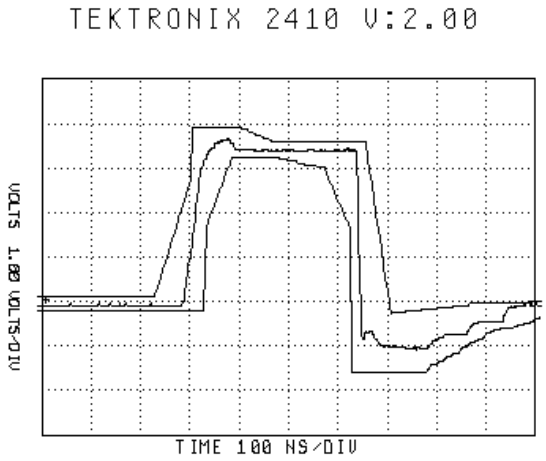
Based on the above connections, the T1XC/SUNI-PDH can be operated in Looptime configuration by setting the PLLREF1 bit in register 07H on the T1XC to logic one and the PLLREF0 bit to logic zero. This selects the RCLKO as the reference source for TCLKO. The TCLKO is connected to PDH's TICLK and is used as the reference source for the PDH's transmit data line, TDAT. The PDH should be set to either the E1 ADM or PLCP mode to disable the PDH's loopback function.

From the same connections, the T1XC/SUNI-PDH can be operated in Source time configuration by setting the PLLREF[1:0] bits to "11" in register 07H. This selects TCLKI, which is connected to an external clock source, as the clock for TCLKO on the E1XC.

APPENDIX A. TYPICAL T1XC TEMPLATE TEST RESULTS

The following figures show the typical results of template testing. Each line length build-out setting of the T1XC (controlled in Register 14H) is tested against the associated range of real cable.

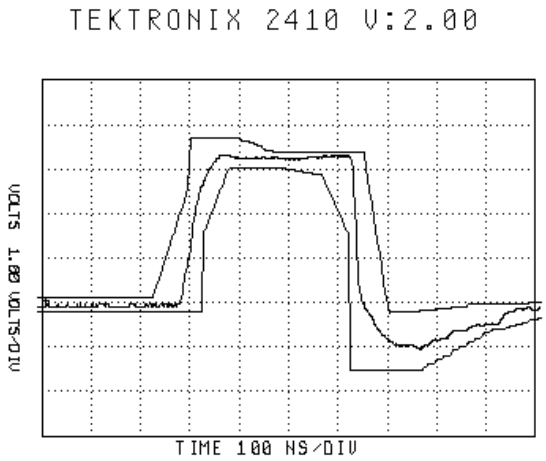
0-110ft Build-Out @ Cable Length=0ft:



DS1 TEMPLATE TEST ** PASS **
STANDARD: ANSI T1.102
SETUP FILE: DS1.SET
TEMPLATE: DS1.WVD ANSI-FIT
DATE: 03/10/94 TIME: 16:59

AMPL 3.48V WIDTH 332.0nS OFFSET -118mV
RISE 34.4nS FALL 6.5nS

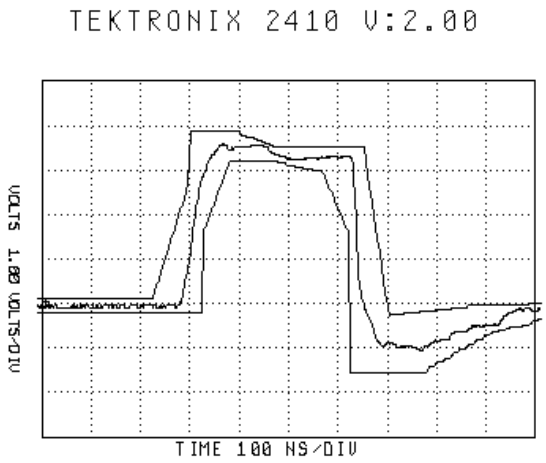
0-110ft Build-Out @ Cable Length=110ft:



DS1 TEMPLATE TEST ** PASS **
STANDARD: ANSI T1.102
SETUP FILE: DS1.SET
TEMPLATE: DS1.WVD ANSI-FIT
DATE: 03/10/94 TIME: 17:02

AMPL 3.31V WIDTH 332.0nS OFFSET -110mV
RISE 50.5nS FALL 14.3nS

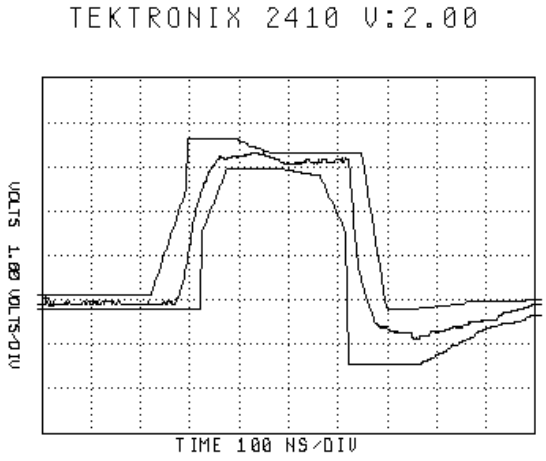
110-220ft Build-Out @ Cable Length=110ft:



DS1 TEMPLATE TEST ** PASS **
STANDARD: ANSI T1.102
SETUP FILE: DS1.SET
TEMPLATE: DS1.WVD ANSI-FIT
DATE: 03/10/94 TIME: 17:03

AMPL 3.43V WIDTH 330.0nS OFFSET -100mV
RISE 42.9nS FALL 14.3nS

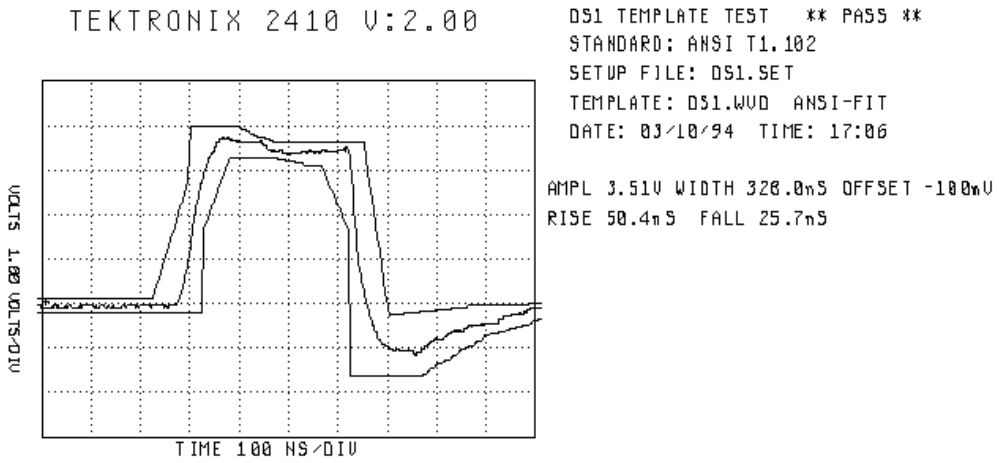
110-220ft Build-Out @ Cable Length=220ft:



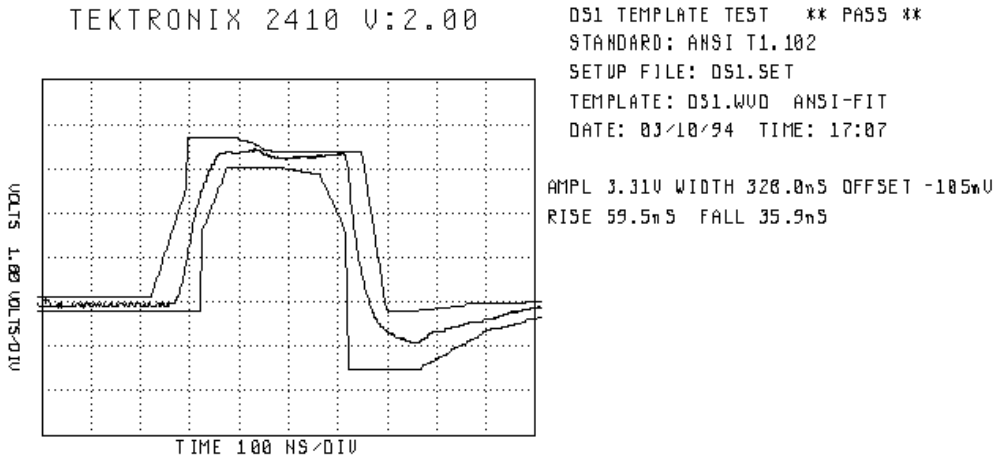
DS1 TEMPLATE TEST ** PASS **
STANDARD: ANSI T1.102
SETUP FILE: DS1.SET
TEMPLATE: DS1.WVD ANSI-FIT
DATE: 03/10/94 TIME: 17:05

AMPL 3.24V WIDTH 328.0nS OFFSET -110mV
RISE 54.6nS FALL 27.9nS

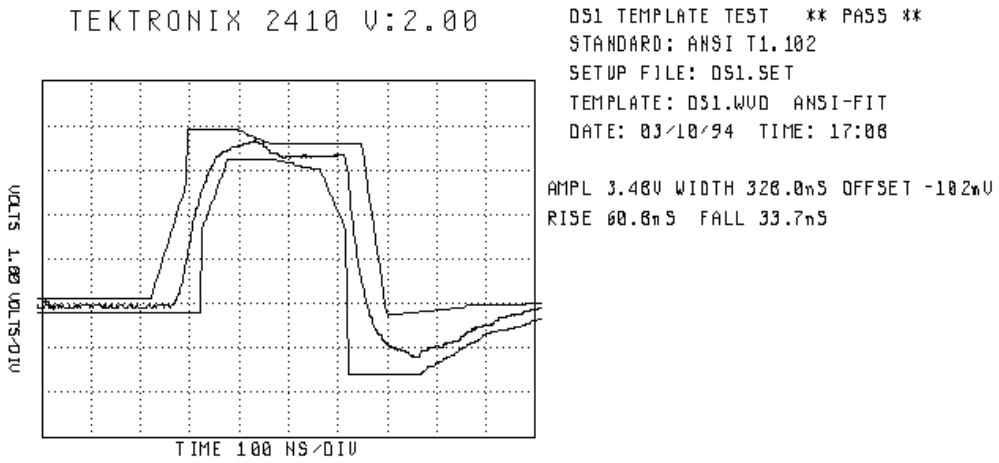
220-330ft Build-Out @ Cable Length=220ft:



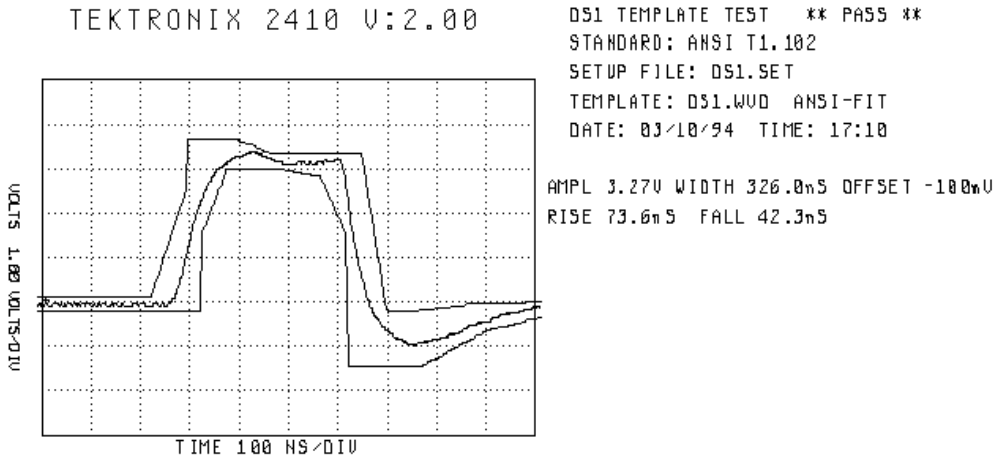
220-330ft Build-Out @ Cable Length=330ft:



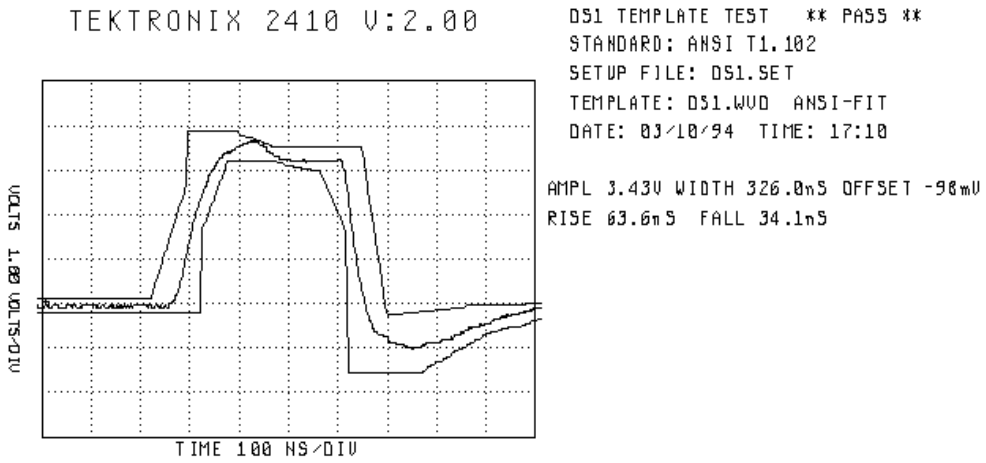
330-440ft Build-Out @ Cable Length=330ft:



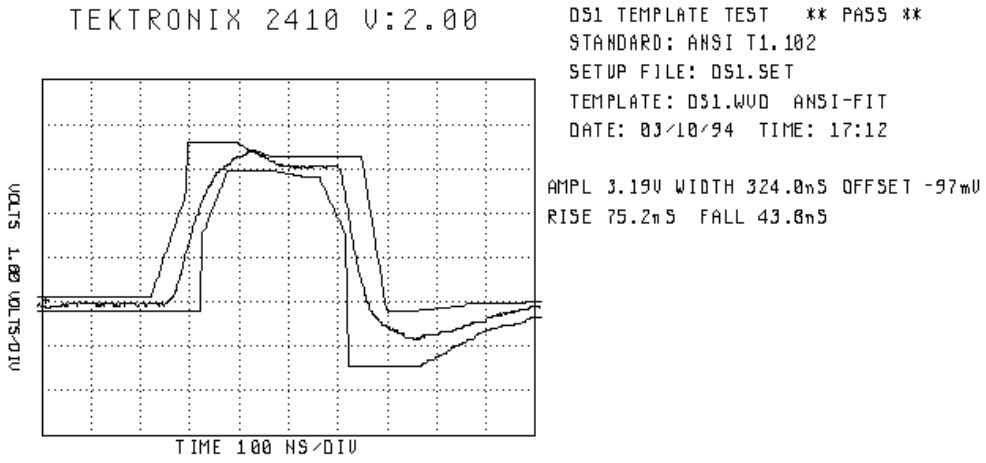
330-440ft Build-Out @ Cable Length=440ft:



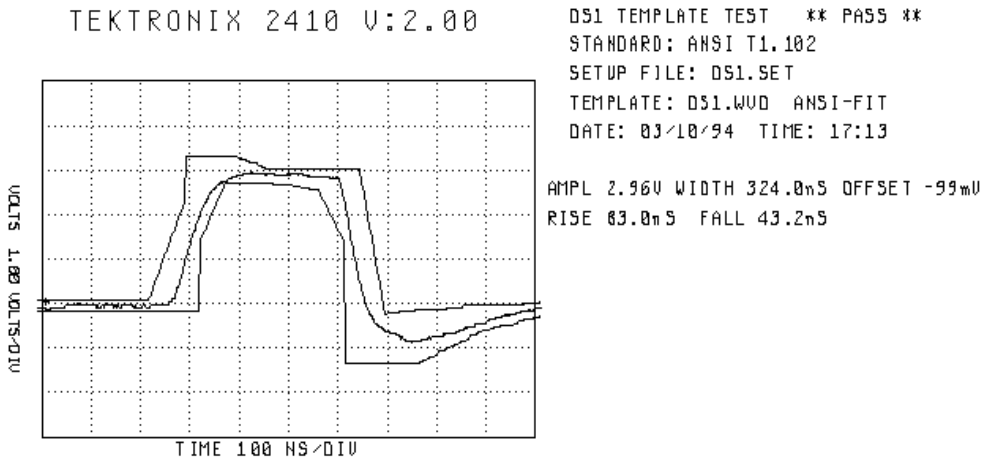
440-550ft Build-Out @ Cable Length=440ft:



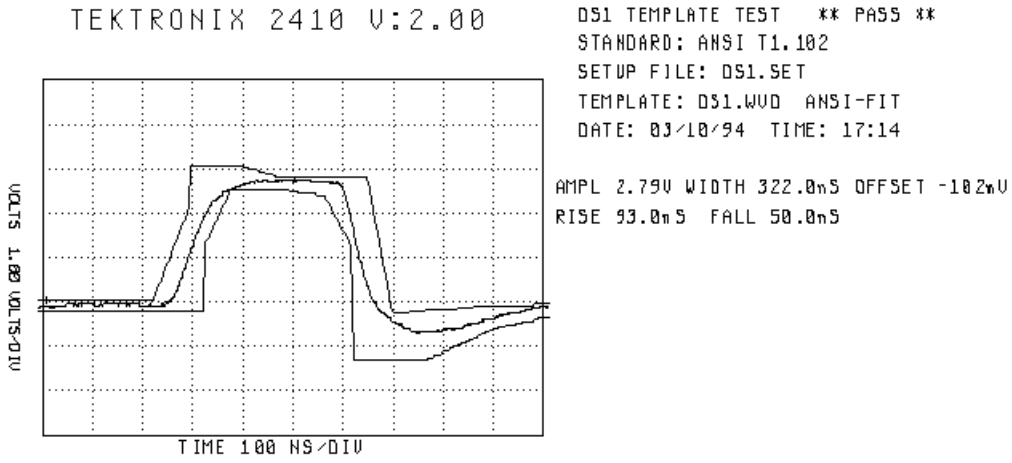
440-550ft Build-Out @ Cable Length=550ft:



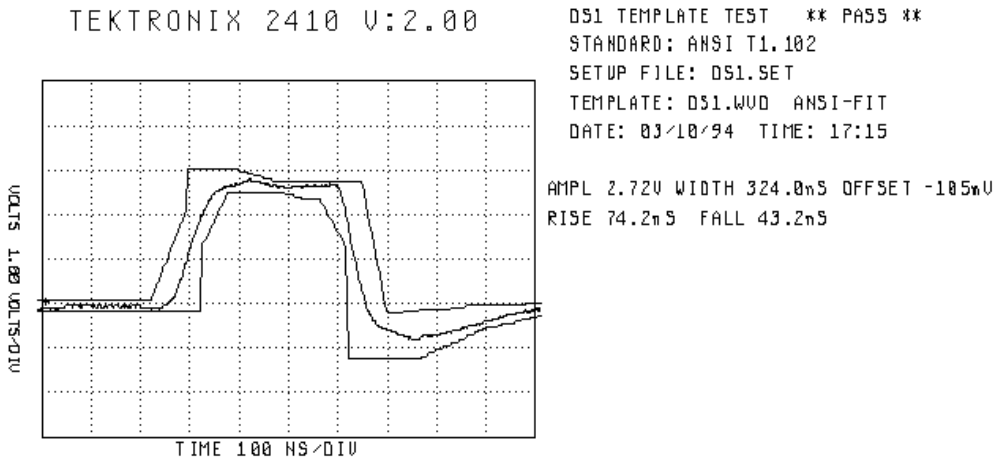
550-660ft Build-Out @ Cable Length=550ft:



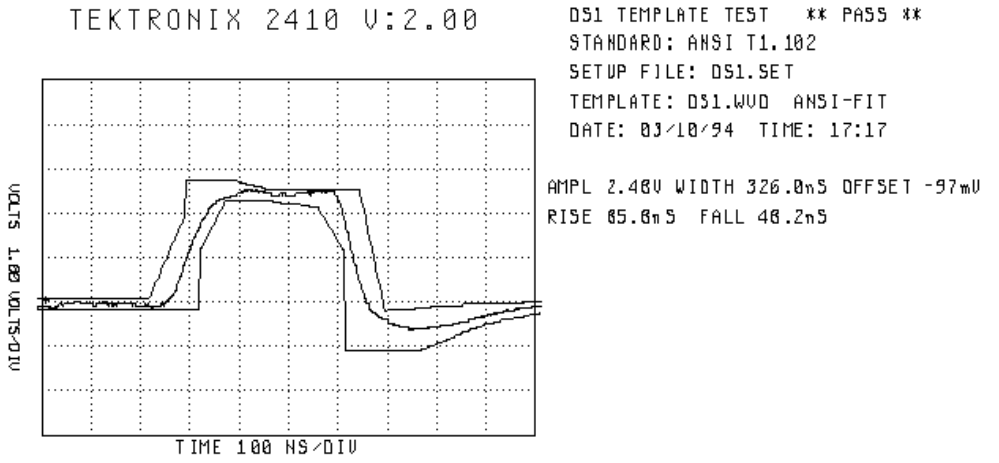
550-660ft Build-Out @ Cable Length=660ft:



>655ft Build-Out @ Cable Length=660ft:



>655ft Build-Out @ Cable Length=715ft:



NOTES

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