PM7322

RCMP-800

DATA SHEET ERRATA

ERRATA

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CONTENTS

1 LEGEND

1. unaltered text is unchanged to add context to changes

2. new material is bold and Italicized

~~3. obsolete material is struck out~~

4. comments specific to this document are in italics

5. A vertical bar in left margin indicates that this is a new item which was not present in the previous issue of this document.

2 CHANGES TO DATASHEET ISSUE 6

The Congestion Control feature is removed. Hence Changes 2.1 to 2.3, 2.5 to 2.13.

2.1 Pg. 1

- ~~Discards on command all low priority (high CLP bit) cells to relieve switch congestion.~~

2.2 Pg. 2

- Counts maintained for entire device include total cells input, total cells output, OAM cells, ~~cells discarded due to congestion,~~ corrupted OAM cells, and cells with unassigned/invalid VPI/VCIs.

2.3 Pg. 25

~~CONG~~ ***VSS_DC21***	~~Input~~ ***Ground***	123	~~The congestion indication (CONG) input signals that cell congestion is occurring in an element downstream of the RCMP-800 and that all low priority cells be dropped. If CONG is high, the RCMP-800 drops all cells with a one in the CLP bit position after policing has occurred, except AAL5 end-of-message (EOM) cells. (Dropping an EOM cell results in corrupting two packets; this does help to relieve the congestion.)~~ ~~CONG may be treated as an asynchronous input.~~ ***This ground pin should be connected to GND in common with VSS_DC.***

2.4 Pg. 40

Table 1 VC Table Record

SA[19:16]	MSB(39)					LSB(0)
0000	Reserved for Search Table					
0001	MSN (8)		TUC (16)		Reserved for Search Table (16)	
0010	NNI (1)	Search FieldB (11)	VPI (12)		VCI (16)	
0011	Status ~~(4)~~	Config ~~(6)~~	Extended Status ~~(9)~~	OAM Config ~~(8)~~	UDF ~~(8)~~	BWD Routing Tag ~~(5)~~

The field widthes should be as follows:

SA[19:16]	MSB(39)					LSB(0)
0000	Reserved for Search Table					
0001	MSN (8)		TUC (16)		Reserved for Search Table (16)	
0010	NNI (1)	Search FieldB (11)	VPI (12)		VCI (16)	
0011	Status	Config ***(4)***	Extended Status ***(6)***	OAM Config ***(9)***	UDF ***(8)***	BWD Routing Tag ***(8) (5)***

2.5 Pg. 48

AAL5 Packet Tagging and Dropping

An AAL5 packet can be up to 1366 cells long. If a cell is dropped early in a packet due to policing ~~or congestion~~, then the remaining cells of the packet represent wasted bandwidth. Optionally, all remaining cells of a packet can be dropped or tagged once a single cell has been dropped or tagged.

2.6 Pg. 49

- ~~number of CLP=1 cells dropped due to congestion~~

2.7 Pg. 59

~~Congestion Control~~

~~Congestion control is handled by a single signal, CONG, entering the device. When this signal indicates that congestion is being experienced by the switch core, all low priority cells (high CLP bit) are discarded. This includes cells which are made low priority during the policing process.~~

2.8 Pg. 66

The “Count of Cells Dropped Due to Congestion” register is removed since the Congestion Control function is removed.

0x34	~~Count of Cells Dropped Due to Congestion~~ ***Reserved***

2.9 Pg. 125

Register 0x30: Counter Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	~~R~~	~~DROPCH~~ ***Reserved***	X
Bit 4	R	INVALCH	X
Bit 3	R	OAMERRCH	X
Bit 2	R	OAMCH	X
Bit 1	R	XFER	X
Bit 0	R	OVR	X

This register contains status information indicating when counter data has been transferred into the holding registers and indicating whether the holding registers have been overrun. It also indicates if the any of the counts are non-zero.

~~DROPCH:~~

~~The DROPCH bit is set to logic 1 if the Count of Cells Dropped Due to Congestion is a non-zero value.~~

2.10 Pg. 126

XFER:

The XFER bit indicates that a transfer of counter data (i.e. data for one or more of the ~~Dropped Cells Due to Congestion register,~~ Invalid Cell Count register, Errored OAM Cell Count register and Valid OAM Cell Count register) has occurred. A logic 1 in this bit position indicates that a latch request, initiated by writing to one of the counter register locations, was received and a transfer of the counter values has occurred. A logic 0 indicates that no transfer has occurred. The XFER bit is cleared (acknowledged) by reading this register. The XFERI bit of the Master Interrupt Status #1 is set when the XFER bit is asserted.

2.11 Pg. 130

~~Register 0x34: Count of Cells Dropped Due to Congestion~~

~~Bit~~	~~Type~~	~~Function~~	~~Default~~
~~Bit 15~~	~~R~~	~~DROP[15]~~	~~X~~
~~Bit 14~~	~~R~~	~~DROP[14]~~	~~X~~
~~Bit 13~~	~~R~~	~~DROP[13]~~	~~X~~
~~Bit 12~~	~~R~~	~~DROP[12]~~	~~X~~
~~Bit 11~~	~~R~~	~~DROP[11]~~	~~X~~
~~Bit 10~~	~~R~~	~~DROP[10]~~	~~X~~
~~Bit 9~~	~~R~~	~~DROP[9]~~	~~X~~
~~Bit 8~~	~~R~~	~~DROP[8]~~	~~X~~
~~Bit 7~~	~~R~~	~~DROP[7]~~	~~X~~
~~Bit 6~~	~~R~~	~~DROP[6]~~	~~X~~
~~Bit 5~~	~~R~~	~~DROP[5]~~	~~X~~
~~Bit 4~~	~~R~~	~~DROP[4]~~	~~X~~
~~Bit 3~~	~~R~~	~~DROP[3]~~	~~X~~
~~Bit 2~~	~~R~~	~~DROP[2]~~	~~X~~
~~Bit 1~~	~~R~~	~~DROP[1]~~	~~X~~
~~Bit 0~~	~~R~~	~~DROP[0]~~	~~X~~

~~DROP[15:0]:~~

~~The DROP[15:0] bits represent the number of cells that have been discarded due to an assertion of the CONG input since the last time the count was transferred. The count is transferred by writing to either address 0x00, 0x31,~~

~~0x32, 0x33 or 0x34. Such a write transfers the internally accumulated dropped cell count to this register within three SYSCLK cycles and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that ensures that coincident events are not lost.~~

2.12 Pg. 138

The CONG pin is removed from the following list for test mode 0.

	0x41	0x48	0x4A	0x5C	0x62	0x63	0x64	0x7A	0x7B
D[15]		IDAT[15][1]			SD[15]	SD[31]			
D[14]		IDAT[14][1]			SD[14]	SD[30]			
D[13]		IDAT[13][1]	IPOLL		SD[13]	SD[29]			
D[12]		IDAT[12][1]			SD[12]	SD[28]	SP[4]		
D[11]		IDAT[11][1]	IBUS8	~~CONG~~	SD[11]	SD[27]	SP[3]	OBUS8	
D[10]		IDAT[10][1]	ISOC[1]		SD[10]	SD[26]	SP[2]		
D[9]		IDAT[9][1]	IPRTY[1][1]		SD[9]	SD[25]	SP[1]		
D[8]		IDAT[8][1]	IPRTY[0][1]		SD[8]	SD[24]	SP[0]		
D[7]		IDAT[7][1]	ICA[4][1]		SD[7]	SD[23]	SD[39]		
D[6]		IDAT[6][1]	ICA[3][1]		SD[6]	SD[22]	SD[38]		
D[5]		IDAT[5][1]	ICA[2][1]		SD[5]	SD[21]	SD[37]		
D[4]	ONESEC	IDAT[4][1]	ICA[1][1]		SD[4]	SD[20]	SD[36]		
D[3]	TCK	IDAT[3][1]			SD[3]	SD[19]	SD[35]		
D[2]	TRSTB	IDAT[2][1]			SD[2]	SD[18]	SD[34]		
D[1]	TMS	IDAT[1][1]			SD[1]	SD[17]	SD[33]		
D[0]	TDI	IDAT[0][1]			SD[0]	SD[16]	SD[32]		ORDENB

2.13 Pg. 140

The CONG pin is changed to an Internal Delay element in the Boundary SCAN chain. The logic value to be expected in the chain location is indicated in parenthesis.

Pin/Enable	Type	Boundary Scan Register Bit	Pin/Enable	Type	Boundary Scan Register Bit
SYSCLK	I	91	CSB	I	33
IDAT[15:0]	I	90:75	WRB	I	32
IPRTY[1:0]	I	74:73	RDB	I	31
ISOC	I	72	RSTB	I	30
IFCLK	I	71	INTB	O	29
IAVALID_ICA[4]	I/O	70	DREQ	O	28
IADDR_OEB (for IAVALID_ICA[4] & IADDR_ICA[3:2])	E	69	OTSEN	I	27
IADDR_ICA[3:2]	I/O	68:67	OBUS8	I	26
ICA[1]	I	66	ORDENB	I	25
IADDR_IWRENB[4:2]	O	65:63	OCA	O	24
IWRENB[1]	O	62	OFCLK	I	23
IPOLL	I	61	OSOC	O	22
IBUS8	I	60	ODATOEB (for ODAT[15:0], OSOC and OPRTY[1:0]	E	21
ONESEC	I	59	OPRTY[1:0]	O	20:19
D[15:0]	I/O	58:43	ODAT[15:0]	O	18:3
DOEB (for D[15:0])	E	42	BUSYB	O	2
A[6:0]	I	41:35	~~CONG~~ ***Internal Delay (Expect Logic 0)***	I	1
ALE	I	34	HIZ*	E	0

2.14 Patent Information

No patent information in the original data sheet.

Note: The technology discussed is protected by one or more of the following Patents:

U.S. Patent No. 5,889,778 U.S. Patent No. 6,108,303 U.S. Patent No. 6,128,766 Canadian Patent No. 2,181,293 Canadian Patent No. 2,209,887 UK Patent No. 2,303,521 Japanese Patent No. 2,965,907

Relevant patent applications and other patents may also exist.

3 ANOMALIES

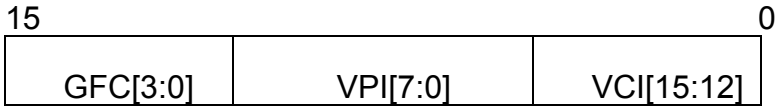
3.1 Data corruption in the first word of a cell

The RCMP can corrupt the first 16-bit word of an ATM cell under certain circumstances. **This error occurs only when OAM cells are inserted in the cell slot immediately before the outgoing user cell** (ie. there is no delay between the OAM cell and the user cell). Only the non-overwritten (ie. not translated or replaced with other fields) portion of the incoming header can get corrupted. **Therefore, if OAM functions are not enabled, this problem does not exist.**

The corrupted word may be prepended or postpended information, or the first 16-bit word of the ATM cell header, depending on the cell length which is controlled by the output cell configuration programmed in the RCMP (register 0x38). The following describes the three cases that could occur:

Case 1: Output cell has 27 words

If the RCMP is configured to output only 27-word cells (i.e. 53-byte ATM cells in 16-bit mode), then the following fields can get corrupted:



If the RCMP is configured to overwrite part of the first header word, then only the non-overwritten portion of the header can get corrupted. For example, if the RCMP is configured to perform VP switching on a connection, the VPI field and the GFC field will be correct, but VCI[15:12] fields can get corrupted.

Case 2: Output cell has prepend words

If there are prepend (with or without postpend) words, then it is the first 16-bit word of prepend that can get corrupted, and the header bytes of the cell will not be affected. Note that corruption occurs only if the incoming prepend words are not overwritten. That is, if the GPREPO bit of RCMP register 0x18 is set to a logic 1, then the incoming prepended words will be replaced, and no corruption of that first word will occur. For the case where incoming cells have 27 words only, and prepend words are added to the output cell, then no corruption occurs, since the prepend words are considered to be “overwritten”.

Case 3: Output cell has postpend words

If there are only postpend words, then it is the first 16-bit word of postpend that can get corrupted, and the header bytes of the cell will not be affected. Note that corruption only occurs only if the incoming postpend words are not overwritten. That is, if the GPREPO bit of RCMP register 0x18 is set to a logic 1, then the incoming postpend words will be replaced, and no corruption of that first word will occur. For the case where incoming cells have 27 words only, and postpend words are added to the output cell, then no corruption occurs, since the postpend words are considered to be "overwritten".

Work-Around

1) Do not use the 27-word mode (ie. RCMP outputing 27-word cells)

or

2) If you do need to use the 27-word mode, do the following:

- Configure the RCMP to output 28-word cells, with the extra word being a postpend word:
  - Write 8043 to register 0x38 and then write 8042 to the same register. The "8043" is to reset the output FIFO first.
- Set the OCALEVEL0 bit in register 0x38 to 0, to configure the OCA signal to deassert four words before the end of the cell

* This assumes that the device receiving cells from the RCMP uses the OSOC signal to indicate start-of-cell, and will start accepting the words of the cell aligned to the OSOC signal (words that may have arrived before the OSOC would be discarded).

Mechanism of work-around:

The first time when the RCMP outputs a 28-word cell, the receiving device will read the first 27 words, accepts the cell and then stop. At the same time, since the OCALEVEL0 bit is set to 0, the OCA signal will have deasserted when 27 words have been read.

Now, when the RCMP has a new cell to output, it asserts OCA. This time, there is the last word of the previous cell (this word is simply garbage) still remaining in the FIFO. When the receiving device asserts the read enable (ORDENB), it reads this "garbage" word, and then it reads the first word of the new cell, and so on. However, the OSOC signal will only be asserted aligned to the first word of the new cell. Therefore, the receiving device will resync its counter and read in the 27 words of the new cells, and will discard the garbage cell.

This then repeats for any new cells that are output by the RCMP.

This work-around has been tested in the lab, running full 622Mbps traffic.

3.2 OCA Deassertion

There is an anomaly in the operation of OCA when the OCALEVEL0=0 mode is used (ie. the "early deassertion mode"). When a cell enters the FIFO at the same time the last word of a cell is read out, OCA is errorneously asserted and then deasserted on the next cycle. The problem does not exist if OCALEVEL0=1.

Workaround:

1. Do not use the OCALEVEL0=0 mode. Almost all applications do not require this mode. This is because the "early deassertion mode" is only useful for an input interface, where the "CA" signal indicates that the FIFO is almost full, such that it cannot accept another cell. Now, if the source sending the cell to this input is heavily pipelined, then this "early deassertion" would be used to avoid queuing another cell to be sent.
   Since in the case of the RCMP, it is an output interface, this "early deassertion mode" is almost never used.

2. Sample OCA on two successive cycles before reading out a cell.

NOTES

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