PM5355

POINT TO POINT PROTOCOL OVER SONET USING THE S/UNI-PLUS & S/UNI-622

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TABLE OF CONTENTS

1 OVERVIEW

1.1 Introduction

This application note addresses the need to transfer a point to point protocol (such as the Internet Protocol, IP, or any other packet based protocol) over the SONET/SDH payload envelopes of the STS-12c/STM-4, STS-3c/STM-1 or STS-1/STM-0 frame.

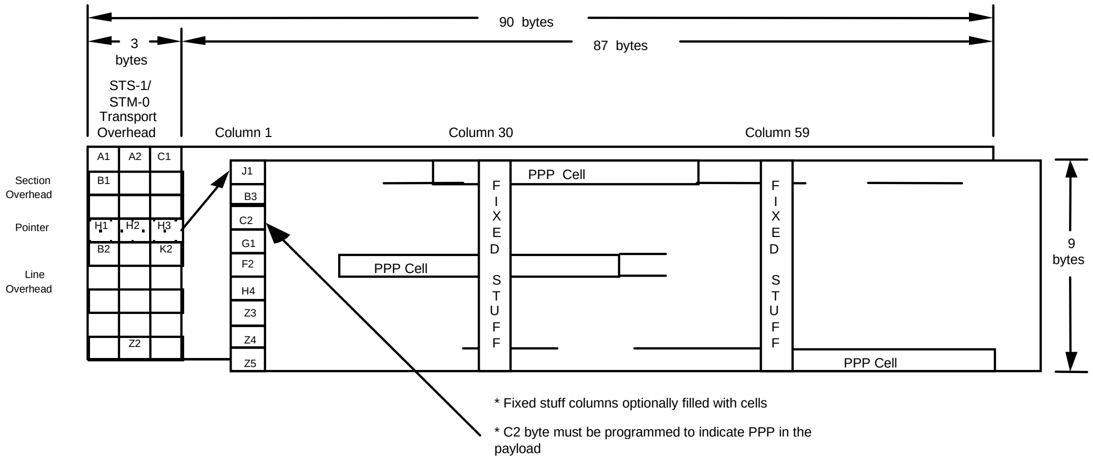
The S/UNI-622 and S/UNI-PLUS are utilized in a special mode of operation that allows the ATM functionality to be bypassed. Additional external logic is required that adapts the SCI-PHY bus cell format to interface to the PPP/POS Assembler/Disassembler. The exact required software and external glue logic varies depending upon the exact implementation. Possible implementations include using a 16 bit 27 word SCI-PHY cell format or an 8 bit 53 byte SCI-PHY cell format. The scope of this application note will be to describe the complete implementation details (consisting of both the software programming of the S/UNI devices, the external logic required for adapting the ATM SCI-PHY interface, and the scrambling/descrambling functionality) to allow PPP deployment over SONET/SDH using the S/UNI-622 and S/UNI-PLUS.

As a side effect of disabling the ATM level functionality, one issue to be aware of is that the ATM payload scrambler is also bypassed and as a result there is no PPP data scrambling/descrambling function. Although the higher level SONET/SDH scrambler/descrambler still exists, the lack of a PPP/POS level scrambling/descrambling function makes it much simpler for a malicious user to defeat the clock recovery functionality of a network node, thereby causing the network to fail. At present the "Network Working Group document RFC 1619" states that scrambling is not required when the PPP/POS cells are inserted into the SONET/SDH payload. For future applications this document will be revised to include the requirement of the scrambling/descrambling functionality. In order to address this future requirement, external logic will be included in this application note to implement the scrambling/descrambling function.

1.2 Frame Structures Over Which PPP is Deployed By the S/UNI Devices

Each of the frame structures processed by the S/UNI-622 and the S/UNI-PLUS are shown below in figure 1 to figure 3.

Figure 1 shows the STS-1/STM-0 mapping. The S/UNI-622 and S/UNI-PLUS both support two STS-1/STM-0 mappings, one with the indicated stuff columns containing fixed stuff bytes and the other with the indicated stuff columns used for cell bytes.

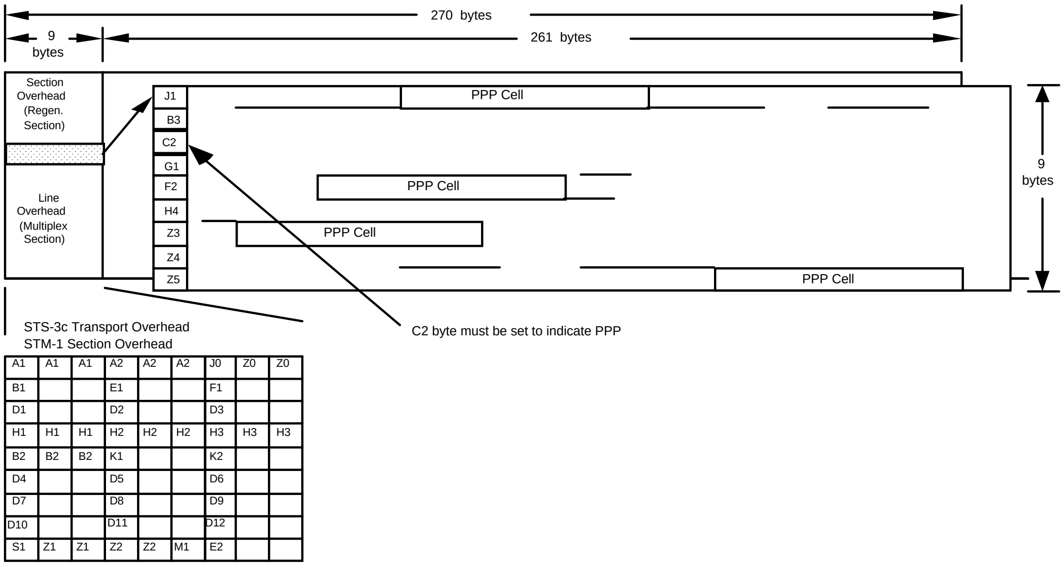


* Fixed stuff columns optionally filled with cells

* C2 byte must be programmed to indicate PPP in the payload

Figure 1: A SONET/SDH STS-1/STM-0 Frame Showing Transport Overhead

Figure 2 shows the STS-3c (STM-1) mapping. In this mapping, no stuff columns are included in the SPE. The entire SPE is used for PPP cell bytes.

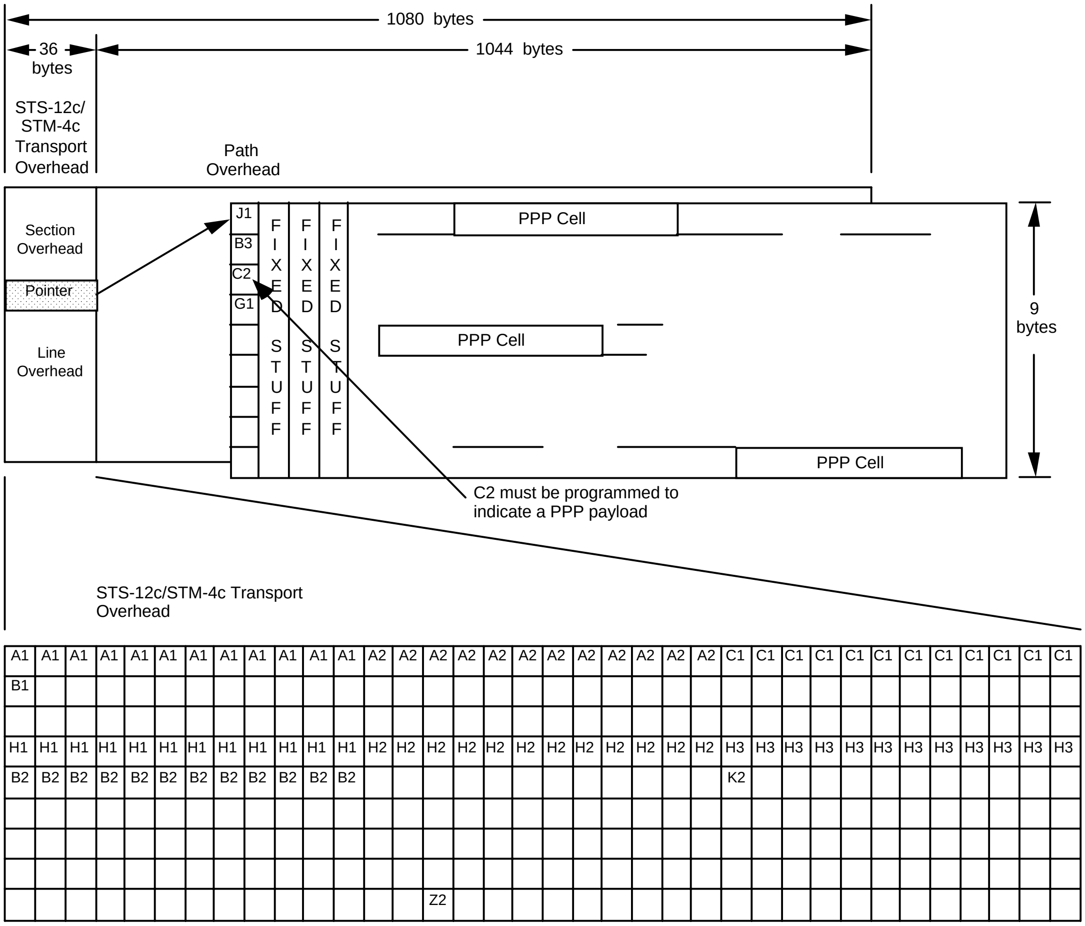

270 bytes
9 bytes
261 bytes
Section Overhead (Regen. Section)
Line Overhead (Multiplex Section)
J1
B3
C2
G1
F2
H4
Z3
Z4
Z5
PPP Cell
PPP Cell
PPP Cell
PPP Cell
9 bytes
C2 byte must be set to indicate PPP

STS-3c Transport Overhead
STM-1 Section Overhead

A1	A1	A1	A2	A2	A2	J0	Z0	Z0
B1			E1			F1		
D1			D2			D3		
H1	H1	H1	H2	H2	H2	H3	H3	H3
B2	B2	B2	K1			K2		
D4			D5			D6		
D7			D8			D9		
D10			D11			D12		
S1	Z1	Z1	Z2	Z2	M1	E2		

Figure 2: A SONET/SDH STS-3c/STM-1 Frame Showing Transport Overhead

Figure 3 shows the STS-12c (STM-4c) mapping. For this mapping, three stuff columns are provided. In this mode of operation, the S/UNI-622 always stuffs the fixed stuff columns with the byte contained in the TACP Fixed Stuff/GFC register. No other options are provided.



A1	A1	A1	A1	A1	A1	A1	A1	A1	A1	A1	A1	A2	A2	A2	A2	A2	A2	A2	A2	A2	A2	A2	A2	C1	C1	C1	C1	C1	C1	C1	C1	C1	C1	C1	C1
B1																																			
H1	H1	H1	H1	H1	H1	H1	H1	H1	H1	H1	H1	H2	H2	H2	H2	H2	H2	H2	H2	H2	H2	H2	H2	H3	H3	H3	H3	H3	H3	H3	H3	H3	H3	H3	H3
B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2													K2											
													Z2																						

Figure 3: A SONET/SDH STS-12c/STM-4c Frame Showing Transport Overhead

2 16 BIT SCI_PHY BUS: ATM BYPASS WITH 16 BIT 27 WORD DATA I/F.

The PM5347 SUNI-PLUS and the PM5355 S/UNI-622 contain an option that disables the ATM Cell Processing and allows raw data to be inserted or extracted from the SONET Payload.

Figure 4 shows the S/UNI-PLUS device operating with the ATM Cell Processing bypassed. Only the ATM cell processing blocks that process the ATM cell validation and delineation functions are bypassed, the rest of the ATM circuitry including the 4 cell FIFO and the SCI-PHY interface still expect to process a 27 word data structure (such as an ATM cell) and therefore still expects the TSOC input to be used correctly.

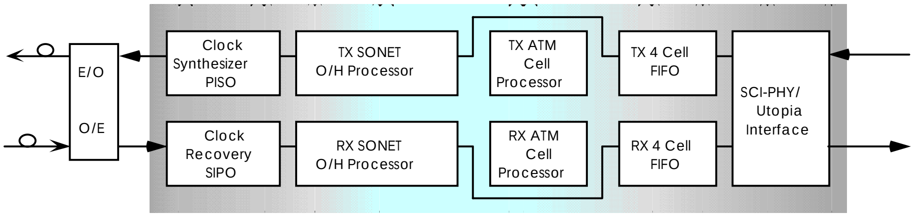


Figure 4: S/UNI-PLUS Operating In ATM Bypass

Figure 5 below shows the S/UNI-622 device operating with the ATM Cell Processing bypassed.

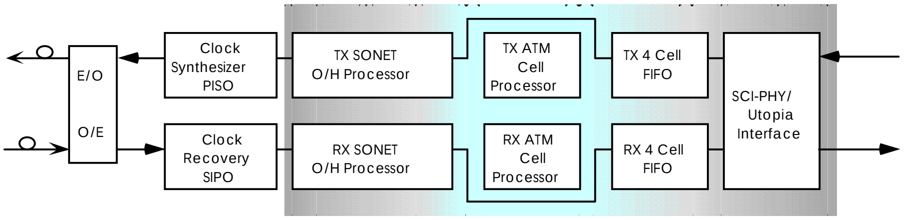


Figure 5: S/UNI-622 Operating In ATM Bypass

Again, as with the S/UNI-PLUS, only the ATM cell processing blocks that process the ATM cell validation and delineation functions are bypassed, the rest of the ATM circuitry including the 4 cell FIFO and the SCI-PHY interface still expect to process a 53 byte data structure.

The SCI-PHY interface expects data from the PPP generator to be received in blocks of 27 words in a 16 bit bus mode of operation. Figure 6 below shows the expected PPP data on the TDAT[15:0] inputs of the S/UNI-622 or S/UNI-PLUS with respect to the TSOC control input.

	Bit 15 Bit 8	Bit 7 Bit 0
Word 1	PPP BYTE 1(ATM H1)	PPP BYTE 2(ATM H2)
Word 2	PPP BYTE 3(ATM H3)	PPP BYTE 4(ATM H4)
Word 3	PPP BYTE 5(ATM HEC)	PPP DUMMY BYTE (HEC STAT/CNTRL)
Word 4	PPP BYTE 6 (ATM1)	PPP BYTE 7 (ATM2)
Word 5	PPP BYTE 8 (ATM3)	PPP BYTE 9 (ATM4)
Word 6	PPP BYTE 9 (ATM5)	PPP BYTE 11 (ATM6)
	⋮	⋮
Word 27	PPP BYTE 52 (ATM47)	PPP BYTE 53 (ATM48)

Figure 5: 27 Word PPP Cell Data Format at the SCI-PHY Interface

The TSOC input must mark PPP byte 1. The PPP dummy byte is a one byte stuff that must be inserted into the transmit FIFO. This dummy byte will not be transmitted over the SONET/SDH payload and hence will not affect bandwidth utilization.

An ATM IDLE cell will be transmitted if the transmit FIFO contains less than 1 full cell at the end of transmitting the last cell. Therefore, in order to successfully implement PPP the transmit FIFO must never become empty. In the receive direction, the cell data format at the SCI_PHY interface is identical and is numbered with respect to the RSOC output. The RSOC output will mark PPP byte 1 and the PPP dummy byte must be dropped before the PPP/POS cell is passed on to the HDLC controller.

2.1 Software Programming For Point to Point (ATM Bypass) Operation

Tables 1 and 2 below describe the register programming required to disable ATM processing in the S/UNI-622 and the S/UNI-PLUS respectively. All affected register addresses are identical for both cases except for the TCAINV bit. The TCAINV bit is located in register 0x03 in the S/UNI-PLUS, but it is in register 0x04 in the S/UNI-622.

Normally, received ATM cells are delineated by the S/UNI device by finding and locking on to the HEC byte. In order to process PPP data, this functionality must be disabled by setting high the CDDIS bit in the RACP block. Once disabled, the incoming data is arbitrarily locked to a random delineation and continuously writes 53 bytes chunk of data to the FIFO. As a direct consequence of this action, the HEC byte now has no meaning and everything associated with this byte must also be disabled. First, the HCSADD bit in the RACP and TACP blocks must be set to logic 0 to disable the addition of the coset polynomial, $x^6+x^4+x^2+1$ to the 5th octet of the

53 bytes residing in the FIFO. Next, the discarding of cells based on the detection of HCS errors must be disabled by setting the HCSPASS bit to logic 1 in the RACP block. The insertion of an internally generated the HEC byte must be disabled by setting the HCSB bit to logic 1 in the TACP block. The DDSCR bit controls the descrambling of the cell payload when data is received by the RACP. Setting DDSCR to a logic one disables this feature. In the transmit direction the DSCR bit controls the scrambling of the cell payload. Setting DSCR to a logic one, disables scrambling inside the TACP of the last 48 bytes of the 53 byte transmitted data. Note, that the disabling of the scrambling and descrambling is required because the data is arbitrarily delineated when received at the far end and identification of the scrambled data bytes cannot be made for descrambling purposes. Because the ATM functionality is disabled the DISCOR bit in the RACP must be set to logic 1 to disable the one bit error correction algorithm. For PPP payloads the C2 byte must be set to the hexadecimal value of 16 by writing to the TPOP Path Signal Label register. The HCSCTLEB bit must be set to logic 1 to disable the alteration of the fifth octet (normally the fifth octet is the HCS byte transmitted out to the line) due to the mask information contained in the 6th byte in a 27 word structure (dummy byte). The TCAINV bit must be set to logic 1 to invert the TCA output. Normally, there is no reason to invert this signals, but since the hardware implementation (described in the following sections of this document) directly connects the TCA to TWRENB, the sense of this output must be inverted. Lastly, in the S/UNI-PLUS, the PASS bit in the RACP needs to be set to logic 1 so that POS data that may have boundaries that look like cells with VPI/VCI bytes equal to zero do not get dropped.

Bit	Reg #	Register Name	Value
CDDIS	0x5C	RACP GFC/Misc. Control	1
HCSADD	0x50	RACP Control	0
HCSPASS	0x50	RACP Control	1
DDSCR	0x50	RACP Control	1
DISCOR	0x50	RACP Control	1
PASS	0x50	RACP Control	1
DSCR	0x60	TACP Control	1
HCSB	0x60	TACP Control	1
HCSADD	0x60	TACP Control	0
C2 (PPP Payload)	0x48	TPOP Path Signal Label	16 Hex
HCSCTLEB	0x63	TACP FIFO Control	1
TCAINV	0x03	S/UNI Master Control	1

Table 1: Bit Settings To Bypass ATM Cell Processing & Enable PPP Transport (POS) Over The SUNI-PLUS (PM5347)

Bit	Reg #	Register Name	Value
CDDIS	0x5C	RACP GFC/Misc. Control	1
HCSADD	0x50	RACP Control	0
HCSPASS	0x50	RACP Control	1
DDSCR	0x50	RACP Control	1
DISCOR	0x50	RACP Control	1
PASS	0x50	RACP Control	1
DSCR	0x60	TACP Control	1
HCSB	0x60	TACP Control	1
HCSADD	0x60	TACP Control	0
C2 (PPP Payload)	0x48	TPOP Path Signal Label	16 Hex
HCSCTLEB	0x63	TACP FIFO Control	1
TCAINV	0x04	S/UNI Master Control	1

Table 2: Bit Settings To Bypass ATM Cell Processing & Enable PPP Transport (POS) Over The SUNI-622 (PM5355)

In addition to the above software programming, external hardware must be designed to control the adding and discarding of the dummy byte located in the 6th byte of the 27 word format. This hardware is described in the following section.

2.2 H/W Interface Supporting PPP (POS) On The 27 Word SCI-PHY I/F

Figures 7 and 8 below shows two possible configurations that will enable PPP to be deployed over OC-12c, OC-3c and OC-1. The PCI DMA controller fetches data from memory and passes it to the RFC 1619 HDLC controller. The HDLC controller in turn passes the data through the FIFO manager to the S/UNI-622 (or S/UNI-PLUS).

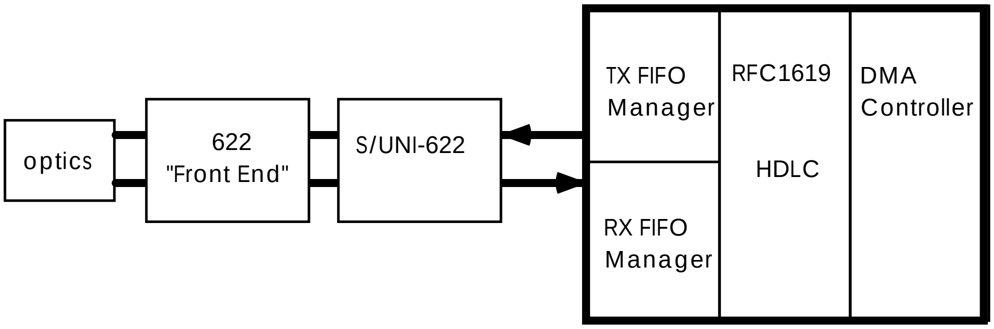


Figure 7: PPP over an OC-12c Link Using 27 Word SCI-PHY I/F

In the transmit direction, the FIFO manager converts PPP data from the HDLC packet assembler and stuffs the dummy byte into the 6th byte of the 27 word interface expected by the SCI-PHY bus. In the receive direction, the FIFO manager converts the 27 word cell from the SCI-PHY interface and destuff (and discards) the 6th byte of the 27 word data structure. The remaining 53 bytes are passed on to the HDLC controller that disassembles the PPP data and transfers it to memory through the DMA controller.

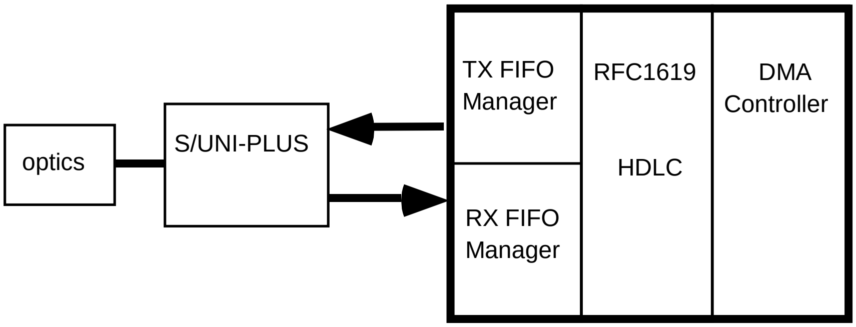
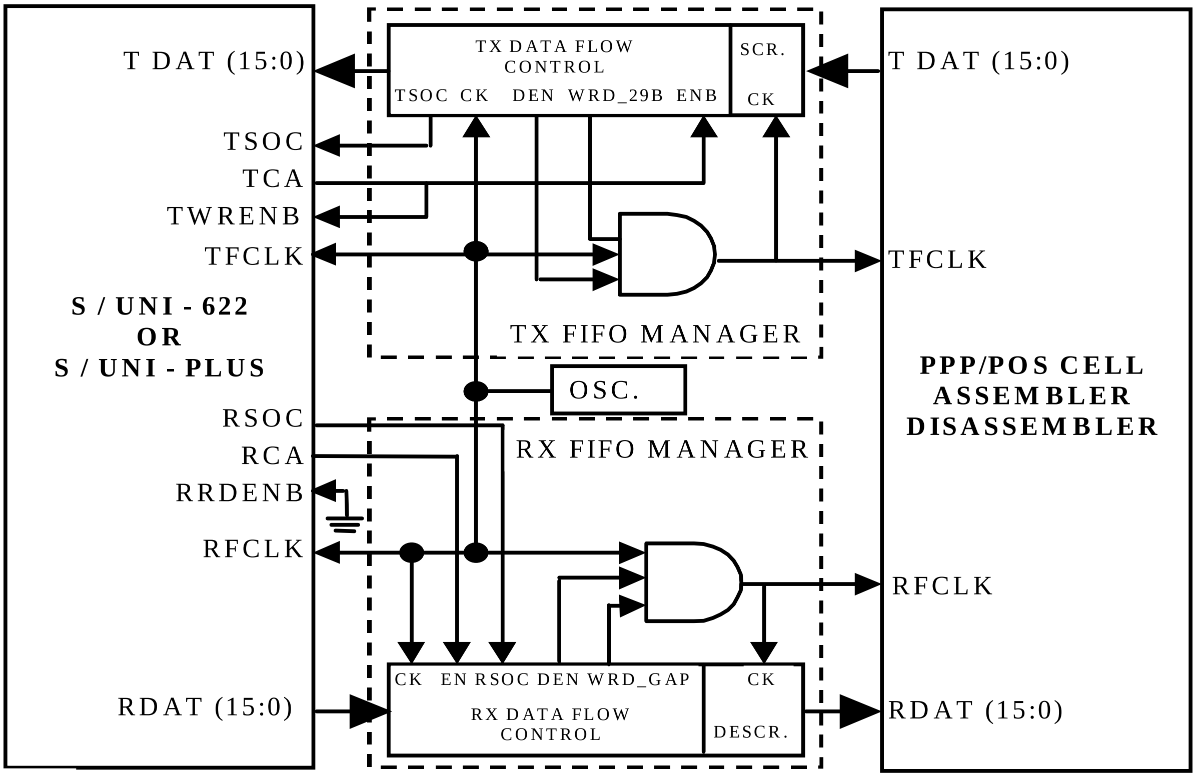


Figure 8: PPP over OC-3c or OC-1 Using 27 Word SCI_PHY I/F

Figure 8 is very similar to figure 7, the main difference being that the S/UNI-PLUS is now used as the line interface (for OC-3 rates) instead of the S/UNI-622 (for OC-12c rates). The biggest advantage of the FIFO manager block is that it is logically identical for both configurations shown above. Only the frequency of operation is different, a minimum of 37.44MHz for OC-12c, 9.35MHz for OC-3c or 3.096MHz for OC-1.

The interface between the S/UNI device and the RFC1619 based HDLC PPP/POS Cell Assembler/Disassembler is shown below in figure 9.



NOTE: The TCA output must be inverted by programming TCAINV to logic 1.

Figure 9: PPP over an STS-3c, STS-12c or an STS-1 Link Using 16 Bit Bus Interface.

The RX FIFO Manager generates a gapped clock to the PPP/POS Cell Assembler/Disasembler. A gap of one word period every 54 words is generated to account for the two dummy bytes received from the S/UNI within a 54 word period. As a result, only 53 words are transferred to the PPP/POS Cell Assembler/Disasembler for every 54 words received from the S/UNI device. Similarly, the TX FIFO Manager generates a one word gap to the PPP/POS Cell

Assembler/Disassembler every 54 words to account for the insertion of dummy bytes into the S/UNI device. i.e. for every 53 words received from the PPP/POS Cell Assembler/Disasembler, 54 words are transferred into the S/UNI device, and a gap of one byte period every 53 words received from the PPP/POS Cell Assembler/Disassembler is generated to account for this.

In the transmit direction the TCA output is directly connected to the TWRENB input of the S/UNI device. This enables writes to the transmit FIFO as soon as there is space available for one or more cells. In this way, the transmit FIFO is not allowed to go empty as long as the clock frequency does not fall below the frequency required to support full bandwidth of an OC-12, OC-3 or an OC-1 signal. The TCA output also controls the counter (EN input) and the gapping of the clock to the Cell Assembler/Disasembler. The counter is disabled from counting when TCA indicates a FIFO full status and at the same time the PPP/POS Cell Assembler/Disasembler is stopped from being clocked.

2.2.1 TX Data Flow Control Block Description

The TX Data Flow Control block controls the clock gapping to the PPP/POS Assembler/Disassembler and buffers the data to the S/UNI device such that the dummy stuff byte in byte position 6 (of a 54 byte/27word cell structure) is taken into account. Figure 10 shows the circuitry required by the TX Data Flow Control block. It consists of a 6 bit gray counter, an 8 bit register, a JK DFF, a DFF and a sixteen bit 2-1 multiplexer controlled by some glue logic.

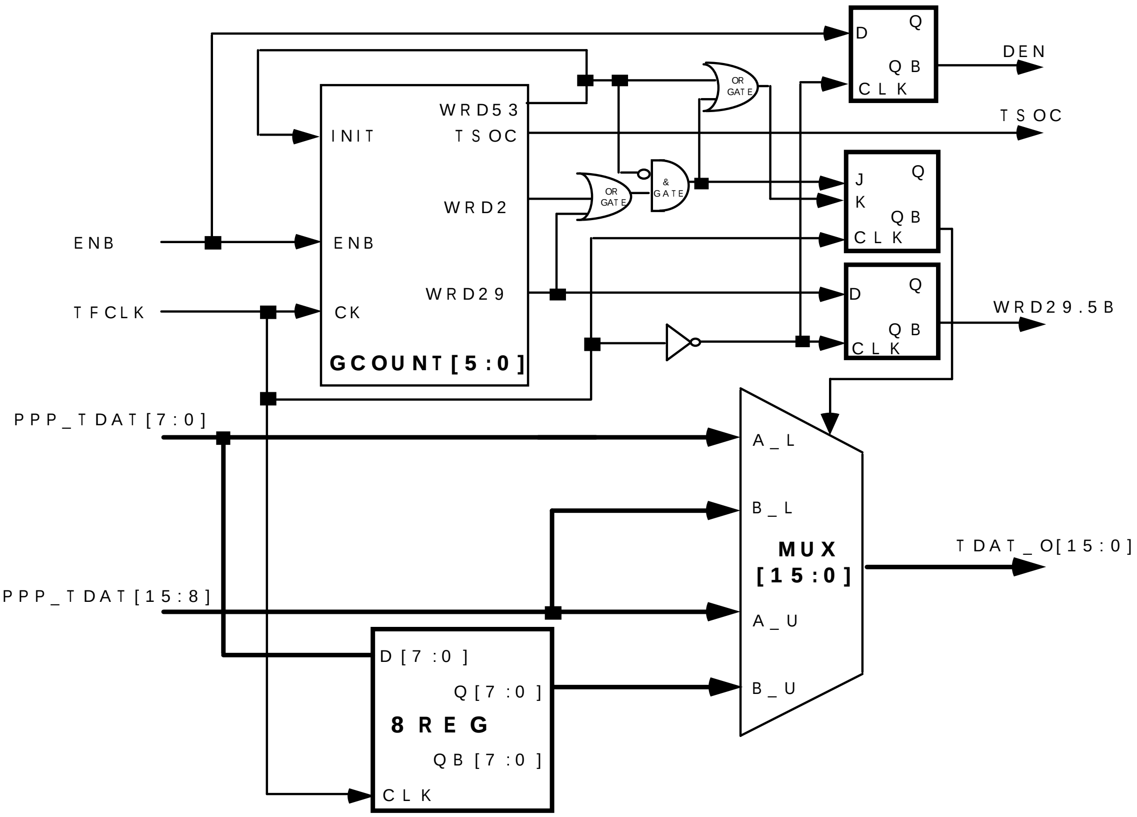


Figure 10: TX Data Flow Control.

The TSOC output is generated every 27 words written into the S/UNI device. The TSOC output will be generated when the counter is in state 0 (indicating the first word of the first 27 word structure) or when it is in state 27 (indicating the first word of the 2nd 27 word structure. The counter is disabled when the ENB input is low and will be controlled by the TCA signal from the S/UNI device. The WRD_29.5B output is active on the falling edge of clock and is the retimed version of the WRD_29 output of the counter. WRD_29 is active high when the counter reaches state 29. This information is shown in the timing diagram of figure 11. The DEN output is a half clock period delayed version of the ENB input. This output is used to gap out the clock to the PPP/POS Cell Assembler Disassembler during FIFO full periods.

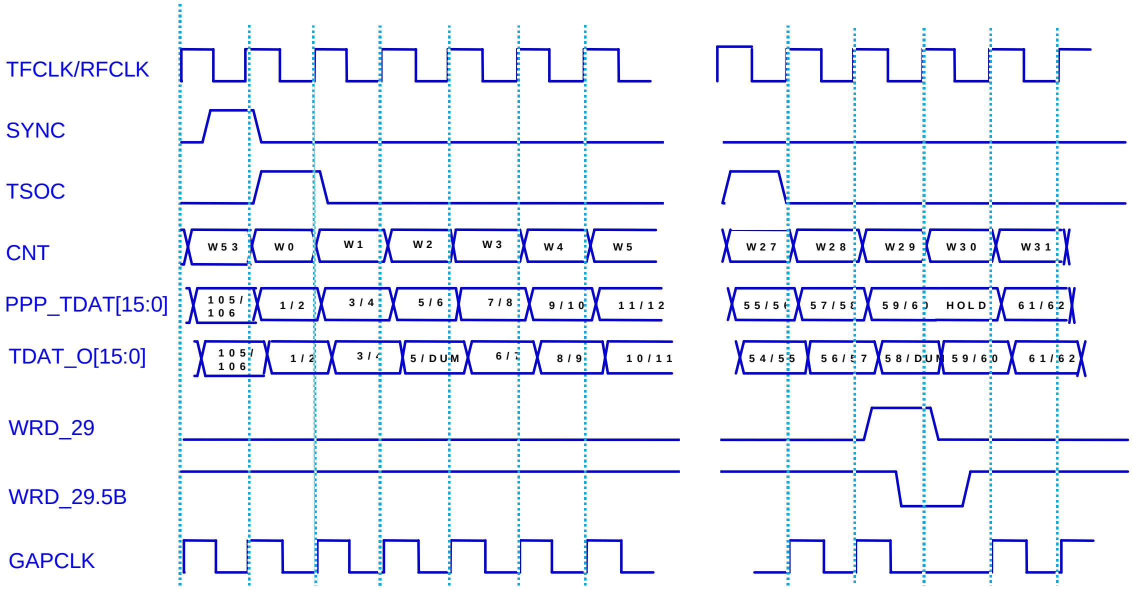


Figure 11: TX Data Flow Control Timing

The data flow is controlled by the 8 bit register and the multiplexer and the output of the JK flip-flop. Assuming the byte order output from the PPP/POS Cell Assembler/Disassembler is byte numbers 1-2, 3-4, ...53-54, 55-56,......105-106, 1-2, 3-4.....etc. then the TX Data Flow Control will output bytes to the S/UNI device in the order 1-2, 3-4, 5-DUM, 6-7, 8-9, ...52-53, 54-55, 56-57, 58-DUM, ...105-106, 1-2....etc. Where DUM is the stuffed dummy bytes in the 6th byte location of each 27 word data structure. Note, the HCSCTLEB bit must be set to logic 0 to disable the effect of the dummy byte on the HEC octet sent out on the line. The PPP_TDAT[15:0] trace shows the data sourced by the PPP/POS Cell Assembler/Disassembler and the TDAT_O[15:0] trace shows the data being written into the S/UNI device. The gap of one clock cycle is generated to the PPP/POS Cell Assembler/Disassembler during the time the S/UNI is sampling the 58-DUM word. During the gap period the data from the PPP/POS Cell Assembler/Disassembler is shown as being held at the previous byte value, although in reality it is a don't care.

The upper byte data is input on the PPP_TDAT[15:8] inputs and is driven by the PPP/POS Cell Assembler/Disassembler. Similarly the lower byte data is driven by the PPP/POS Cell Assembler/Disassembler on the PPP_TDAT[7:0] inputs. The data selection on the multiplexer is controlled by the output of the JK flip-flop and requires the counter to pass through state 53 before the JK-FF is properly initialized. After initialization the multiplexer passes the data straight through, i.e. A_L and A_U inputs pass through to the TDAT_O[15:0] outputs. This is the normal mode of operation. The 8 bit register continually samples the lower byte of the PPP_TDAT inputs. This continues until the third word of the 1st 27 word data structure is passed to the S/UNI device. At same time as the rising edge that samples W2 at the S/UNI device, the JK-FF will toggle to the opposite state. This causes the multiplexer to select the stored version of the previous words lower byte and direct it to the upper byte of TDAT_O. At the same time, the upper byte on PPP_TDAT is directed to the lower byte on TDAT_O. Essentially, this mode of operation compensates for the dummy byte that was transmitted during the W2 time. This mode of operation continues until the third byte (i.e. during W29) of the next 27 word data structure. At this time the S/UNI device samples the third word, (with the lower byte of TDAT_O originating from the upper byte of PPP_TDAT and the upper byte of TDAT_O originating from the previous words PPP_TDAT lower byte) while at the same time the clock to the PPP/POS Cell Assembler/Disassembler is gapped. This gapping accounts for the two dummy bytes inserted by the TX Flow Control during the previous W2 and W29 word times. At the end of the gapped cycle period, the JK-FF toggles back and the control to the multiplexer reverts to the normal mode of operation, i.e. such that the PPP_TDAT[7:0] inputs map to the TDAT_O[7:0] outputs and PPP_TDAT[15:8] inputs map to the TDAT_O[15:8] outputs. When the counter reaches state 53 it will naturally transition back to the 0 state to start the 54 word transfer process again.

2.2.1.1 GCOUNT[5:0]

This counter is ideally a gray code counter with 54 states. It is initialized by INIT on the rising edge of clock and will stop counting when the ENB input is at logic 1. The TSOC output is valid during state 0. The WRD2 output is generated during state 2, and the WRD29 output is generated during state 29. The WRD53 output is generated during state 53 for one clock period. The CK input is the clock input. A normal counter can be used, however a gray counter should be considered when timing is critical. Note: All decoded outputs, such as the WRD2 output, are valid only when the enable ENB is active. When the counter is held disabled during a state that would normally generate a decoded output, then that output is held inactive.

2.2.1.2 MUX[15:0]

This sub-block is a 16 bit wide 2 to 1 multiplexer.

2.2.1.3 8REG

This sub-block is a 8 bit register that samples the input on the rising edge of CLK.

2.2.2 Scrambler

Since the scrambling function of the ATM payload must be disabled by the ATM bypass process, the PPP data must be scrambled externally. Figure 12 below shows the scrambler circuit. This implementation is based on the $X^{43} + 1$ polynomial implemented on a word wide basis. To understand what is happening in this circuit it is simpler to imagine a bit serial stream being XORed with a one clock delayed version of the XOR gate output. The output of the XOR gate is the bit serial scrambled data. In the implementation shown in figure 12, the XOR function is a 16 bit wide bus operating with 16 XOR gates in parallel together with the oldest 16 bits from a 43 bit shift register. The shift register shifts 16 bits at a time and the shifted bits eventually fall off the end. The end result is the same as described for the bit serial case.

The descrambling circuit (described later in this document) will operate on this scrambled data and will self synchronize. No external synchronization signal is required.

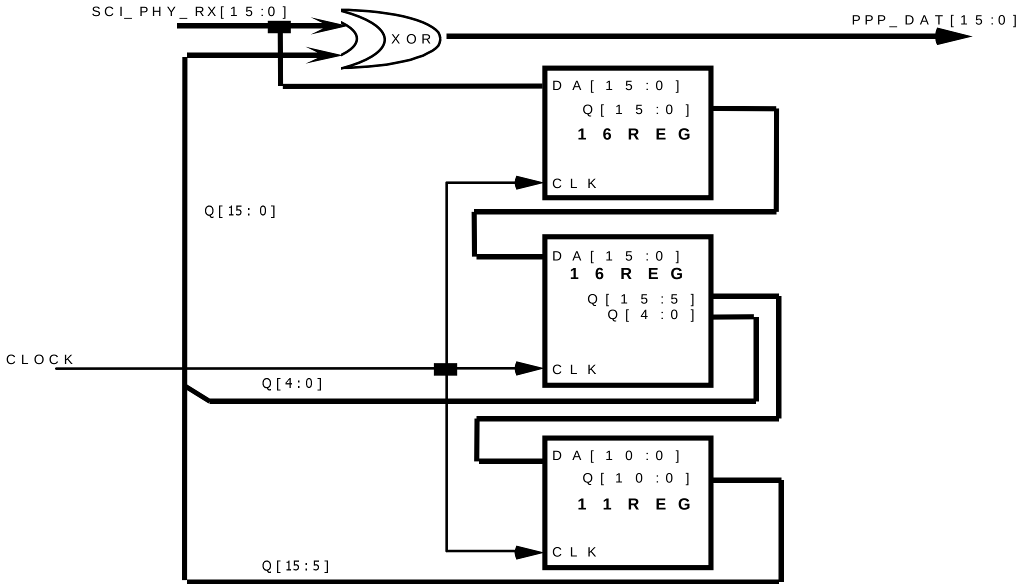


Figure 12: TX Data Scrambler

2.2.2.1 16REG

This block is a sixteen bit parallel input parallel output register clocked on the rising edge of clock.

2.2.2.2 11REG

This block is an eleven bit parallel input parallel output register clocked on the rising edge of clock.

2.2.3 RX Data Flow Control

The RX Data Flow Control block controls the clock gapping to the PPP/POS Assembler Disassembler and buffers the data such that the dummy stuff byte from the S/UNI device is extracted and discarded. Figure 12 shows the circuitry required by the RX Data Flow Control block. It consists of a 6 bit gray counter, an 8 bit multiplexed register, a JK-DFF, a DFF and a sixteen bit 2-1 multiplexer controlled by some glue logic. This block is architecturally similar to the TX Data Flow Control block but performs the exact inverse function. It converts the 54 words of data received from the S/UNI device to 53 words of data by extracting the two dummy bytes in words W2 and W29.

Every odd occurrence of RSOC synchronizes the gray counter to its second state (identifying W1) on the rising edge of clock. The gray counter has 54 states and initializes itself back to the 0 state after reaching state 53. The WRD29 and WRD2 outputs of the gray counter are used to toggle the JK-FF and this in turn controls the mode of operation of the circuit. The JK-FF is reset to logic 0 on the rising edge when the RSOC input is received. The DFF retimes the WRD2 signal from the gray counter to the falling edge and its output is used to gap the clock to the PPP/POS Cell Assembler/Disassembler.

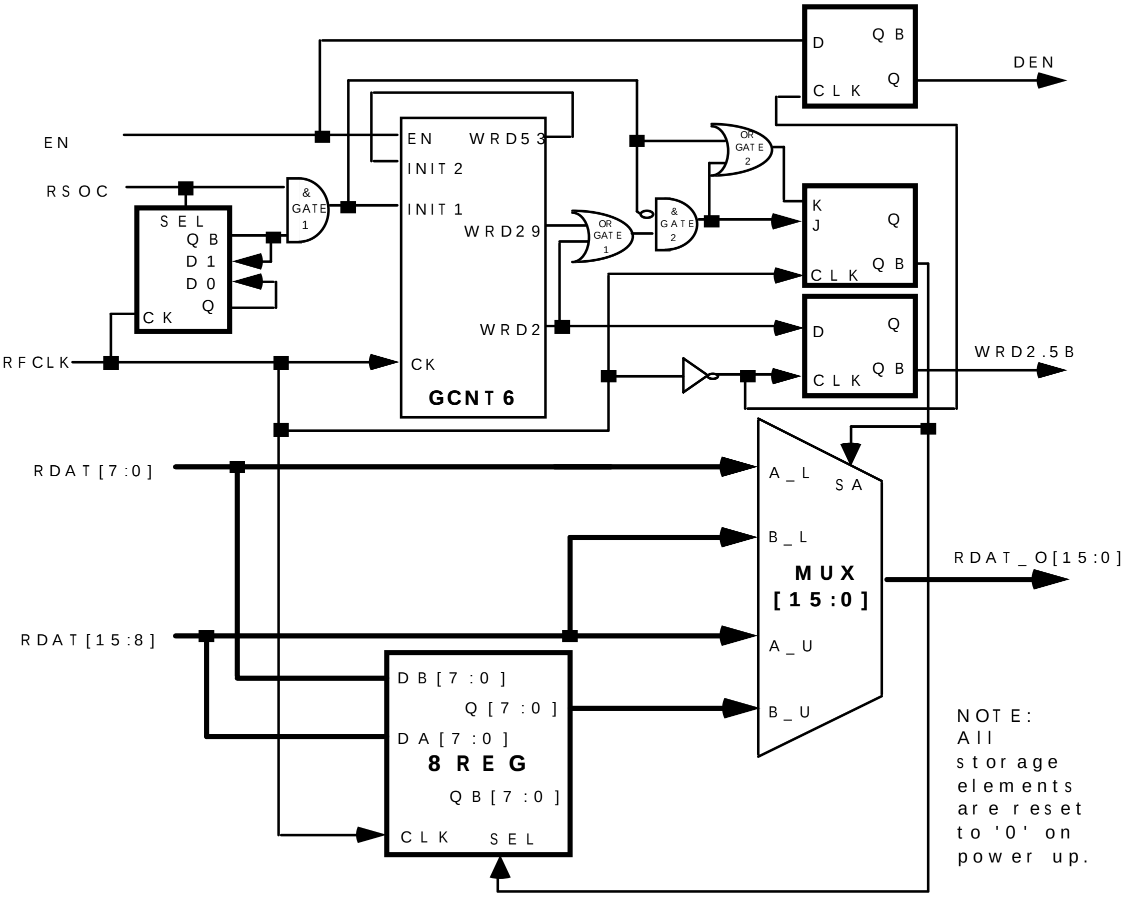


Figure 13: RX Data Flow Control.

The RX Data Flow Control circuit operates in two distinct states, state S0 and S1. Operation in state S0 is achieved when the JK-FF is reset by the RSOC input or the WRD29 output from the gray counter.

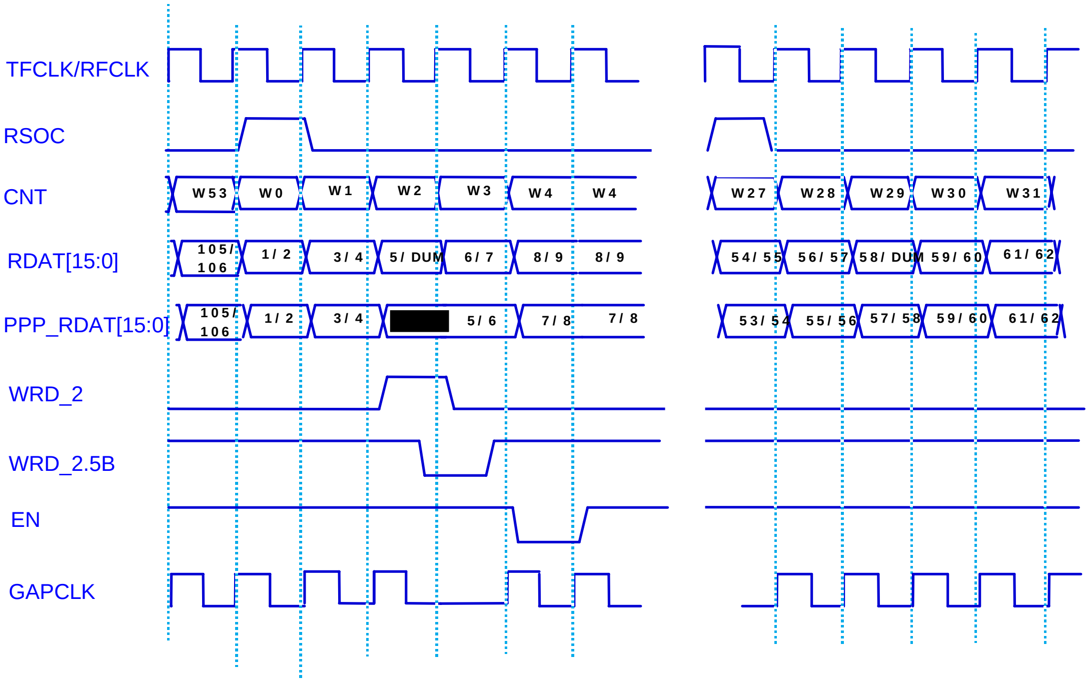


Figure 14: RX Data Flow Control.

Operation in state S1 is achieved when the JK-FF is set, by the gray counters WRD2 output being high. In state S0 the gray counter will be processing words W3 - W29 on the SCI-PHY data bus and in state S1 the gray counter will be processing words W0 - W2 and W30 - W53 on the SCI-PHY data bus. Figure 14 shows the operational timing related to this block.

When operating in state S0, the 8 bit multiplexed register stores the upper byte of RDAT[16:0] and the 16 bit multiplexer selects the RDAT[16:0] inputs directly to the PPP_RDAT_O[15:0] outputs. When operating in state S1, the 8 bit multiplexed register stores the lower byte of RDAT[16:0] and the 16 bit multiplexer connects the RDAT[15:8] inputs to the PPP_RDAT_O[7:0] outputs and connects the output of the multiplexed register to the PPP_RDAT_O[15:8] outputs. This process, together with the one clock gap inserted during W3, ensures that the stuff bytes are filtered and the PPP data is passed through.

The EN input enables the gray counter. When EN is logic 1 the counter will increment at each rising edge of clock. When EN is logic 0 the counter is held at the last count and all decoded count values are inhibited by logically ANDing the EN input with the decoded count. Therefore, all outputs from GCNT6 are inactive when the EN input is logic 0. The DEN output is the EN input retimed to the falling edge of clock.

2.2.3.1 GCNT6

This counter is a gray code counter with 54 states. It is initialized by INIT1 and INIT2 on the rising edge of clock. The counter is initialized to the first state when initialized by INIT1 and to the second state when initialized by INIT2. The CK input is the clock input. The EN input is an active high enable. Note: All outputs from this block are held inactive whenever the enable EN is inactive. i.e WRD29 is held inactive when the counter is held in the 29th state while the EN input is logic 0.

2.2.3.2 MUX[15:0]

This sub-block is a 16 bit wide 2 to 1 multiplexer.

2.2.3.3 8REG

This sub-block is a 8 bit register that samples the input on the rising edge of CLK.

2.2.4 Descrambler

Since the descrambling function of the ATM payload must be disabled by the ATM bypass process, the PPP data must be descrambled externally. Figure 15 below shows the descrambler circuit. This implementation is based on the $X^{43} + 1$ polynomial implemented on a word wide basis. To understand what is happening in this circuit it is simpler to imagine a bit serial stream being XORed with a one clock delayed version of the XOR gate output. The output of the XOR gate is the bit serial descrambled data. In the implementation shown in figure 15, the XOR function is a 16 bit wide bus operating with 16 XOR gates in parallel together with the oldest 16 bits from a 43 bit shift register. The shift register shifts 16 bits at a time and the shifted bits eventually fall off the end. The end result is the same as described for the bit serial case.

The scrambling circuit (described earlier in this document) operates in a similar fashion. No external synchronization signal is required since the descrambler is self synchronizing.

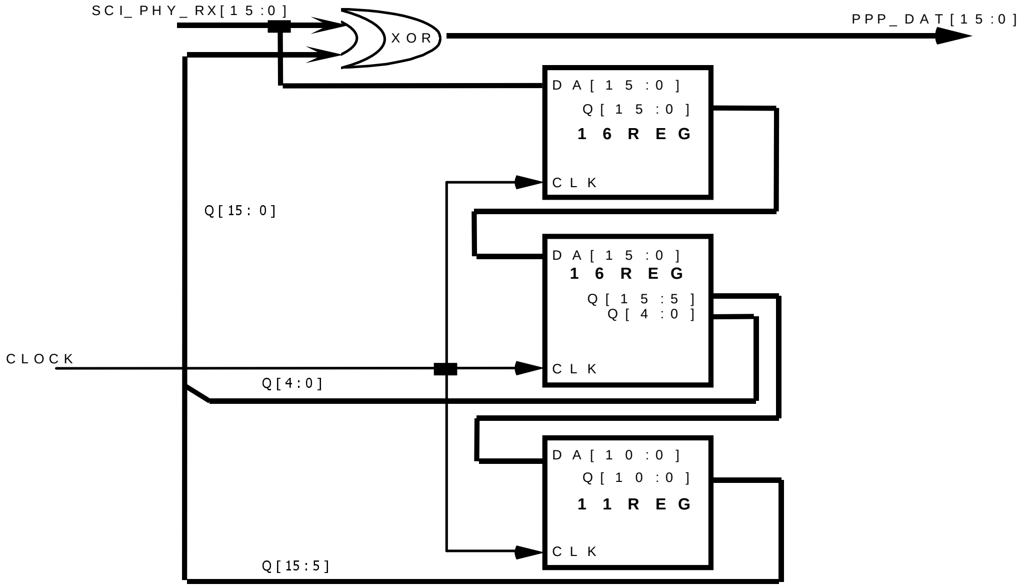


Figure 15: RX Data Descrambler

2.2.4.1 16REG

This block is a sixteen bit parallel input parallel output register clocked on the rising edge of clock.

2.2.4.2 11REG

This block is an eleven bit parallel input parallel output register clocked on the rising edge of clock.

3 8 BIT SCI_PHY BUS : ATM BYPASS WITH 8 BIT 53 BYTE DATA I/F.

The PM5347 SUNI-PLUS contains an option that disables the ATM Cell Processing and allows raw data to be inserted or extracted from the SONET Payload.

Figure 4 and figure 5 and the software programming still apply to this mode of operation exactly as described in the 27 word 16 bus operation mode. The main difference for this mode of operation is that there are no dummy/stuff bytes at the SCI-PHY interface. Since there are no stuff bytes to process, the interface circuitry between the PPP/POS Cell Assembler/Disassembler and the S/UNI device requires only a subset of the circuitry shown in figure 9.

As a result, figure 9 simplifies to the figure shown in figure 16, figure 10 simplifies to the figure shown in figure 17 and figure 13 simplifies to the figure shown in figure 18.

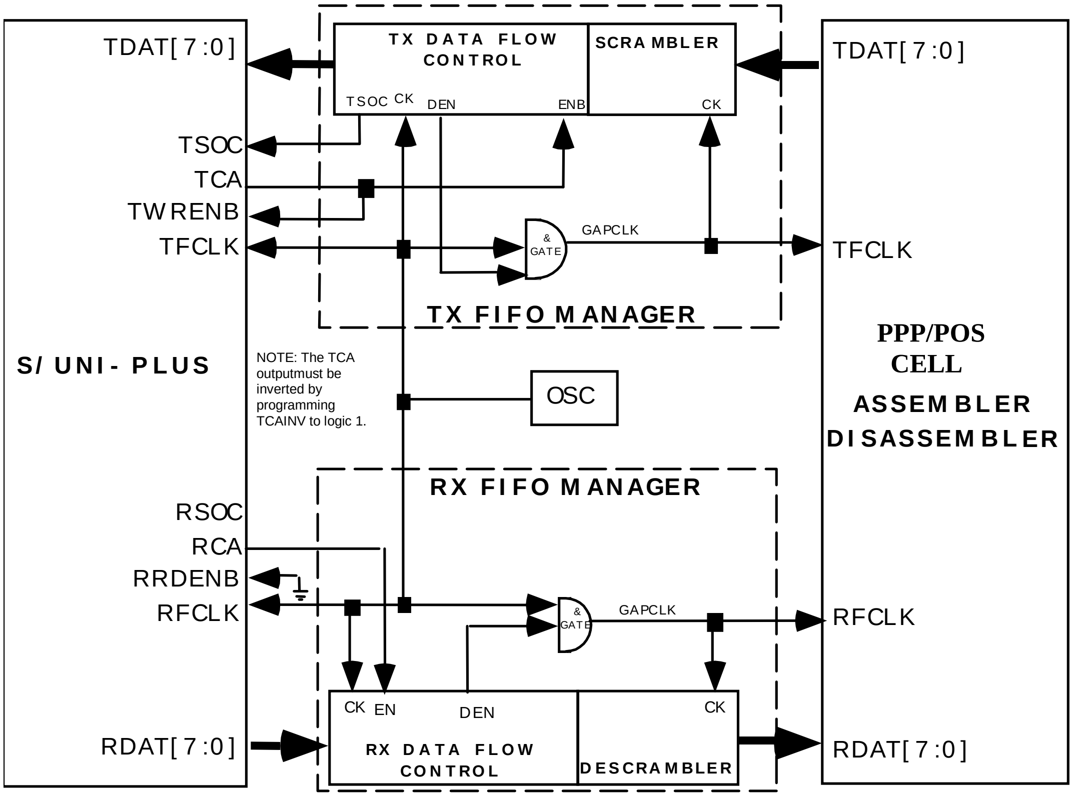


Figure 16: PPP over an STS-3c or an STS-1 Link Using 8 Bit Bus Interface.

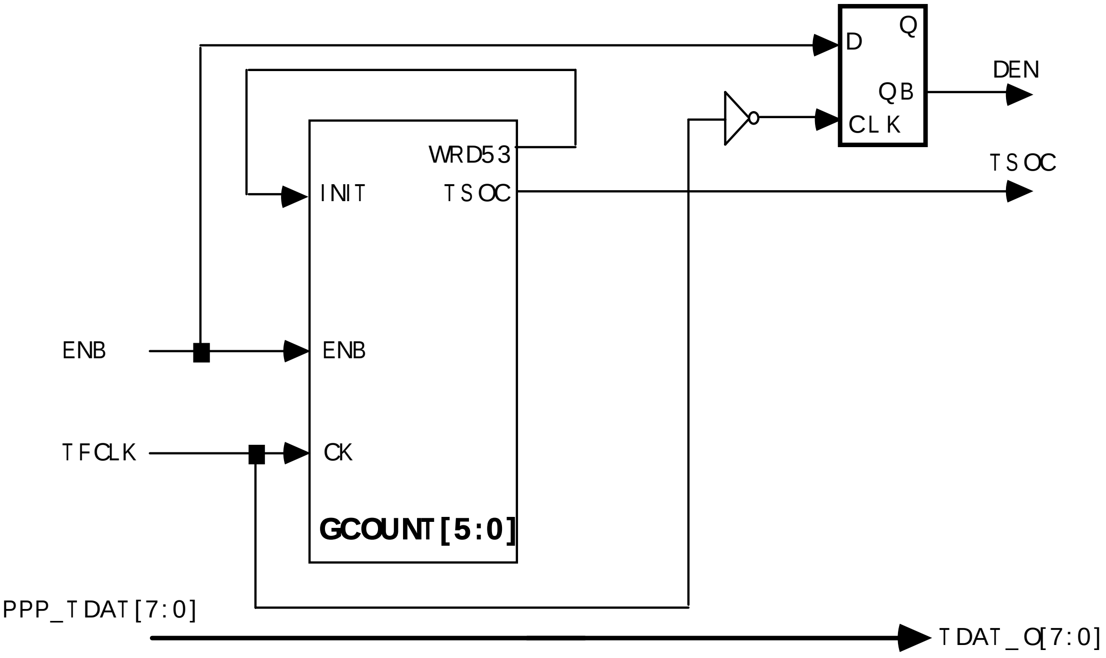


Figure 17: TX Data Flow Control.

In the transmit direction, the scrambler block remains unchanged and the TX Data Flow Control simplifies to the circuit shown in figure 17.

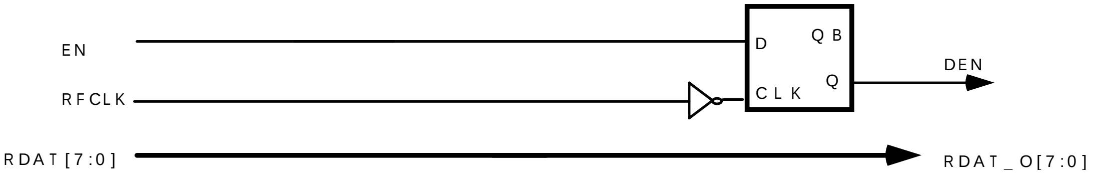


Figure 18: RX Data Flow Control.

In the receive direction, the descrambler block remains unchanged and the RX Data Flow Control simplifies to the circuit shown in figure 18.

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